E. Lattice Semiconductor Corporation - <u>LFE3-95EA-8FN1156C Datasheet</u>



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-8fn1156c

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PLL/DLL Cascading

LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

The DLLs in the LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

PLL/DLL PIO Input Pin Connections

All LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 2-7.

Figure 2-7. Sharing of PIO Pins by PLLs and DLLs in LatticeECP3 Devices



Note: Not every PLL has an associated DLL.

Clock Dividers

LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide. Figure 2-8 shows the clock divider connections.



MULTADDSUBSUM DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 0. Additionally, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 1. The results of both addition/subtractions are added by the second ALU following the slice cascade path. The user can enable the input, output and pipeline registers. Figure 2-30 and Figure 2-31 show the MULTADDSUBSUM sysDSP element.

Figure 2-30. MULTADDSUBSUM Slice 0





Figure 2-31. MULTADDSUBSUM Slice 1



Advanced sysDSP Slice Features

Cascading

The LatticeECP3 sysDSP slice has been enhanced to allow cascading. Adder trees are implemented fully in sys-DSP slices, improving the performance. Cascading of slices uses the signals CIN, COUT and C Mux of the slice.

Addition

The LatticeECP3 sysDSP slice allows for the bypassing of multipliers and cascading of adder logic. High performance adder functions are implemented without the use of LUTs. The maximum width adders that can be implemented are 54-bit.

Rounding

The rounding operation is implemented in the ALU and is done by adding a constant followed by a truncation operation. The rounding methods supported are:

- Rounding to zero (RTZ)
- Rounding to infinity (RTI)
- Dynamic rounding
- Random rounding
- Convergent rounding



Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysl/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysl/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-32. PIC Diagram



* Signals are available on left/right/top edges only.

** Signals are available on the left and right sides only

*** Selected PIO.



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-32. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as LVDS inputs.

Table 2-11. PIO Signal List

Name	Туре	Description
INDD	Input Data	Register bypassed input. This is not the same port as INCK.
IPA, INA, IPB, INB	Input Data	Ports to core for input data
OPOSA, ONEGA ¹ , OPOSB, ONEGB ¹	Output Data	Output signals from core. An exception is the ONEGB port, used for tristate logic at the DQS pad.
CE	PIO Control	Clock enables for input and output block flip-flops.
SCLK	PIO Control	System Clock (PCLK) for input and output/TS blocks. Connected from clock ISB.
LSR	PIO Control	Local Set/Reset
ECLK1, ECLK2	PIO Control	Edge clock sources. Entire PIO selects one of two sources using mux.
ECLKDQSR ¹	Read Control	From DQS_STROBE, shifted strobe for memory interfaces only.
DDRCLKPOL ¹	Read Control	Ensures transfer from DQS domain to SCLK domain.
DDRLAT ¹	Read Control	Used to guarantee INDDRX2 gearing by selectively enabling a D-Flip-Flop in dat- apath.
DEL[3:0]	Read Control	Dynamic input delay control bits.
INCK	To Clock Distribution and PLL	PIO treated as clock PIO, path to distribute to primary clocks and PLL.
TS	Tristate Data	Tristate signal from core (SDR)
DQCLK0 ¹ , DQCLK1 ¹	Write Control	Two clocks edges, 90 degrees out of phase, used in output gearing.
DQSW ²	Write Control	Used for output and tristate logic at DQS only.
DYNDEL[7:0]	Write Control	Shifting of write clocks for specific DQS group, using 6:0 each step is approxi- mately 25ps, 128 steps. Bit 7 is an invert (timing depends on input frequency). There is also a static control for this 8-bit setting, enabled with a memory cell.
DCNTL[6:0]	PIO Control	Original delay code from DDR DLL
DATAVALID ¹	Output Data	Status flag from DATAVALID logic, used to indicate when input data is captured in IOLOGIC and valid to core.
READ	For DQS_Strobe	Read signal for DDR memory interface
DQSI	For DQS_Strobe	Unshifted DQS strobe from input pad
PRMBDET	For DQS_Strobe	DQSI biased to go high when DQSI is tristate, goes to input logic block as well as core logic.
GSRN	Control from routing	Global Set/Reset

1. Signals available on left/right/top edges only.

2. Selected PIO.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs, in the left, right and top edges, contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-33 shows the input register block for the left, right and top edges. The input register block for the bottom edge contains one element to register the input signal and no DDR registers. The following description applies to the input register block for PIOs in the left, right and top edges only.







Note: Simplified diagram does not show CE/SET/REST details.

Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysl/O buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDRX2 gearing of output logic. ODDRX2 gearing is used in DDR3 memory interfaces. The PIO blocks on the bottom contain the SDR registers but do not support generic DDR.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.



Package	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
256 ftBGA	1	1	—	—	—
328 csBGA	2 channels	—	—	—	—
484 fpBGA	1	1	1	1	
672 fpBGA	—	1	2	2	2
1156 fpBGA	—	—	3	3	4

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block



PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.



SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond and ispLEVER design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

Table 2-15. LatticeECP3 Primary and Secondary Protocol Support

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI



SERDES Power Supply Requirements^{1, 2, 3}

Symbol	Description	Тур.	Max.	Units
Standby (Power Do	own)	•		1
I _{CCA-SB}	V _{CCA} current (per channel)	3	5	mA
I _{CCIB-SB}	Input buffer current (per channel)		—	mA
I _{CCOB-SB}	Output buffer current (per channel)	—	_	mA
Operating (Data Ra	ite = 3.2 Gbps)		•	•
I _{CCA-OP}	V _{CCA} current (per channel)	68	77	mA
I _{CCIB-OP}	Input buffer current (per channel)	5	7	mA
I _{CCOB-OP}	Output buffer current (per channel)	19	25	mA
Operating (Data Ra	ite = 2.5 Gbps)	·		·
I _{CCA-OP}	V _{CCA} current (per channel)	66	76	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	15	18	mA
Operating (Data Ra	te = 1.25 Gbps)			·
I _{CCA-OP}	V _{CCA} current (per channel)	62	72	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	15	18	mA
Operating (Data Ra	ite = 250 Mbps)	·		·
I _{CCA-OP}	V _{CCA} current (per channel)	55	65	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	14	17	mA
Operating (Data Ra	ite = 150 Mbps)	·		·
I _{CCA-OP}	V _{CCA} current (per channel)	55	65	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	5	mA
I _{CCOB-OP}	Output buffer current (per channel)	14	17	mA

1. Equalization enabled, pre-emphasis disabled.

2. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).

3. Pre-emphasis adds 20 mA to ICCA-OP data.



sysI/O Differential Electrical Characteristics LVDS25

Parameter	Description	Test Conditions	Min.	Тур.	Max.	Units
V _{INP} ¹ , V _{INM} ¹	Input Voltage		0	_	2.4	V
V _{CM} ¹	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	_	2.35	V
V _{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	_	_	mV
I _{IN}	Input Current	Power On or Power Off		_	+/-10	μΑ
V _{OH}	Output High Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm		1.38	1.60	V
V _{OL}	Output Low Voltage for V_{OP} or V_{OM}	R _T = 100 Ohm	0.9 V	1.03	_	V
V _{OD}	Output Voltage Differential	(V _{OP} - V _{OM}), R _T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V _{OD} Between High and Low		_	_	50	mV
V _{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2$, R _T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V _{OS} Between H and L		_	_	50	mV
I _{SAB}	Output Short Circuit Current	V _{OD} = 0V Driver Outputs Shorted to Each Other	_	_	12	mA

1, On the left and right sides of the device, this specification is valid only for $V_{CCIO} = 2.5$ V or 3.3 V.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

						6			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
f _{MAX GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250		250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-35EA	683	_	688		690	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	683	—	688	—	690	_	ps
f _{MAX GDDR}	DDRX1 Clock Frequency	ECP3-35EA	—	250	—	250	_	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	683	_	688		690		ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	683	—	688	—	690	_	ps
f _{MAX GDDR}	DDRX1 Clock Frequency	ECP3-17EA	—	250	_	250	_	250	MHz
Generic DDRX1 Ou	tput with Clock and Data Aligne	d at Pin (GDDRX1_TX.	SCLK.Ali	gned) ¹⁰					
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-150EA	—	335	—	338	—	341	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-150EA	—	335	—	338		341	ps
f _{MAX} GDDR	DDRX1 Clock Frequency	ECP3-150EA	_	250	_	250		250	MHz
	Data Invalid Before Clock	ECP3-70EA/95EA	_	339	_	343		347	ps
t _{DIAGDDB}	Data Invalid After Clock	ECP3-70EA/95EA	_	339	_	343		347	ps
f _{MAX} GDDR	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250		250	MHz
	Data Invalid Before Clock	ECP3-35EA		322		320		321	ps
	Data Invalid After Clock	ECP3-35EA	_	322	_	320		321	ps
f _{MAX GDDB}	DDRX1 Clock Frequency	ECP3-35EA	_	250	_	250		250	MHz
	Data Invalid Before Clock	ECP3-17EA		322		320		321	ps
	Data Invalid After Clock	ECP3-17EA	_	322	_	320		321	ps
f _{MAX GDDB}	DDRX1 Clock Frequency	ECP3-17EA	_	250	_	250		250	MHz
Generic DDRX1 Ou	Itput with Clock and Data (<10 B	its Wide) Centered at F	in (GDD	RX1_TX.	DQS.Cen	tered) ¹⁰			
Left and Right Side	25		-			-			
t _{DVBGDDR}	Data Valid Before CLK	ECP3-150EA	670		670		670	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-150EA	670	_	670	_	670	_	ps
f _{MAX GDDB}	DDRX1 Clock Frequency	ECP3-150EA	_	250	_	250	_	250	MHz
	Data Valid Before CLK	ECP3-70EA/95EA	657		652		650	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-70EA/95EA	657	_	652		650	_	ps
f _{MAX GDDB}	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250	_	250	MHz
	Data Valid Before CLK	ECP3-35EA	670		675		676	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	670	—	675	—	676	_	ps
f _{MAX GDDR}	DDRX1 Clock Frequency	ECP3-35EA	—	250	—	250	_	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	670	—	670	—	670	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	670	_	670	_	670	_	ps
f _{MAX} GDDR	DDRX1 Clock Frequency	ECP3-17EA	_	250	_	250		250	MHz
Generic DDRX2 Ou	tput with Clock and Data (>10 B	its Wide) Aligned at Pi	n (GDDR	X2_TX.A	ligned)				
Left and Right Side	es								
t _{DIBGDDR}	Data Invalid Before Clock	All ECP3EA Devices	—	200	—	210	_	220	ps
t _{DIAGDDR}	Data Invalid After Clock	All ECP3EA Devices	—	200	—	210	—	220	ps
f _{MAX GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	500	_	420	_	375	MHz
Generic DDRX2 Ou	tput with Clock and Data (>10 B	its Wide) Centered at P	in Using	DQSDL	L (GDDF	X2_TX.C	QSDLL.	Centered)11
Left and Right Side	S								
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	400		400		431	_	ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	400	—	400	—	432	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz

Over Recommended Commercial Operating Conditions



Figure 3-8. Generic DDRX1/DDRX2 (With Clock Center on Data Window)





LatticeECP3 Internal Switching Characteristics^{1, 2, 5}

		-8		-7		-6		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units.
PFU/PFF Logi	c Mode Timing							
t _{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.147	_	0.163	_	0.179	ns
t _{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.281		0.335	_	0.379	ns
t _{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.593	—	0.674	—	0.756	ns
t _{LSRREC_PFU}	Asynchronous Set/Reset recovery time for PFU Logic		0.298		0.345		0.391	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.134	_	0.144	_	0.153		ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.097	_	-0.103	_	-0.109	_	ns
t _{SUD_PFU}	Clock to D input setup time	0.061	_	0.068	_	0.075		ns
t _{HD_PFU}	Clock to D input hold time	0.019	_	0.013	_	0.015		ns
t _{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	_	0.243	_	0.273	_	0.303	ns
PFU Dual Port	Memory Mode Timing							
t _{CORAM_PFU}	Clock to Output (F Port)	—	0.710	—	0.803	—	0.897	ns
t _{SUDATA_PFU}	Data Setup Time	-0.137	_	-0.155	_	-0.174		ns
t _{HDATA_PFU}	Data Hold Time	0.188	_	0.217	_	0.246	_	ns
t _{SUADDR_PFU}	Address Setup Time	-0.227	_	-0.257	_	-0.286		ns
t _{HADDR_PFU}	Address Hold Time	0.240	_	0.275	_	0.310	_	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.055		-0.055	-	-0.063	_	ns
t _{HWREN_} PFU	Write/Read Enable Hold Time	0.059	_	0.059	_	0.071	_	ns
PIC Timing								
PIO Input/Out	out Buffer Timing							
t _{IN_PIO}	Input Buffer Delay (LVCMOS25)		0.423		0.466		0.508	ns
t _{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.241	_	1.301	_	1.361	ns
IOLOGIC Inpu	t/Output Timing							
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.956		1.124		1.293		ns
t _{HI_PIO}	Input Register Hold Time (Data after Clock)	0.225		0.184		0.240		ns
t _{COO_PIO}	Output Register Clock to Output Delay ⁴	-	1.09	-	1.16	-	1.23	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	0.220	_	0.185	_	0.150	_	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	-0.085		-0.072		-0.058		ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.117	_	0.103	_	0.088	_	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.107	_	-0.094	_	-0.081	_	ns
EBR Timing								
t _{CO_EBR}	Clock (Read) to output from Address or Data	—	2.78	—	2.89	—	2.99	ns
t _{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.31	—	0.32	—	0.33	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.218	_	-0.227	_	-0.237	_	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.249		0.257		0.265	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	-0.071		-0.070		-0.068		ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.118		0.098		0.077		ns
t _{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	-0.107	_	-0.106	_	-0.106	—	ns

Over Recommended Commercial Operating Conditions



HDMI (High-Definition Multimedia Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-22. Transmit and Receive^{1, 2}

		Spec. Co		
Symbol	Description	Min. Spec.	Max. Spec.	Units
Transmit				
Intra-pair Skew		—	75	ps
Inter-pair Skew		—	800	ps
TMDS Differential Clock Jitter		—	0.25	UI
Receive				
R _T	Termination Resistance	40	60	Ohms
V _{ICM}	Input AC Common Mode Voltage (50-Ohm Set- ting)	—	50	mV
TMDS Clock Jitter	Clock Jitter Tolerance	—	0.25	UI

1. Output buffers must drive a translation device. Max. speed is 2 Gbps. If translation device does not modify rise/fall time, the maximum speed is 1.5 Gbps.

2. Input buffers must be AC coupled in order to support the 3.3 V common mode. Generally, HDMI inputs are terminated by an external cable equalizer before data/clock is forwarded to the LatticeECP3 device.



Figure 3-21. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3-22. sysCONFIG Master Serial Port Timing









Figure 3-24. Power-On-Reset (POR) Timing



Time taken from V_{CC}, V_{CCAUX} or V_{CCIO8}, whichever is the last to cross the POR trip point.
Device is in a Master Mode (SPI, SPIm).
The CFG pins are normally static (hard wired).



Figure 3-25. sysCONFIG Port Timing



sysl/O Differential Electrical Characteristics

Transition Reduced LVDS (TRLVDS DC Specification)

Over Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units
V _{CCO}	Driver supply voltage (+/- 5%)	3.14	3.3	3.47	V
V _{ID}	Input differential voltage	150	_	1200	mV
V _{ICM}	Input common mode voltage	3	_	3.265	V
V _{CCO}	Termination supply voltage	3.14	3.3	3.47	V
R _T	Termination resistance (off-chip)	45	50	55	Ohms

Note: LatticeECP3 only supports the TRLVDS receiver.



Mini LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Тур.	Max.	Units
Z _O	Single-ended PCB trace impedance	30	50	75	Ohms
R _T	Differential termination resistance	50	100	150	Ohms
V _{OD}	Output voltage, differential, V _{OP} - V _{OM}	300	_	600	mV
V _{OS}	Output voltage, common mode, $ V_{OP} + V_{OM} /2$	1	1.2	1.4	V
ΔV_{OD}	Change in V _{OD} , between H and L	—	_	50	mV
ΔV_{ID}	Change in V _{OS} , between H and L	—	_	50	mV
V _{THD}	Input voltage, differential, V _{INP} - V _{INM}	200	_	600	mV
V _{CM}	Input voltage, common mode, $ V_{INP} + V_{INM} /2$	0.3+(V _{THD} /2)	_	2.1-(V _{THD} /2)	
T _R , T _F	Output rise and fall times, 20% to 80%	—	_	550	ps
T _{ODUTY}	Output clock duty cycle	40	—	60	%

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.



Signal Descriptions (Cont.)

Signal Name	I/O	Description			
D7/SPID0	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configura- tion.			
DI/CSSPI0N/CEN	I/O	Serial data input for slave serial mode. SPI/SPIm mode chip select.			
Dedicated SERDES Signals ³					
PCS[Index]_HDINNm	I	High-speed input, negative channel m			
PCS[Index]_HDOUTNm	0	High-speed output, negative channel m			
PCS[Index]_REFCLKN	I	Negative Reference Clock Input			
PCS[Index]_HDINPm	I	High-speed input, positive channel m			
PCS[Index]_HDOUTPm	0	High-speed output, positive channel m			
PCS[Index]_REFCLKP	I	Positive Reference Clock Input			
PCS[Index]_VCCOBm		Output buffer power supply, channel m (1.2V/1.5)			
PCS[Index]_VCCIBm		Input buffer power supply, channel m (1.2V/1.5V)			

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.

2. These pins are dedicated inputs or can be used as general purpose I/O.

3. m defines the associated channel in the quad.



Pin Information Summary (Cont.)

Pin Information Summary		ECP3-95EA			ECP3-150EA		
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	672 fpBGA	1156 fpBGA	
	Bank 0	21	30	43	30	47	
	Bank 1	18	24	39	24	43	
Emulated	Bank 2	8	12	13	12	18	
Differential I/O	Bank 3	20	23	33	23	37	
per Bank	Bank 6	22	25	33	25	37	
	Bank 7	11	16	18	16	24	
	Bank 8	12	12	12	12	12	
	Bank 0	0	0	0	0	0	
	Bank 1	0	0	0	0	0	
Highspeed	Bank 2	6	9	9	9	15	
Differential I/O	Bank 3	9	12	16	12	21	
per Bank	Bank 6	11	14	16	14	21	
	Bank 7	9	12	13	12	18	
	Bank 8	0	0	0	0	0	
	Bank 0	42/21	60/30	86/43	60/30	94/47	
	Bank 1	36/18	48/24	78/39	48/24	86/43	
Total Single Ended/	Bank 2	28/14	42/21	44/22	42/21	66/33	
Total Differential	Bank 3	58/29	71/35	98/49	71/35	116/58	
I/O per Bank	Bank 6	67/33	78/39	98/49	78/39	116/58	
	Bank 7	40/20	56/28	62/31	56/28	84/42	
	Bank 8	24/12	24/12	24/12	24/12	24/12	
	Bank 0	3	5	7	5	7	
	Bank 1	3	4	7	4	7	
	Bank 2	2	3	3	3	4	
DDR Groups Bonded	Bank 3	3	4	5	4	7	
per Bank	Bank 6	4	4	5	4	7	
	Bank 7	3	4	4	4	6	
	Configuration Bank8	0	0	0	0	0	
SERDES Quads		1	2	3	2	4	

1. These pins must remain floating on the board.



Package Pinout Information

Package pinout information can be found under "Data Sheets" on the LatticeECP3 product pages on the Lattice website at http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3 and in the Diamond or ispLEVER software tools. To create pinout information from within ispLEVER Design Planner, select **Tools > Spreadsheet View**. Then select **Select File > Export** and choose a type of output file. To create a pin information file from within Diamond select **Tools > Spreadsheet View** or **Tools >Package View**; then, select **File > Export** and choose a type of output file. See Diamond or ispLEVER Help for more information.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- Power Calculator tool included with the Diamond and ispLEVER design tools, or as a standalone download from www.latticesemi.com/software