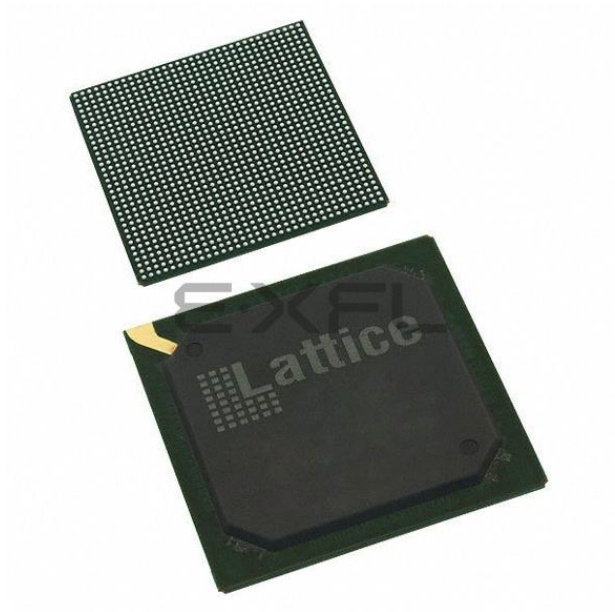
Lattice Semiconductor Corporation - LFE3-95EA-8FN1156I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

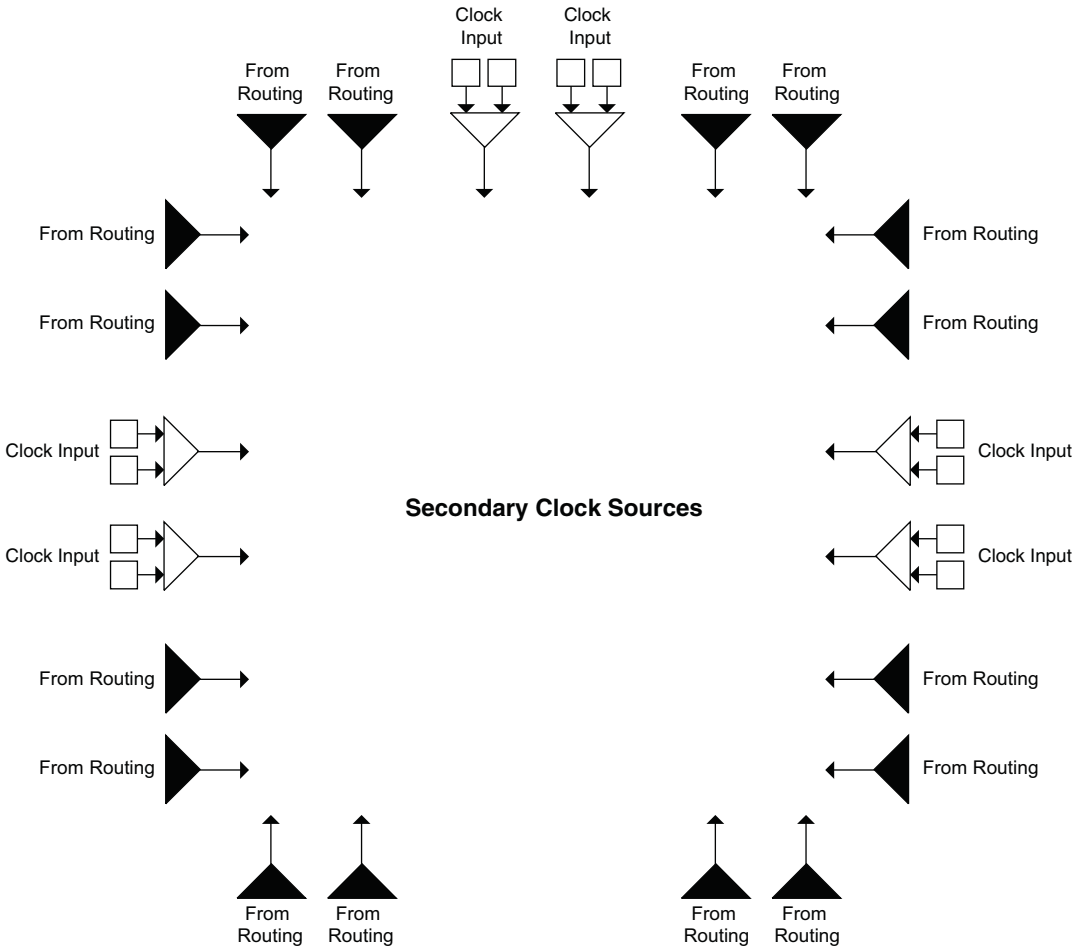
Details	
Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-8fn1156i

Secondary Clock/Control Sources

LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-14 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for the clock.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7.

Figure 2-14. Secondary Clock Sources



Note: Clock inputs can be configured in differential or single-ended mode.

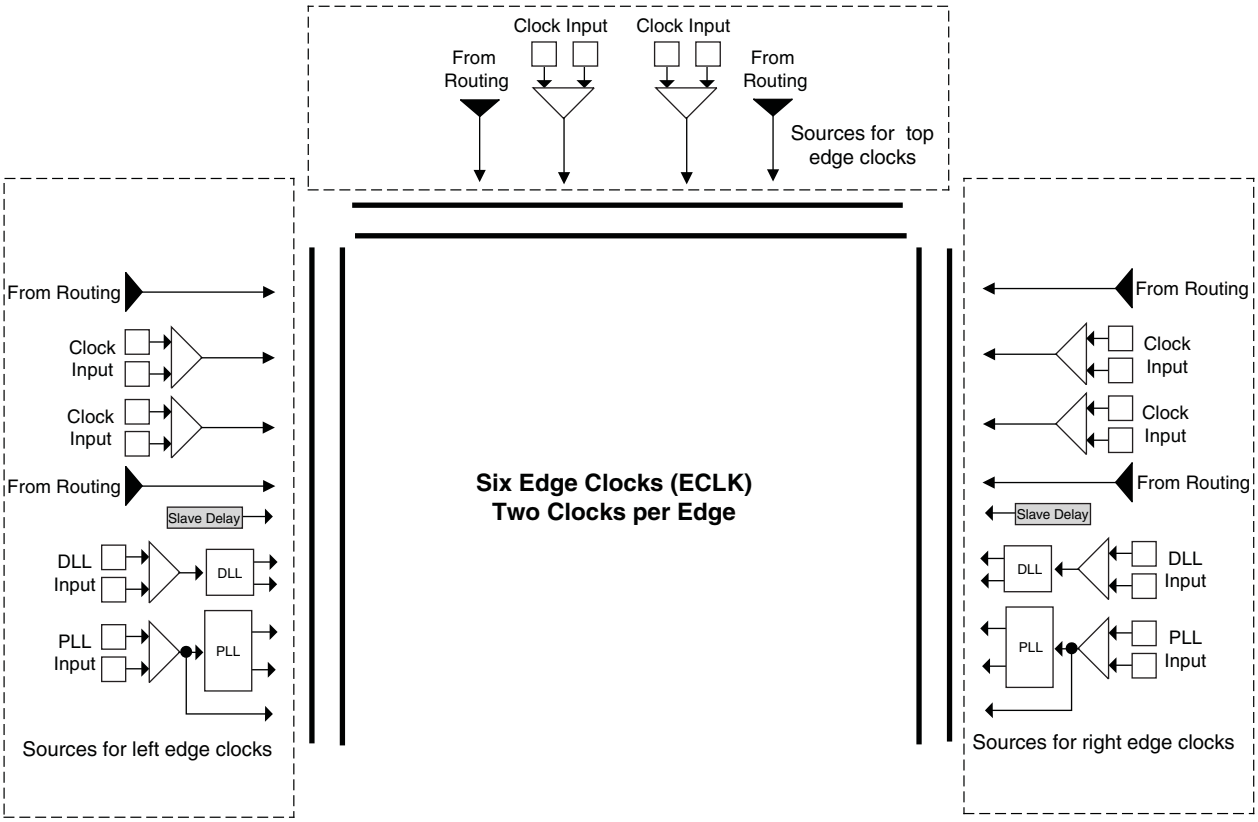
Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-15 shows this special vertical routing channel and the 20 secondary clock regions for the LatticeECP3 family of devices. All devices in the LatticeECP3 family have eight secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.

Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-19.

Figure 2-19. Edge Clock Sources



Notes:
1. Clock inputs can be configured in differential or single ended mode.
2. The two DLLs can also drive the two top edge clocks.
3. The top left and top right PLL can also drive the two top edge clocks.

Edge Clock Routing

LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-20 shows the selection muxes for these clocks.

The edge clocks on the top, left, and right sides of the device can drive the secondary clocks or general routing resources of the device. The left and right side edge clocks also can drive the primary clock network through the clock dividers (CLKDIV).

sysMEM Memory

LatticeECP3 devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-7. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths. For more information, please see TN1179, LatticeECP3 Memory Usage Guide.

Table 2-7. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

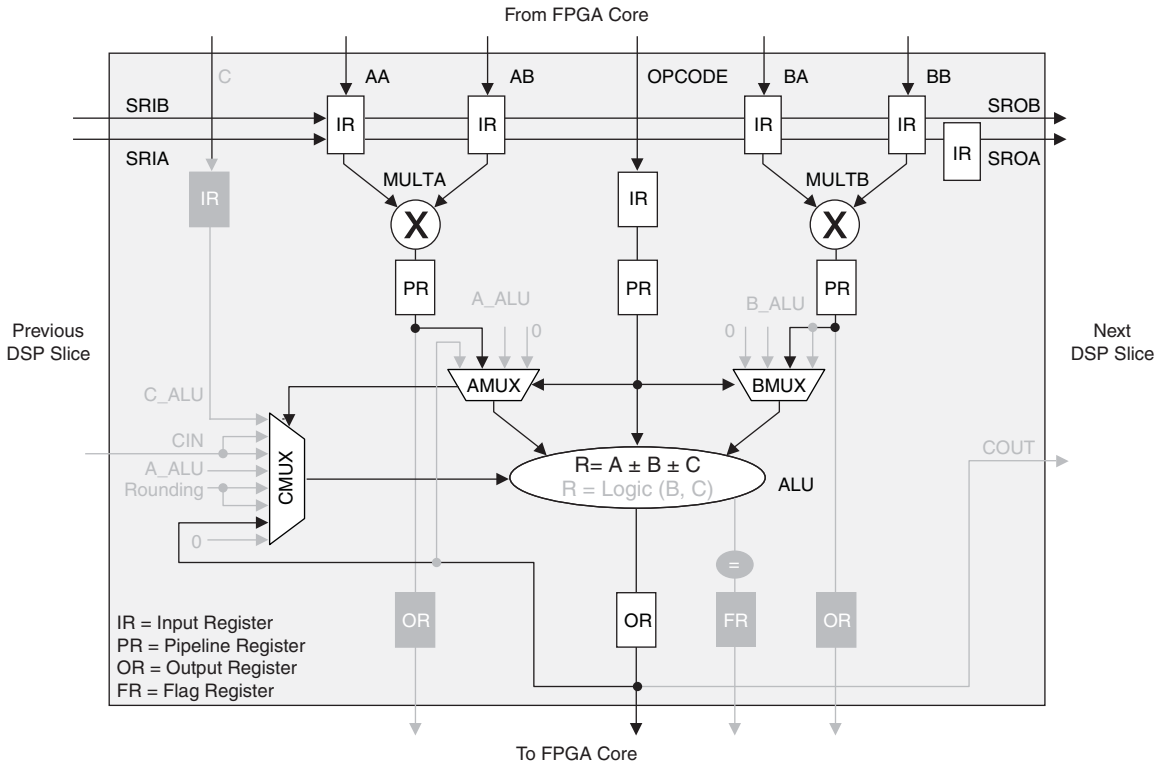
Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

MMAC DSP Element

The LatticeECP3 supports a MAC with two multipliers. This is called Multiply Multiply Accumulate or MMAC. In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value and with the result of the multiplier operation of operands BA and BB. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-28 shows the MMAC sysDSP element.

Figure 2-28. MMAC sysDSP Element



MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 2-29 shows the MULTADDSUB sysDSP element.

Figure 2-29. MULTADDSUB

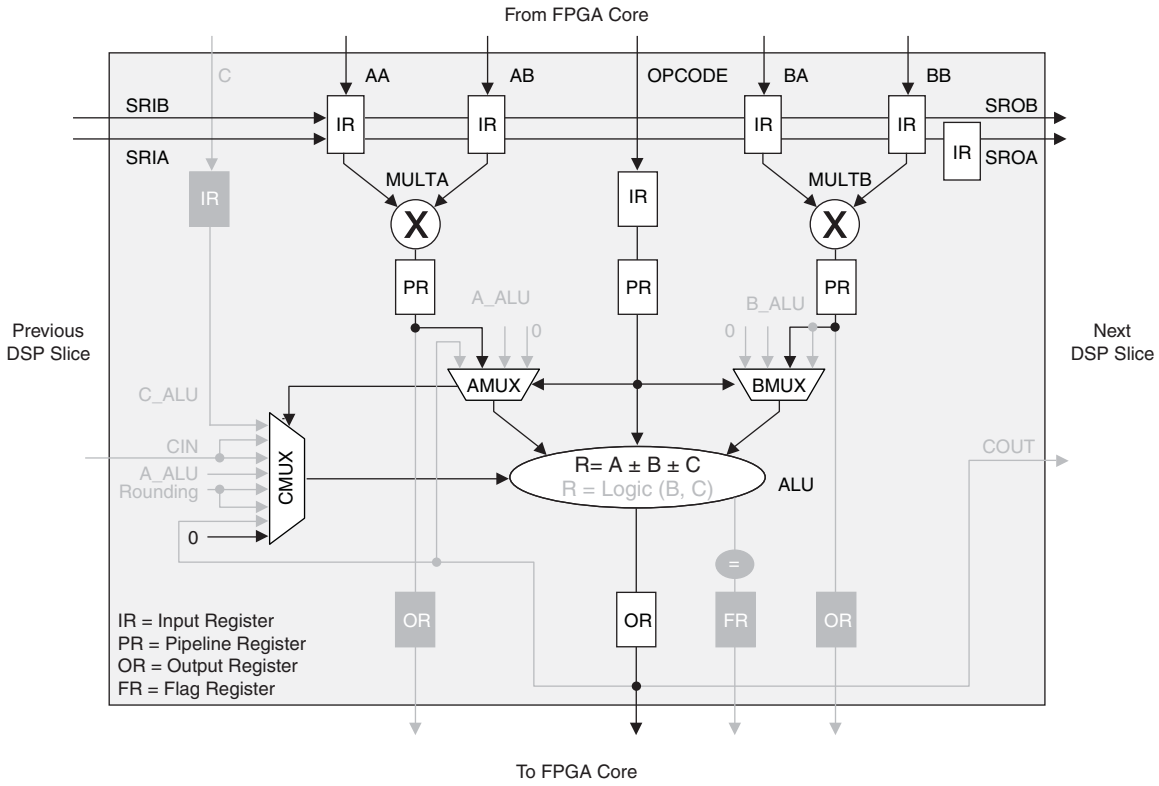
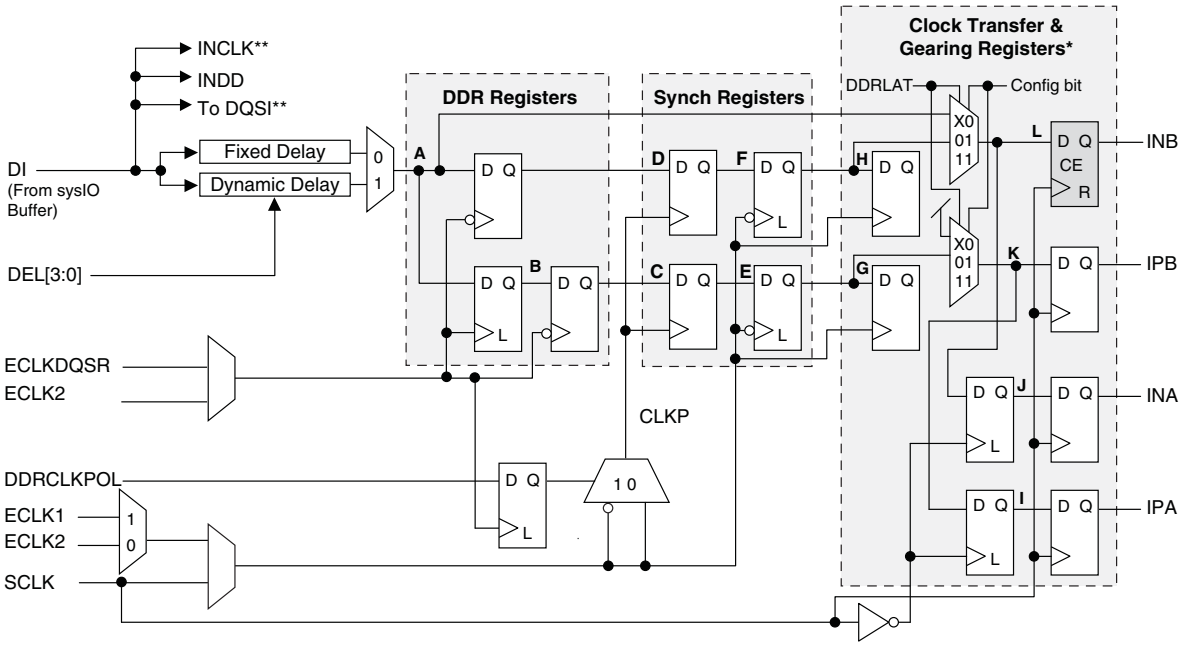


Figure 2-33. Input Register Block for Left, Right and Top Edges



* Only on the left and right sides.
** Selected PIO.
Note: Simplified diagram does not show CE/SET/REST details.

Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDRX2 gearing of output logic. ODDRX2 gearing is used in DDR3 memory interfaces.The PIO blocks on the bottom contain the SDR registers but do not support generic DDR.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 2-35 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

Bottom Edge

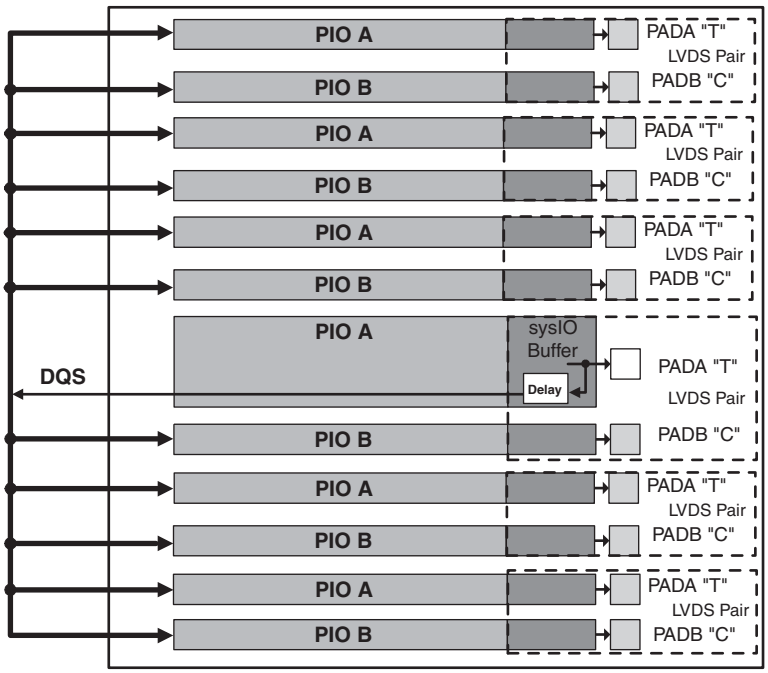
PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

Figure 2-35. DQS Grouping on the Left, Right and Top Edges



2. **Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
   The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

   LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. **Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**
   The sysI/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bi-directional pads to reduce ringing on the receiving end.

Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysI/O Standards

The LatticeECP3 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysI/O buffer to support a variety of standards please see TN1177, LatticeECP3 sysIO Usage Guide.

LatticeECP3 Internal Switching Characteristics[1, 2, 5]

Over Recommended Commercial Operating Conditions

Parameter	Description	–8		–7		–6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.147	—	0.163	—	0.179	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.281	—	0.335	—	0.379	ns
t_{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.593	—	0.674	—	0.756	ns
t_{LSRREC_PFU}	Asynchronous Set/Reset recovery time for PFU Logic		0.298		0.345		0.391	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.134	—	0.144	—	0.153	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	–0.097	—	–0.103	—	–0.109	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.061	—	0.068	—	0.075	—	ns
t_{HD_PFU}	Clock to D input hold time	0.019	—	0.013	—	0.015	—	ns
t_{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.243	—	0.273	—	0.303	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output (F Port)	—	0.710	—	0.803	—	0.897	ns
t_{SUDATA_PFU}	Data Setup Time	–0.137	—	–0.155	—	–0.174	—	ns
t_{HDATA_PFU}	Data Hold Time	0.188	—	0.217	—	0.246	—	ns
t_{SUADDR_PFU}	Address Setup Time	–0.227	—	–0.257	—	–0.286	—	ns
t_{HADDR_PFU}	Address Hold Time	0.240	—	0.275	—	0.310	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	–0.055	—	–0.055	—	–0.063	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.059	—	0.059	—	0.071	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.423	—	0.466	—	0.508	ns
t_{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.241	—	1.301	—	1.361	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.956	—	1.124	—	1.293	—	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	0.225	—	0.184	—	0.240	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay[4]	-	1.09	-	1.16	-	1.23	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	0.220	—	0.185	—	0.150	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	–0.085	—	–0.072	—	–0.058	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.117	—	0.103	—	0.088	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	–0.107	—	–0.094	—	–0.081	—	ns
EBR Timing								
t_{CO_EBR}	Clock (Read) to output from Address or Data	—	2.78	—	2.89	—	2.99	ns
t_{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.31	—	0.32	—	0.33	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	–0.218	—	–0.227	—	–0.237	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.249	—	0.257	—	0.265	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	–0.071	—	–0.070	—	–0.068	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.118	—	0.098	—	0.077	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory	–0.107	—	–0.106	—	–0.106	—	ns

LatticeECP3 Family Timing Adders[1, 2, 3, 4, 5, 7] (Continued)

Over Recommended Commercial Operating Conditions

Buffer Type	Description	–8	–7	–6	Units
RSDS25	RSDS, VCCIO = 2.5 V	–0.07	–0.04	–0.01	ns
PPLVDS	Point-to-Point LVDS, True LVDS, VCCIO = 2.5 V or 3.3 V	–0.22	–0.19	–0.16	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.67	0.76	0.86	ns
HSTL18_I	HSTL_18 class I 8mA drive, VCCIO = 1.8 V	1.20	1.34	1.47	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.89	1.00	1.11	ns
HSTL18D_I	Differential HSTL 18 class I 8 mA drive	1.20	1.34	1.47	ns
HSTL18D_II	Differential HSTL 18 class II	0.89	1.00	1.11	ns
HSTL15_I	HSTL_15 class I 4 mA drive, VCCIO = 1.5 V	1.67	1.83	1.99	ns
HSTL15D_I	Differential HSTL 15 class I 4 mA drive	1.67	1.83	1.99	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	1.12	1.17	1.21	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	1.08	1.12	1.15	ns
SSTL33D_I	Differential SSTL_3 class I	1.12	1.17	1.21	ns
SSTL33D_II	Differential SSTL_3 class II	1.08	1.12	1.15	ns
SSTL25_I	SSTL_2 class I 8 mA drive, VCCIO = 2.5 V	1.06	1.19	1.31	ns
SSTL25_II	SSTL_2 class II 16 mA drive, VCCIO = 2.5 V	1.04	1.17	1.31	ns
SSTL25D_I	Differential SSTL_2 class I 8 mA drive	1.06	1.19	1.31	ns
SSTL25D_II	Differential SSTL_2 class II 16 mA drive	1.04	1.17	1.31	ns
SSTL18_I	SSTL_1.8 class I, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18_II	SSTL_1.8 class II 8 mA drive, VCCIO = 1.8 V	0.70	0.84	0.97	ns
SSTL18D_I	Differential SSTL_1.8 class I	0.70	0.84	0.97	ns
SSTL18D_II	Differential SSTL_1.8 class II 8 mA drive	0.70	0.84	0.97	ns
SSTL15	SSTL_1.5, VCCIO = 1.5 V	1.22	1.35	1.48	ns
SSTL15D	Differential SSTL_15	1.22	1.35	1.48	ns
LVTTL33_4mA	LVTTL 4 mA drive, VCCIO = 3.3V	0.25	0.24	0.23	ns
LVTTL33_8mA	LVTTL 8 mA drive, VCCIO = 3.3V	–0.06	–0.06	–0.07	ns
LVTTL33_12mA	LVTTL 12 mA drive, VCCIO = 3.3V	–0.01	–0.02	–0.02	ns
LVTTL33_16mA	LVTTL 16 mA drive, VCCIO = 3.3V	–0.07	–0.07	–0.08	ns
LVTTL33_20mA	LVTTL 20 mA drive, VCCIO = 3.3V	–0.12	–0.13	–0.14	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive, fast slew rate	0.25	0.24	0.23	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive, fast slew rate	–0.06	–0.06	–0.07	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive, fast slew rate	–0.01	–0.02	–0.02	ns
LVCMOS33_16mA	LVCMOS 3.3 16 mA drive, fast slew rate	–0.07	–0.07	–0.08	ns
LVCMOS33_20mA	LVCMOS 3.3 20 mA drive, fast slew rate	–0.12	–0.13	–0.14	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive, fast slew rate	0.12	0.10	0.09	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive, fast slew rate	–0.05	–0.06	–0.07	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16 mA drive, fast slew rate	–0.12	–0.13	–0.14	ns
LVCMOS25_20mA	LVCMOS 2.5 20 mA drive, fast slew rate	–0.12	–0.13	–0.14	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive, fast slew rate	0.11	0.12	0.14	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive, fast slew rate	–0.04	–0.03	–0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16 mA drive, fast slew rate	–0.04	–0.03	–0.03	ns

SERDES/PCS Block Latency

Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

Table 3-8. SERDES/PCS Latency Breakdown

Item	Description	Min.	Avg.	Max.	Fixed	Bypass	Units
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	word clk
T3	SERDES Bridge transmit	—	—	—	2	1	word clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	word clk
R4	Word alignment	3.1	—	4	—	—	word clk
R5	8b10b decoder	—	—	—	1	—	word clk
R6	Clock Tolerance Compensation	7	15	23	1	1	word clk
R7	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.

Figure 3-12. Transmitter and Receiver Latency Block Diagram

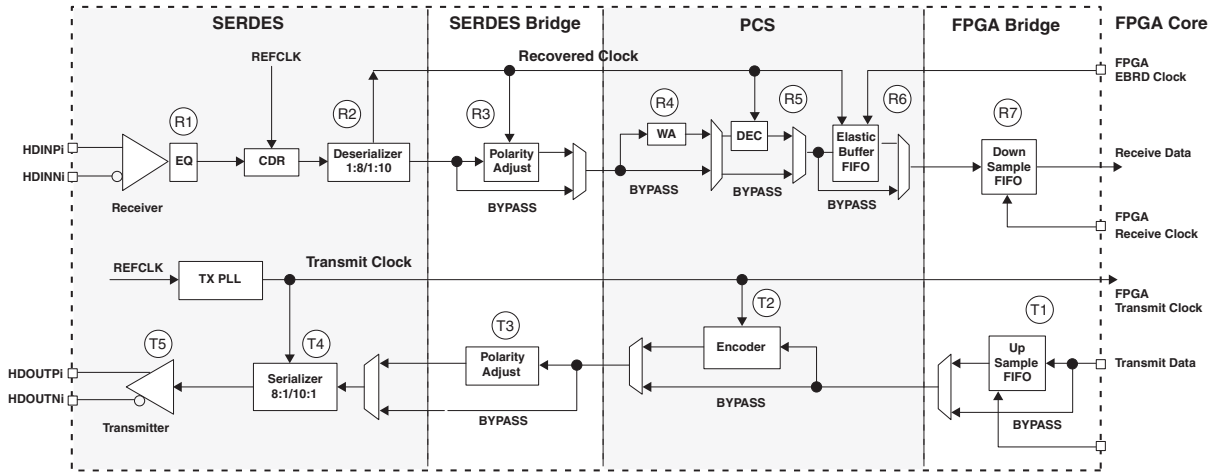
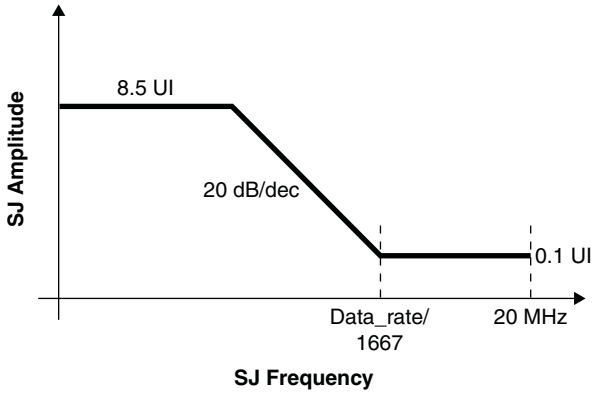


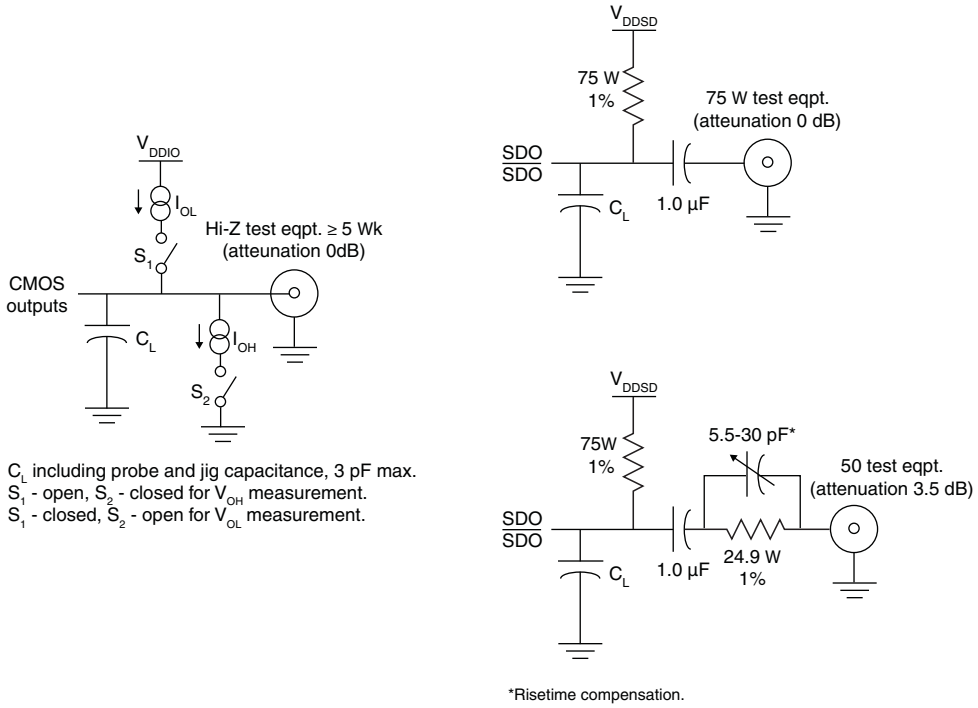
Figure 3-18. XAUI Sinusoidal Jitter Tolerance Mask



Note: The sinusoidal jitter tolerance is measured with at least 0.37 UIpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55 UIpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65 UIpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).

Figure 3-19. Test Loads

Test Loads



C_L including probe and jig capacitance, 3 pF max.
S_1 - open, S_2 - closed for V_{OH} measurement.
S_1 - closed, S_2 - open for V_{OL} measurement.

*Risetime compensation.

Timing Jitter Bandpass

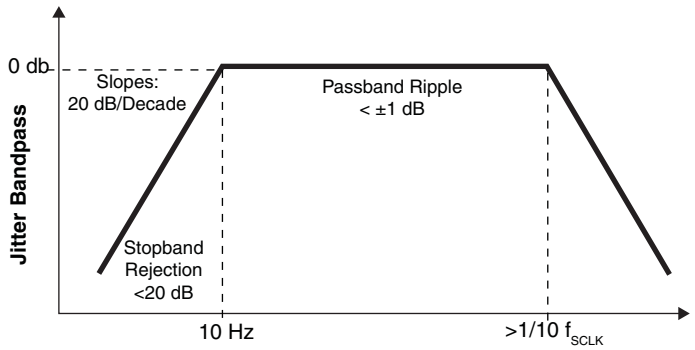
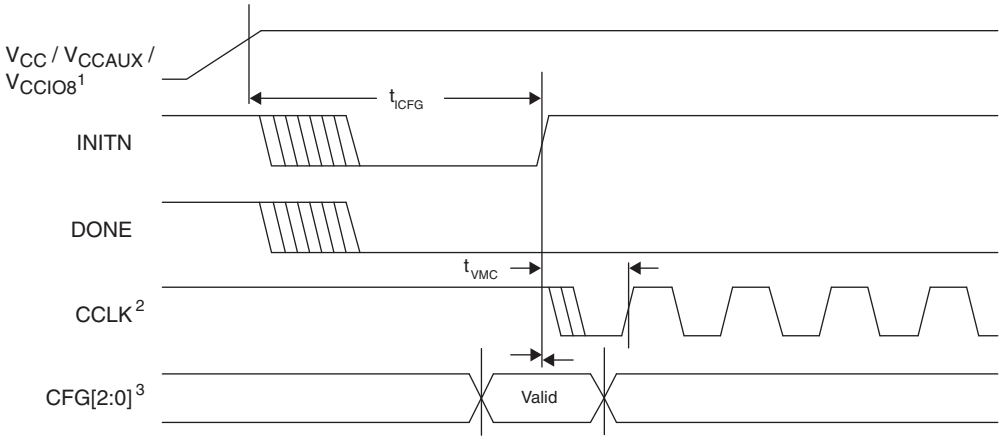
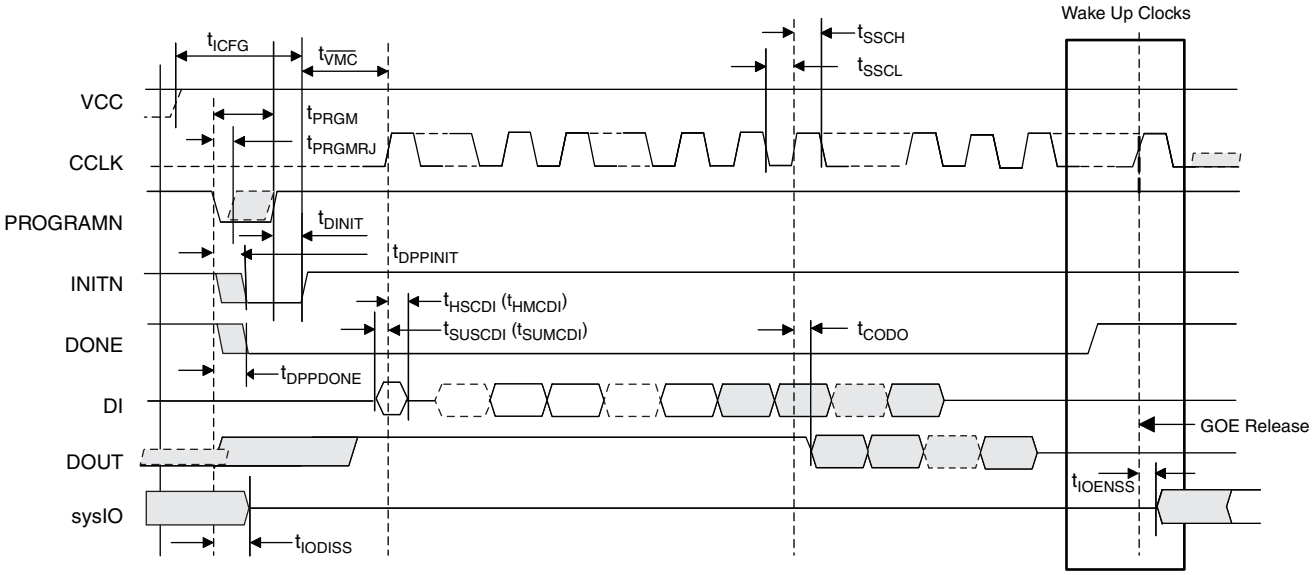


Figure 3-24. Power-On-Reset (POR) Timing



1. Time taken from V_{CC}, V_{CCAUX} or V_{CCIO8}, whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPIm).
3. The CFG pins are normally static (hard wired).

Figure 3-25. sysCONFIG Port Timing



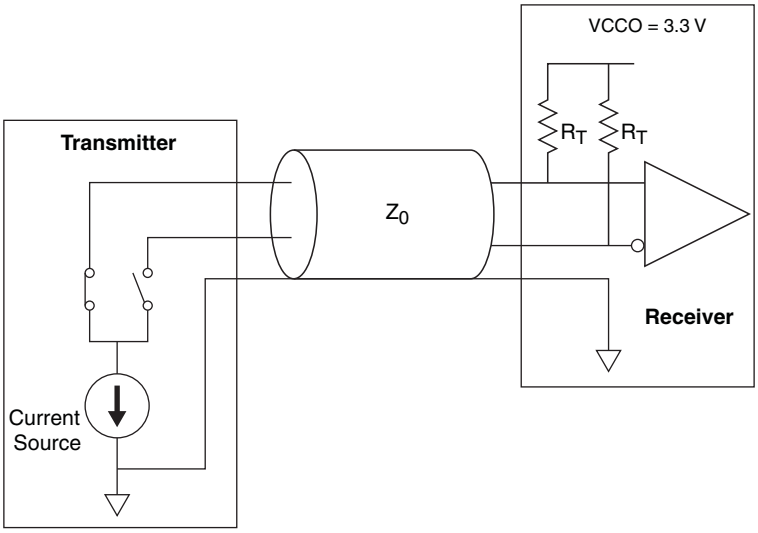
sysI/O Differential Electrical Characteristics

Transition Reduced LVDS (TRLVDS DC Specification)

Over Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units
V_{CCO}	Driver supply voltage (+/– 5%)	3.14	3.3	3.47	V
V_{ID}	Input differential voltage	150	—	1200	mV
V_{ICM}	Input common mode voltage	3	—	3.265	V
V_{CCO}	Termination supply voltage	3.14	3.3	3.47	V
R_T	Termination resistance (off-chip)	45	50	55	Ohms

Note: LatticeECP3 only supports the TRLVDS receiver.



Mini LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	Ohms
R_T	Differential termination resistance	50	100	150	Ohms
V_{OD}	Output voltage, differential, $\|V_{OP} - V_{OM}\|$	300	—	600	mV
V_{OS}	Output voltage, common mode, $\|V_{OP} + V_{OM}\|/2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD}, between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS}, between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $\|V_{INP} - V_{INM}\|$	200	—	600	mV
V_{CM}	Input voltage, common mode, $\|V_{INP} + V_{INM}\|/2$	$0.3+(V_{THD}/2)$	—	$2.1-(V_{THD}/2)$	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	550	ps
T_{ODUTY}	Output clock duty cycle	40	—	60	%

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. It is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. It is a dedicated pin.
CCLK	I	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. It is a dedicated pin.
MCLK	I/O	Output Configuration Clock for configuring an FPGA in SPI, SPIm, and Master configuration modes.
BUSY/SISPI	O	Parallel configuration mode busy indicator. SPI/SPIm mode data output.
CSN/SN/OEN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. Parallel burst Flash output enable.
CS1N/HOLDN/RDY	I	Parallel configuration mode active-low chip select. Slave SPI hold input.
WRITEN	I	Write enable for parallel configuration modes.
DOUT/CSON/CSSPI1N	O	Serial data output. Chip select output. SPI/SPIm mode chip select.
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. Open drain during configuration. sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. Open drain during configuration.
D1	I/O	Parallel configuration I/O. Open drain during configuration.
D2	I/O	Parallel configuration I/O. Open drain during configuration.
D3/SI	I/O	Parallel configuration I/O. Slave SPI data input. Open drain during configuration.
D4/SO	I/O	Parallel configuration I/O. Slave SPI data output. Open drain during configuration.
D5	I/O	Parallel configuration I/O. Open drain during configuration.
D6/SPID1	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-17EA			ECP3-35EA		
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA
Emulated Differential I/O per Bank	Bank 0	13	10	18	13	21	24
	Bank 1	7	5	12	7	18	18
	Bank 2	2	2	4	1	8	8
	Bank 3	4	2	13	5	20	19
	Bank 6	5	1	13	6	22	20
	Bank 7	6	9	10	6	11	13
	Bank 8	12	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	3	3	6	6
	Bank 3	5	4	9	4	9	12
	Bank 6	5	4	9	4	11	12
	Bank 7	5	6	8	5	9	10
	Bank 8	0	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	26/13	20/10	36/18	26/13	42/21	48/24
	Bank 1	14/7	10/5	24/12	14/7	36/18	36/18
	Bank 2	8/4	9/4	14/7	8/4	28/14	28/14
	Bank 3	18/9	12/6	44/22	18/9	58/29	63/31
	Bank 6	20/10	11/5	44/22	20/10	67/33	65/32
	Bank 7	23/11	30/15	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank[2]	Bank 0	2	1	3	2	3	4
	Bank 1	1	0	2	1	3	3
	Bank 2	0	0	1	0	2	2
	Bank 3	1	0	3	1	3	4
	Bank 6	1	0	3	1	4	4
	Bank 7	1	2	2	1	3	3
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	1	1	1	1	1

1. These pins must remain floating on the board.
2. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-70EA		
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43
	Bank 1	18	24	39
	Bank 2	8	12	13
	Bank 3	20	23	33
	Bank 6	22	25	33
	Bank 7	11	16	18
	Bank 8	12	12	12
High-Speed Differential I/O per Bank	Bank 0	0	0	0
	Bank 1	0	0	0
	Bank 2	6	9	9
	Bank 3	9	12	16
	Bank 6	11	14	16
	Bank 7	9	12	13
	Bank 8	0	0	0
Total Single-Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43
	Bank 1	36/18	48/24	78/39
	Bank 2	28/14	42/21	44/22
	Bank 3	58/29	71/35	98/49
	Bank 6	67/33	78/39	98/49
	Bank 7	40/20	56/28	62/31
	Bank 8	24/12	24/12	24/12
DDR Groups Bonded per Bank[1]	Bank 0	3	5	7
	Bank 1	3	4	7
	Bank 2	2	3	3
	Bank 3	3	4	5
	Bank 6	4	4	5
	Bank 7	3	4	4
	Configuration Bank 8	0	0	0
SERDES Quads		1	2	3

1. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-95EA			ECP3-150EA	
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43	30	47
	Bank 1	18	24	39	24	43
	Bank 2	8	12	13	12	18
	Bank 3	20	23	33	23	37
	Bank 6	22	25	33	25	37
	Bank 7	11	16	18	16	24
	Bank 8	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	6	9	9	9	15
	Bank 3	9	12	16	12	21
	Bank 6	11	14	16	14	21
	Bank 7	9	12	13	12	18
	Bank 8	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43	60/30	94/47
	Bank 1	36/18	48/24	78/39	48/24	86/43
	Bank 2	28/14	42/21	44/22	42/21	66/33
	Bank 3	58/29	71/35	98/49	71/35	116/58
	Bank 6	67/33	78/39	98/49	78/39	116/58
	Bank 7	40/20	56/28	62/31	56/28	84/42
	Bank 8	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank	Bank 0	3	5	7	5	7
	Bank 1	3	4	7	4	7
	Bank 2	2	3	3	3	4
	Bank 3	3	4	5	4	7
	Bank 6	4	4	5	4	7
	Bank 7	3	4	4	4	6
	Configuration Bank8	0	0	0	0	0
SERDES Quads		1	2	3	2	4

1.These pins must remain floating on the board.

LatticeECP3 Family Data Sheet Revision History

March 2015 **Data Sheet DS1021**

Date	Version	Section	Change Summary
March 2015	2.8EA	Pinout Information All	Updated Package Pinout Information section. Changed reference to http://www.latticesemi.com/Products/FPGAandCPLD/LatticeECP3.
			Minor style/formatting changes.
April 2014	02.7EA	DC and Switching Characteristics	Updated LatticeECP3 Supply Current (Standby) table power numbers.
			Removed speed grade -9 timing numbers in the following sections: — Typical Building Block Function Performance — LatticeECP3 External Switching Characteristics — LatticeECP3 Internal Switching Characteristics — LatticeECP3 Family Timing Adders
		Ordering Information	Removed ordering information for -9 speed grade devices.
March 2014	02.6EA	DC and Switching Characteristics	Added information to the sysI/O Single-Ended DC Electrical Characteristics section footnote.
February 2014	02.5EA	DC and Switching Characteristics	Updated Hot Socketing Specifications table. Changed I_{PW} to I_{PD} in footnote 3.
			Updated the following figures: — Figure 3-25, sysCONFIG Port Timing — Figure 3-27, Wake-Up Timing
		Supplemental Information	Added technical note references.
September 2013	02.4EA	DC and Switching Characteristics	Updated the Wake-Up Timing Diagram
			Added the following figures: — Master SPI POR Waveforms — SPI Configuration Waveforms — Slave SPI HOLDN Waveforms
			Added tIODISS and tIOENSS parameters in LatticeECP3 sysCONFIG Port Timing Specifications table.
June 2013	02.3EA	Architecture	sysI/O Buffer Banks text section – Updated description of “Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)” for hot socketing information.
			sysI/O Buffer Banks text section – Updated description of “Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)” for PCI clamp information.
			On-Chip Oscillator section – clarified the speed of the internal CMOS oscillator (130 MHz +/- 15%).
			Architecture Overview section – Added information on the state of the register on power up and after configuration.
		DC and Switching Characteristics	sysI/O Recommended Operating Conditions table – Removed reference to footnote 1 from RSDS standard.
			sysI/O Single-Ended DC Electrical Characteristics table – Modified footnote 1.
			Added Oscillator Output Frequency table.
			LatticeECP3 sysCONFIG Port Timing Specifications table – Updated min. column for t_{CODO} parameter.
			LatticeECP3 Family Timing Adders table – Description column, references to VCCIO = 3.0V changed to 3.3V. For PPLVDS, description changed from emulated to True LVDS and VCCIO = 2.5V changed to VCCIO = 2.5V or 3.3V.