E·XFLattice Semiconductor Corporation - <u>LFE3-95EA-8FN672C Datasheet</u>



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-8fn672c

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LatticeECP3 Family Data Sheet Introduction

February 2012

Features

- Higher Logic Density for Increased System Integration
 - 17K to 149K LUTs
 - 116 to 586 I/Os
- Embedded SERDES
 - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
 - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
 - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO

■ sysDSP[™]

- Fully cascadable slice architecture
- 12 to 160 slices for high performance multiply and accumulate
- Powerful 54-bit ALU operations
- Time Division Multiplexing MAC Sharing
- Rounding and truncation
- Each slice supports
 - -Half 36x36, two 18x18 or four 9x9 multipliers
 - Advanced 18x36 MAC and 18x18 Multiply-
 - Multiply-Accumulate (MMAC) operations

■ Flexible Memory Resources

- Up to 6.85Mbits sysMEM[™] Embedded Block RAM (EBR)
- 36K to 303K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs
 Two DLLs and up to ten PLLs per device
- Pre-Engineered Source Synchronous I/O
 - DDR registers in I/O cells

Table 1-1. LatticeECP3™ Family Selection Guide

• Dedicated read/write levelling functionality

Data Sheet DS1021

- Dedicated gearing logic
- Source synchronous standards support
 ADC/DAC, 7:1 LVDS, XGMII
 Link Speed ADC/DAC devices
 - -High Speed ADC/DAC devices
- Dedicated DDR/DDR2/DDR3 memory with DQS support
- Optional Inter-Symbol Interference (ISI) correction on outputs
- Programmable sysl/O[™] Buffer Supports Wide Range of Interfaces
 - On-chip termination
 - Optional equalization filter on inputs
 - LVTTL and LVCMOS 33/25/18/15/12
 - SSTL 33/25/18/15 I, II
 - HSTL15 I and HSTL18 I, II
 - PCI and Differential HSTL, SSTL
 - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS

Flexible Device Configuration

- Dedicated bank for configuration I/Os
- SPI boot flash interface
- Dual-boot images supported
- Slave SPI
- TransFR™ I/O for simple field updates
- Soft Error Detect embedded macro

System Level Support

- IEEE 1149.1 and IEEE 1532 compliant
- Reveal Logic Analyzer
- ORCAstra FPGA configuration utility
- · On-chip oscillator for initialization & general use
- 1.2 V core power supply

Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18 Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18 x 18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2/2	4/2	10/2	10 / 2	10/2
Packages and SERDES Channels	/ I/O Combinatio	ns		•	
328 csBGA (10 x 10 mm)	2/116				
256 ftBGA (17 x 17 mm)	4 / 133	4 / 133			
484 fpBGA (23 x 23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27 x 27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35 x 35 mm)			12 / 490	12 / 490	16 / 586

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Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices.

PFU Blocks

The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.



Figure 2-4. General Purpose PLL Diagram



Table 2-4 provides a description of the signals in the PLL blocks.

Table 2-4. PLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	0	PLL output to clock tree (phase shifted/duty cycle changed)
CLKOP	0	PLL output to clock tree (no phase shift)
CLKOK	0	PLL output to clock tree through secondary clock divider
CLKOK2	0	PLL output to clock tree (CLKOP divided by 3)
LOCK	0	"1" indicates PLL LOCK to CLKI
FDA [3:0]	I	Dynamic fine delay adjustment on CLKOS output
DRPAI[3:0]	I	Dynamic coarse phase shift, rising edge setting
DFPAI[3:0]	I	Dynamic coarse phase shift, falling edge setting

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP3 family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay



PLL/DLL Cascading

LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

The DLLs in the LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

PLL/DLL PIO Input Pin Connections

All LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 2-7.

Figure 2-7. Sharing of PIO Pins by PLLs and DLLs in LatticeECP3 Devices



Note: Not every PLL has an associated DLL.

Clock Dividers

LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide. Figure 2-8 shows the clock divider connections.



DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.



On-Chip Programmable Termination

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 40, 50, or 60 Ohms. External termination to Vtt should be used for DDR2 and DDR3 memory controller implementation.
- Common mode termination of 80, 100, 120 Ohms for differential inputs

Figure 2-39. On-Chip Termination



Programmable resistance (40, 50 and 60 Ohms)
Parallel Single-Ended Input

Differential Input

See Table 2-12 for termination options for input modes.

Table 2-12. On-Chip Termination Options for Input Modes

IO_TYPE	TERMINATE to VTT ^{1, 2}	DIFFERENTIAL TERMINATION RESISTOR ¹
LVDS25	þ	80, 100, 120
BLVDS25	þ	80, 100, 120
MLVDS	þ	80, 100, 120
HSTL18_I	40, 50, 60	þ
HSTL18_II	40, 50, 60	þ
HSTL18D_I	40, 50, 60	þ
HSTL18D_II	40, 50, 60	þ
HSTL15_I	40, 50, 60	þ
HSTL15D_I	40, 50, 60	þ
SSTL25_I	40, 50, 60	þ
SSTL25_II	40, 50, 60	þ
SSTL25D_I	40, 50, 60	þ
SSTL25D_II	40, 50, 60	þ
SSTL18_I	40, 50, 60	þ
SSTL18_II	40, 50, 60	þ
SSTL18D_I	40, 50, 60	þ
SSTL18D_II	40, 50, 60	þ
SSTL15	40, 50, 60	þ
SSTL15D	40, 50, 60	þ

1. TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature. Use of TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in

an I/O bank.

On-chip termination tolerance +/- 20%

2. External termination to VTT should be used when implementing DDR2 and DDR3 memory controller.



Enhanced Configuration Options

LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dualboot image support.

1. TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

2. Dual-Boot Image Support

Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP3 can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP3 device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Soft Error Detect (SED) Support

LatticeECP3 devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LatticeECP3 device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide.

External Resistor

LatticeECP3 devices require a single external, 10 kOhm \pm 1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCCLK) for configuration. The oscillator and the MCCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCCLK is nominally 2.5 MHz. Table 2-16 lists all the available MCCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

- 1. Device powers up with a nominal Master Clock frequency of 3.1 MHz.
- 2. During configuration, users select a different master clock frequency.
- 3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
- 4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCCLK frequency of 2.5 MHz.

This internal 130 MHz +/- 15% CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

			_	-8		-7		-6	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{DVECLKGDDR}	Data Hold After CLK	All ECP3EA Devices	0.775		0.775	—	0.775		UI
f _{MAX_GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices		250		250		250	MHz
Generic DDRX2 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Pin for Clock Input									
Left and Right Sic	les								
t _{SUGDDR}	Data Setup Before CLK	ECP3-150EA	321		403		471		ps
t _{HOGDDR}	Data Hold After CLK	ECP3-150EA	321		403	_	471		ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	_	405	—	325	_	280	MHz
t _{SUGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	321	_	403	—	535	—	ps
t _{HOGDDR}	Data Hold After CLK	ECP3-70EA/95EA	321	_	403	_	535		ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	_	405		325		250	MHz
t _{SUGDDR}	Data Setup Before CLK	ECP3-35EA	335	_	425	_	535	—	ps
t _{HOGDDR}	Data Hold After CLK	ECP3-35EA	335	—	425	_	535	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	_	405	_	325	_	250	MHz
t _{SUGDDR}	Data Setup Before CLK	ECP3-17EA	335	_	425	—	535	—	ps
t _{HOGDDR}	Data Hold After CLK	ECP3-17EA	335	_	425	_	535		ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	_	405		325		250	MHz
Generic DDRX2 Ir	puts with Clock and Data (>10	Bits Wide) Aligned at Pin	(GDDR)	(2_RX.E	CLK.Alig	ned)			
Left and Right Sid	le Using DLLCLKIN Pin for Clo	ck Input							
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-150EA	—	0.225	_	0.225	_	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775		0.775		0.775		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	_	460	—	385	—	345	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-70EA/95EA		0.225		0.225		0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775		0.775	_	0.775		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA		460		385		311	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	_	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790		0.790	—	0.790	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	_	460		385		311	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-17EA	—	0.210	—	0.210	—	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790	—	0.790	—	0.790	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA	_	460	_	385	_	311	MHz
Top Side Using P	CLK Pin for Clock Input								
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-150EA	_	0.225	—	0.225	_	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-150EA	0.775	—	0.775		0.775	—	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	_	235	_	170	_	130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-70EA/95EA	_	0.225	_	0.225	_	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-70EA/95EA	0.775	_	0.775	—	0.775	_	UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-70EA/95EA	—	235	—	170	—	130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-35EA	—	0.210	—	0.210	_	0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-35EA	0.790		0.790	_	0.790		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-35EA	_	235		170	_	130	MHz
t _{DVACLKGDDR}	Data Setup Before CLK	ECP3-17EA	—	0.210		0.210		0.210	UI
t _{DVECLKGDDR}	Data Hold After CLK	ECP3-17EA	0.790		0.790	_	0.790		UI
f _{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-17EA		235		170		130	MHz

Over Recommended Commercial Operating Conditions



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

							6		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
f _{MAX GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250		250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-35EA	683	_	688		690	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	683	—	688	—	690	_	ps
f _{MAX GDDR}	DDRX1 Clock Frequency	ECP3-35EA	—	250	_	250	_	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	683	_	688		690		ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	683	—	688	—	690	_	ps
f _{MAX GDDR}	DDRX1 Clock Frequency	ECP3-17EA	—	250	_	250	_	250	MHz
Generic DDRX1 Ou	tput with Clock and Data Aligne	d at Pin (GDDRX1_TX.	SCLK.Ali	gned) ¹⁰					
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-150EA	—	335	—	338	—	341	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-150EA	—	335	—	338		341	ps
f _{MAX} GDDR	DDRX1 Clock Frequency	ECP3-150EA	_	250	_	250		250	MHz
	Data Invalid Before Clock	ECP3-70EA/95EA	_	339	_	343		347	ps
t _{DIAGDDB}	Data Invalid After Clock	ECP3-70EA/95EA	_	339	_	343		347	ps
f _{MAX} GDDR	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250		250	MHz
	Data Invalid Before Clock	ECP3-35EA		322		320		321	ps
	Data Invalid After Clock	ECP3-35EA	_	322	_	320		321	ps
f _{MAX GDDB}	DDRX1 Clock Frequency	ECP3-35EA	_	250	_	250		250	MHz
	Data Invalid Before Clock	ECP3-17EA		322		320		321	ps
tDIAGDDR	Data Invalid After Clock	ECP3-17EA	_	322	_	320		321	ps
f _{MAX GDDB}	DDRX1 Clock Frequency	ECP3-17EA	_	250	_	250		250	MHz
Generic DDRX1 Ou	Itput with Clock and Data (<10 B	its Wide) Centered at F	in (GDD	RX1_TX.	DQS.Cen	tered) ¹⁰			
Left and Right Side	25		-			-			
t _{DVBGDDR}	Data Valid Before CLK	ECP3-150EA	670		670		670	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-150EA	670	_	670	_	670	_	ps
f _{MAX GDDB}	DDRX1 Clock Frequency	ECP3-150EA	_	250	_	250	_	250	MHz
	Data Valid Before CLK	ECP3-70EA/95EA	657		652		650	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-70EA/95EA	657	_	652		650	_	ps
f _{MAX GDDB}	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250	_	250	MHz
	Data Valid Before CLK	ECP3-35EA	670		675		676	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	670	—	675	—	676	_	ps
f _{MAX GDDR}	DDRX1 Clock Frequency	ECP3-35EA	—	250	—	250	_	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	670	—	670	—	670	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	670	_	670	_	670	_	ps
f _{MAX} GDDR	DDRX1 Clock Frequency	ECP3-17EA	_	250	_	250		250	MHz
Generic DDRX2 Ou	tput with Clock and Data (>10 B	its Wide) Aligned at Pi	n (GDDR	X2_TX.A	ligned)				
Left and Right Side	es								
t _{DIBGDDR}	Data Invalid Before Clock	All ECP3EA Devices	—	200	—	210	_	220	ps
t _{DIAGDDR}	Data Invalid After Clock	All ECP3EA Devices	—	200	—	210	—	220	ps
f _{MAX GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	500	_	420	_	375	MHz
Generic DDRX2 Ou	tput with Clock and Data (>10 B	its Wide) Centered at P	in Using	DQSDL	L (GDDF	X2_TX.C	QSDLL.	Centered)11
Left and Right Side	S								
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	400		400		431	_	ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	400	—	400	—	432	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	—	400	—	400	—	375	MHz

Over Recommended Commercial Operating Conditions







Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.



LatticeECP3 Family Timing Adders^{1, 2, 3, 4, 5, 7}

Buffer Type	Description	-8	-7	-6	Units
Input Adjusters					
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	0.03	-0.01	-0.03	ns
LVDS25	LVDS, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	0.03	0.00	-0.04	ns
RSDS25	RSDS, VCCIO = 2.5 V	0.03	-0.01	-0.03	ns
PPLVDS	Point-to-Point LVDS	0.03	-0.01	-0.03	ns
TRLVDS	Transition-Reduced LVDS	0.03	0.00	-0.04	ns
Mini MLVDS	Mini LVDS	0.03	-0.01	-0.03	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.3 V	0.17	0.23	0.28	ns
HSTL18_I	HSTL_18 class I, VCCIO = 1.8 V	0.20	0.17	0.13	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.20	0.17	0.13	ns
HSTL18D_I	Differential HSTL 18 class I	0.20	0.17	0.13	ns
HSTL18D_II	Differential HSTL 18 class II	0.20	0.17	0.13	ns
HSTL15_I	HSTL_15 class I, VCCIO = 1.5 V	0.10	0.12	0.13	ns
HSTL15D_I	Differential HSTL 15 class I	0.10	0.12	0.13	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.3 V	0.17	0.23	0.28	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.3 V	0.17	0.23	0.28	ns
SSTL33D_I	Differential SSTL_3 class I	0.17	0.23	0.28	ns
SSTL33D_II	Differential SSTL_3 class II	0.17	0.23	0.28	ns
SSTL25_I	SSTL_2 class I, VCCIO = 2.5 V	0.12	0.14	0.16	ns
SSTL25_II	SSTL_2 class II, VCCIO = 2.5 V	0.12	0.14	0.16	ns
SSTL25D_I	Differential SSTL_2 class I	0.12	0.14	0.16	ns
SSTL25D_II	Differential SSTL_2 class II	0.12	0.14	0.16	ns
SSTL18_I	SSTL_18 class I, VCCIO = 1.8 V	0.08	0.06	0.04	ns
SSTL18_II	SSTL_18 class II, VCCIO = 1.8 V	0.08	0.06	0.04	ns
SSTL18D_I	Differential SSTL_18 class I	0.08	0.06	0.04	ns
SSTL18D_II	Differential SSTL_18 class II	0.08	0.06	0.04	ns
SSTL15	SSTL_15, VCCIO = 1.5 V	0.087	0.059	0.032	ns
SSTL15D	Differential SSTL_15	0.087	0.059	0.032	ns
LVTTL33	LVTTL, VCCIO = 3.3 V	0.07	0.07	0.07	ns
LVCMOS33	LVCMOS, VCCIO = 3.3 V	0.07	0.07	0.07	ns
LVCMOS25	LVCMOS, VCCIO = 2.5 V	0.00	0.00	0.00	ns
LVCMOS18	LVCMOS, VCCIO = 1.8 V	-0.13	-0.13	-0.13	ns
LVCMOS15	LVCMOS, VCCIO = 1.5 V	-0.07	-0.07	-0.07	ns
LVCMOS12	LVCMOS, VCCIO = 1.2 V	-0.20	-0.19	-0.19	ns
PCI33	PCI, VCCIO = 3.3 V	0.07	0.07	0.07	ns
Output Adjusters					
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	1.02	1.14	1.26	ns
LVDS25	LVDS, VCCIO = 2.5 V	-0.11	-0.07	-0.03	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	1.01	1.13	1.25	ns

Over Recommended Commercial Operating Conditions



DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Condition	Min.	Тур.	Max.	Units
f _{REF}	Input reference clock frequency (on-chip or off-chip)		133	—	500	MHz
f _{FB}	Feedback clock frequency (on-chip or off-chip)		133	—	500	MHz
f _{CLKOP} ¹	Output clock frequency, CLKOP		133	—	500	MHz
f _{CLKOS²}	Output clock frequency, CLKOS		33.3	—	500	MHz
t _{PJIT}	Output clock period jitter (clean input)			—	200	ps p-p
	Output clock duty cycle (at 50% levels, 50% duty	Edge Clock	40		60	%
t _{DUTY} cycle input clock, 50% duty cycle circuit turned off, time reference delay mode)		Primary Clock	30		70	%
	Output clock duty cycle (at 50% levels, arbitrary	Primary Clock < 250 MHz	45		55	%
t _{dutytrd}	duty cycle input clock, 50% duty cycle circuit	Primary Clock ≥ 250 MHz	30		70	%
	enabled, time reference delay mode)	Edge Clock	45		55	%
	Output clock duty cycle (at 50% levels, arbitrary	Primary Clock < 250 MHz	40		60	%
t _{DUTYCIR}	duty cycle input clock, 50% duty cycle circuit	Primary Clock ≥ 250 MHz	30		70	%
	cascading	val mode) with DLL Edge Clock	45		55	%
t _{SKEW} ³	Output clock to clock skew between two outputs with the same phase setting		_	—	100	ps
t _{PHASE}	Phase error measured at device pads between off-chip reference clock and feedback clocks		_	—	+/-400	ps
t _{PWH}	Input clock minimum pulse width high (at 80% level)		550	_	_	ps
t _{PWL}	Input clock minimum pulse width low (at 20% level)		550	—	_	ps
t _{INSTB}	Input clock period jitter			—	500	ps
t _{LOCK}	DLL lock time		8	—	8200	cycles
t _{RSWD}	Digital reset minimum pulse width (at 80% level)		3	—	—	ns
t _{DEL}	Delay step size		27	45	70	ps
t _{RANGE1}	Max. delay setting for single delay block (64 taps)		1.9	3.1	4.4	ns
t _{RANGE4}	Max. delay setting for four chained delay blocks		7.6	12.4	17.6	ns

1. CLKOP runs at the same frequency as the input clock.

2. CLKOS minimum frequency is obtained with divide by 4.

3. This is intended to be a "path-matching" design guideline and is not a measurable specification.



SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Symbol	Description	Min.	Тур.	Max.	Units
F _{REF}	Frequency range	15	_	320	MHz
F _{REF-PPM}	Frequency tolerance ¹	-1000	_	1000	ppm
V _{REF-IN-SE}	Input swing, single-ended clock ²	200	_	V _{CCA}	mV, p-p
V _{REF-IN-DIFF}	Input swing, differential clock	200	_	2*V _{CCA}	mV, p-p differential
V _{REF-IN}	Input levels	0	_	V _{CCA} + 0.3	V
D _{REF}	Duty cycle ³	40	_	60	%
T _{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T _{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
Z _{REF-IN-TERM-DIFF}	Differential input termination	-20%	100/2K	+20%	Ohms
C _{REF-IN-CAP}	Input capacitance	_	—	7	pF

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.

2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.

3. Measured at 50% amplitude.

Figure 3-13. SERDES External Reference Clock Waveforms





HDMI (High-Definition Multimedia Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-22. Transmit and Receive^{1, 2}

		Spec. Co		
Symbol	Description	Min. Spec.	Max. Spec.	Units
Transmit		•		
Intra-pair Skew		—	75	ps
Inter-pair Skew		—	800	ps
TMDS Differential Clock Jitter		—	0.25	UI
Receive		•		
R _T	Termination Resistance	40	60	Ohms
V _{ICM}	Input AC Common Mode Voltage (50-Ohm Set- ting)	—	50	mV
TMDS Clock Jitter	Clock Jitter Tolerance	—	0.25	UI

1. Output buffers must drive a translation device. Max. speed is 2 Gbps. If translation device does not modify rise/fall time, the maximum speed is 1.5 Gbps.

2. Input buffers must be AC coupled in order to support the 3.3 V common mode. Generally, HDMI inputs are terminated by an external cable equalizer before data/clock is forwarded to the LatticeECP3 device.



Figure 3-19. Test Loads

Test Loads



















Signal Descriptions (Cont.)

Signal Name	I/O	Description
D7/SPID0	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configura- tion.
DI/CSSPI0N/CEN	I/O	Serial data input for slave serial mode. SPI/SPIm mode chip select.
Dedicated SERDES Signals ³		
PCS[Index]_HDINNm	I	High-speed input, negative channel m
PCS[Index]_HDOUTNm	0	High-speed output, negative channel m
PCS[Index]_REFCLKN	I	Negative Reference Clock Input
PCS[Index]_HDINPm	I	High-speed input, positive channel m
PCS[Index]_HDOUTPm	0	High-speed output, positive channel m
PCS[Index]_REFCLKP	I	Positive Reference Clock Input
PCS[Index]_VCCOBm		Output buffer power supply, channel m (1.2V/1.5)
PCS[Index]_VCCIBm		Input buffer power supply, channel m (1.2V/1.5V)

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.

2. These pins are dedicated inputs or can be used as general purpose I/O.

3. m defines the associated channel in the quad.



LatticeECP3 Family Data Sheet Ordering Information

April 2014

Data Sheet DS1021

LatticeECP3 Part Number Description



1. Green = Halogen free and lead free.

Ordering Information

LatticeECP3 devices have top-side markings, for commercial and industrial grades, as shown below:



Note: See PCN 05A-12 for information regarding a change to the top-side mark logo.

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LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6MG328C	1.2 V	-6	STD	Green csBGA	328	COM	17
LFE3-17EA-7MG328C	1.2 V	-7	STD	Green csBGA	328	COM	17
LFE3-17EA-8MG328C	1.2 V	-8	STD	Green csBGA	328	COM	17
LFE3-17EA-6LMG328C	1.2 V	-6	LOW	Green csBGA	328	COM	17
LFE3-17EA-7LMG328C	1.2 V	-7	LOW	Green csBGA	328	COM	17
LFE3-17EA-8LMG328C	1.2 V	-8	LOW	Green csBGA	328	COM	17
LFE3-17EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	17
LFE3-17EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	17

Commercial

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256C	1.2 V	-6	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7FTN256C	1.2 V	-7	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8FTN256C	1.2 V	-8	STD	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6LFTN256C	1.2 V	-6	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7LFTN256C	1.2 V	-7	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8LFTN256C	1.2 V	-8	LOW	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	33
LFE3-35EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.



Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672CTW ¹	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672CTW ¹	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672CTW ¹	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156CTW1	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156CTW ¹	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156CTW1	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	149

1. Note: Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

• The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.

• The SERDES XRES pin on the TW device passes CDM testing at 250 V.