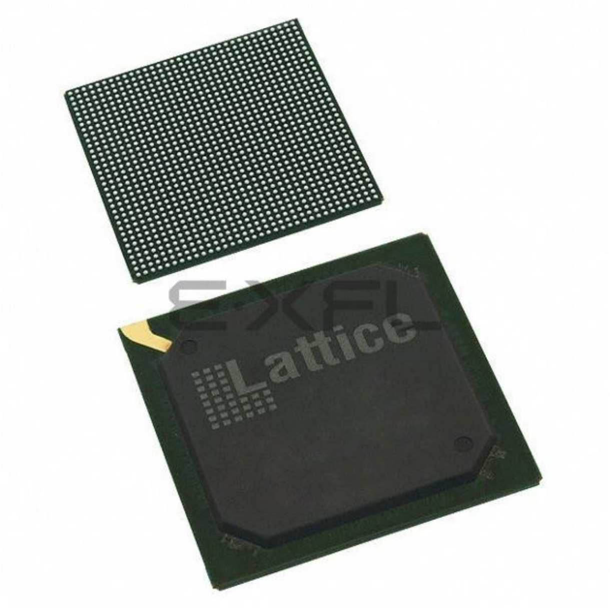

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 11500 |
| Number of Logic Elements/Cells | 92000 |
| Total RAM Bits | 4526080 |
| Number of I/O | 490 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1156-BBGA |
| Supplier Device Package | 1156-FPBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-8lfn1156c |

# LatticeECP3 Family Data Sheet Introduction

February 2012 | Data Sheet DS1021

## Features

- **Higher Logic Density for Increased System Integration**
  - 17K to 149K LUTs
  - 116 to 586 I/Os
- **Embedded SERDES**
  - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
  - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
  - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO
- **sysDSP™**
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36x36, two 18x18 or four 9x9 multipliers
    - Advanced 18x36 MAC and 18x18 Multiply-Multiply-Accumulate (MMAC) operations
- **Flexible Memory Resources**
  - Up to 6.85Mbits sysMEM™ Embedded Block RAM (EBR)
  - 36K to 303K bits distributed RAM
- **sysCLOCK Analog PLLs and DLLs**
  - Two DLLs and up to ten PLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR/DDR2/DDR3 memory with DQS support
  - Optional Inter-Symbol Interference (ISI) correction on outputs
- **Programmable sysI/O™ Buffer Supports Wide Range of Interfaces**
  - On-chip termination
  - Optional equalization filter on inputs
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 33/25/18/15 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
- **Flexible Device Configuration**
  - Dedicated bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
  - Soft Error Detect embedded macro
- **System Level Support**
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - ORCAstra FPGA configuration utility
  - On-chip oscillator for initialization & general use
  - 1.2 V core power supply

*Table 1-1. LatticeECP3™ Family Selection Guide*

| Device | ECP3-17 | ECP3-35 | ECP3-70 | ECP3-95 | ECP3-150 |
|---|---|---|---|---|---|
| LUTs (K) | 17 | 33 | 67 | 92 | 149 |
| sysMEM Blocks (18 Kbits) | 38 | 72 | 240 | 240 | 372 |
| Embedded Memory (Kbits) | 700 | 1327 | 4420 | 4420 | 6850 |
| Distributed RAM Bits (Kbits) | 36 | 68 | 145 | 188 | 303 |
| 18 x 18 Multipliers | 24 | 64 | 128 | 128 | 320 |
| SERDES (Quad) | 1 | 1 | 3 | 3 | 4 |
| PLLs/DLLs | 2 / 2 | 4 / 2 | 10 / 2 | 10 / 2 | 10 / 2 |
| **Packages and SERDES Channels/ I/O Combinations** | | | | | |
| 328 csBGA (10 x 10 mm) | 2 / 116 | | | | |
| 256 ftBGA (17 x 17 mm) | 4 / 133 | 4 / 133 | | | |
| 484 fpBGA (23 x 23 mm) | 4 / 222 | 4 / 295 | 4 / 295 | 4 / 295 | |
| 672 fpBGA (27 x 27 mm) | | 4 / 310 | 8 / 380 | 8 / 380 | 8 / 380 |
| 1156 fpBGA (35 x 35 mm) | | | 12 / 490 | 12 / 490 | 16 / 586 |

***Figure 2-4. General Purpose PLL Diagram***

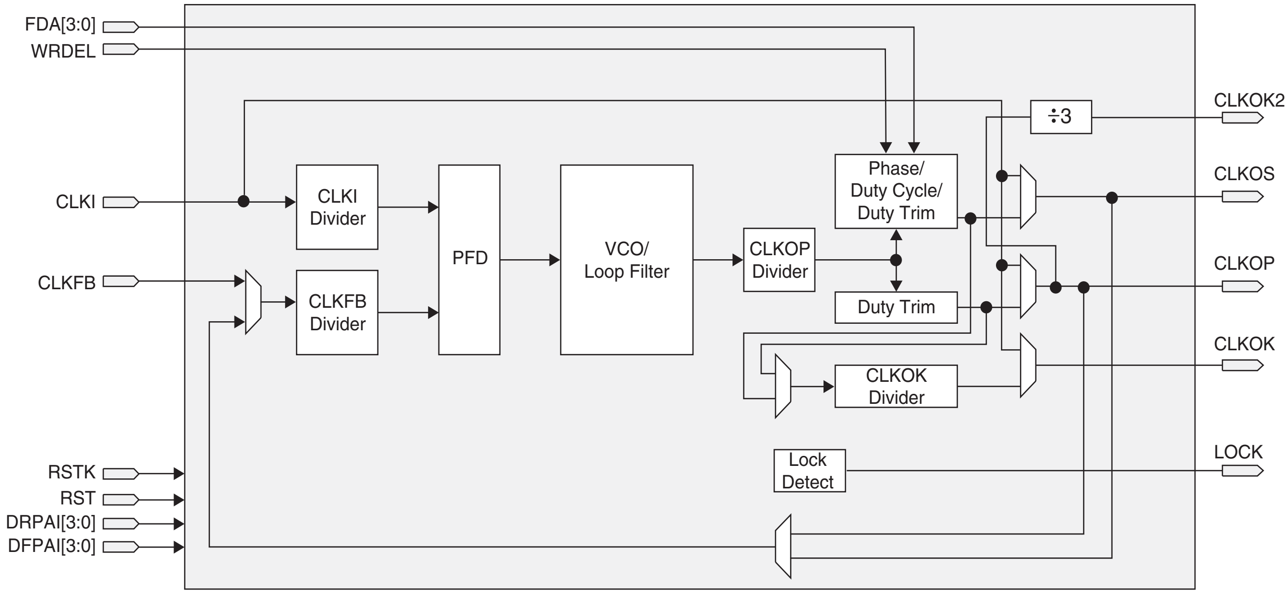



Table 2-4 provides a description of the signals in the PLL blocks.

***Table 2-4. PLL Blocks Signal Descriptions***

| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic) |
| RST | I | “1” to reset PLL counters, VCO, charge pumps and M-dividers |
| RSTK | I | “1” to reset K-divider |
| WRDEL | I | DPA Fine Delay Adjust input |
| CLKOS | O | PLL output to clock tree (phase shifted/duty cycle changed) |
| CLKOP | O | PLL output to clock tree (no phase shift) |
| CLKOK | O | PLL output to clock tree through secondary clock divider |
| CLKOK2 | O | PLL output to clock tree (CLKOP divided by 3) |
| LOCK | O | “1” indicates PLL LOCK to CLKI |
| FDA [3:0] | I | Dynamic fine delay adjustment on CLKOS output |
| DRPAI[3:0] | I | Dynamic coarse phase shift, rising edge setting |
| DFPAI[3:0] | I | Dynamic coarse phase shift, falling edge setting |

## Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP3 family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

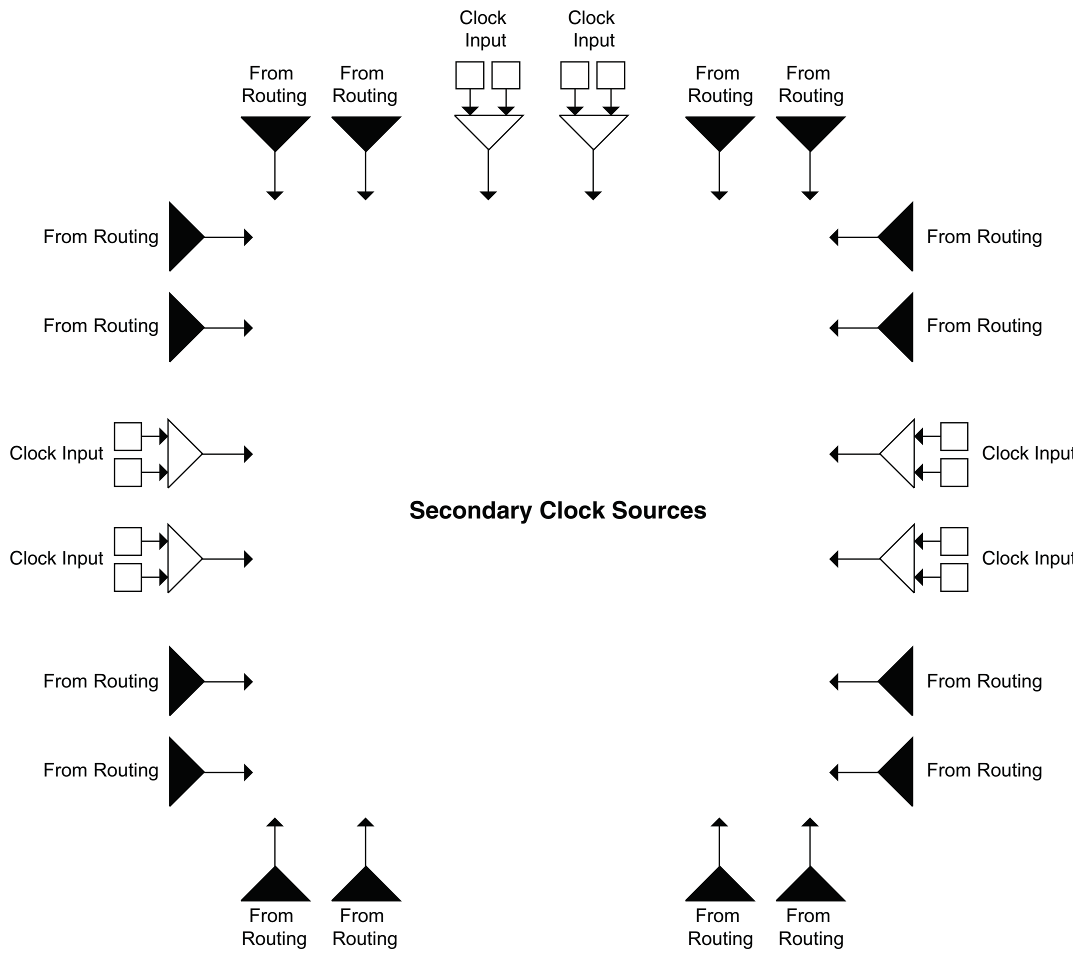
The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay

## Secondary Clock/Control Sources

LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-14 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for the clock.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7.

***Figure 2-14. Secondary Clock Sources***




Note: Clock inputs can be configured in differential or single-ended mode.

## Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-15 shows this special vertical routing channel and the 20 secondary clock regions for the LatticeECP3 family of devices. All devices in the LatticeECP3 family have eight secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.

## Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

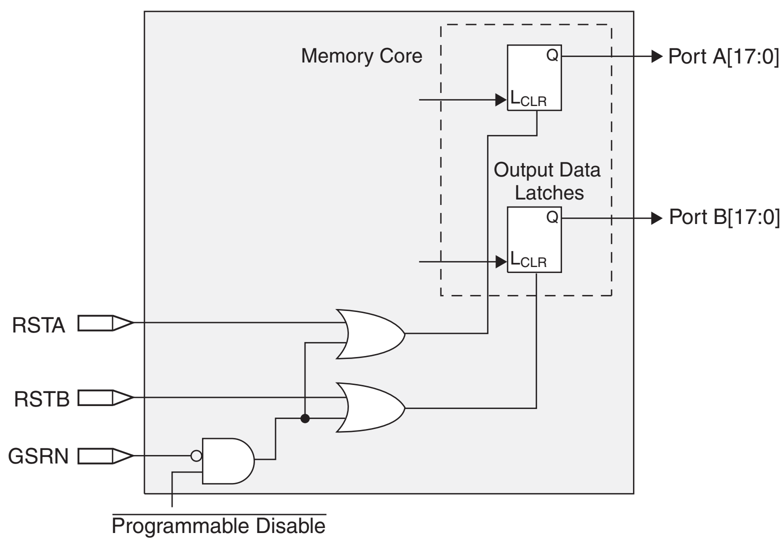
EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

## Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

***Figure 2-22. Memory Core Reset***




For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

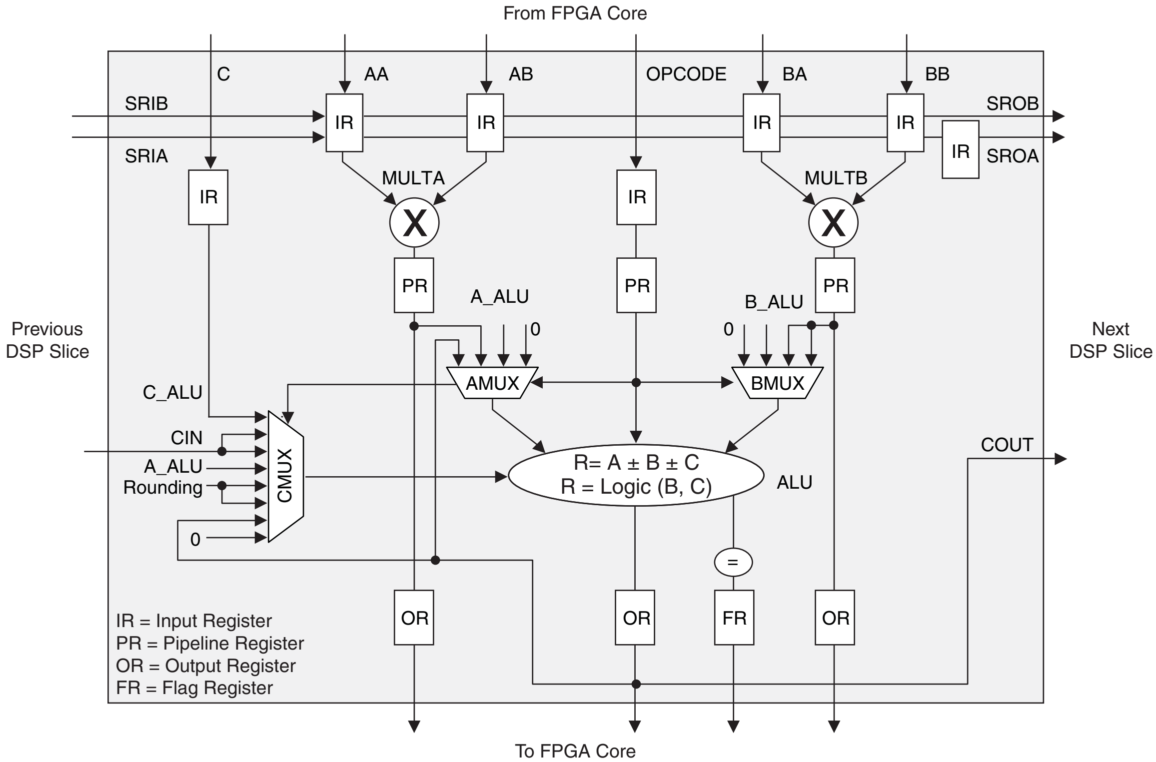
# sysDSP™ Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

## sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.

*Figure 2-25. Detailed sysDSP Slice Diagram*




Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LatticeECP3 slices versus the above functions.

*Table 2-8. Maximum Number of Elements in a Slice*

| Width of Multiply | x9 | x18 | x36 |
|---|---|---|---|
| MULT | 4 | 2 | 1/2 |
| MAC | 1 | 1 | — |
| MULTADDSUB | 2 | 1 | — |
| MULTADDSUBSUM | 1[1] | 1/2 | — |

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

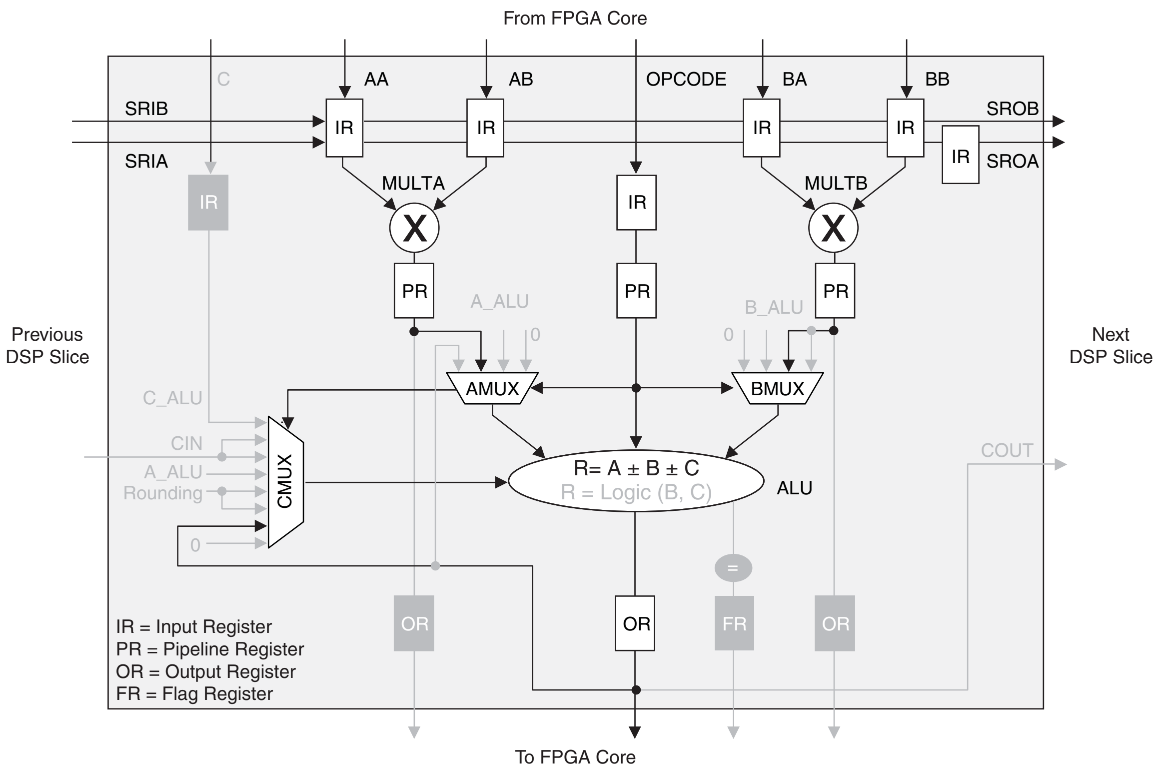
Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting "dynamic operation" the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

## MMAC DSP Element

The LatticeECP3 supports a MAC with two multipliers. This is called Multiply Multiply Accumulate or MMAC. In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value and with the result of the multiplier operation of operands BA and BB. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-28 shows the MMAC sysDSP element.

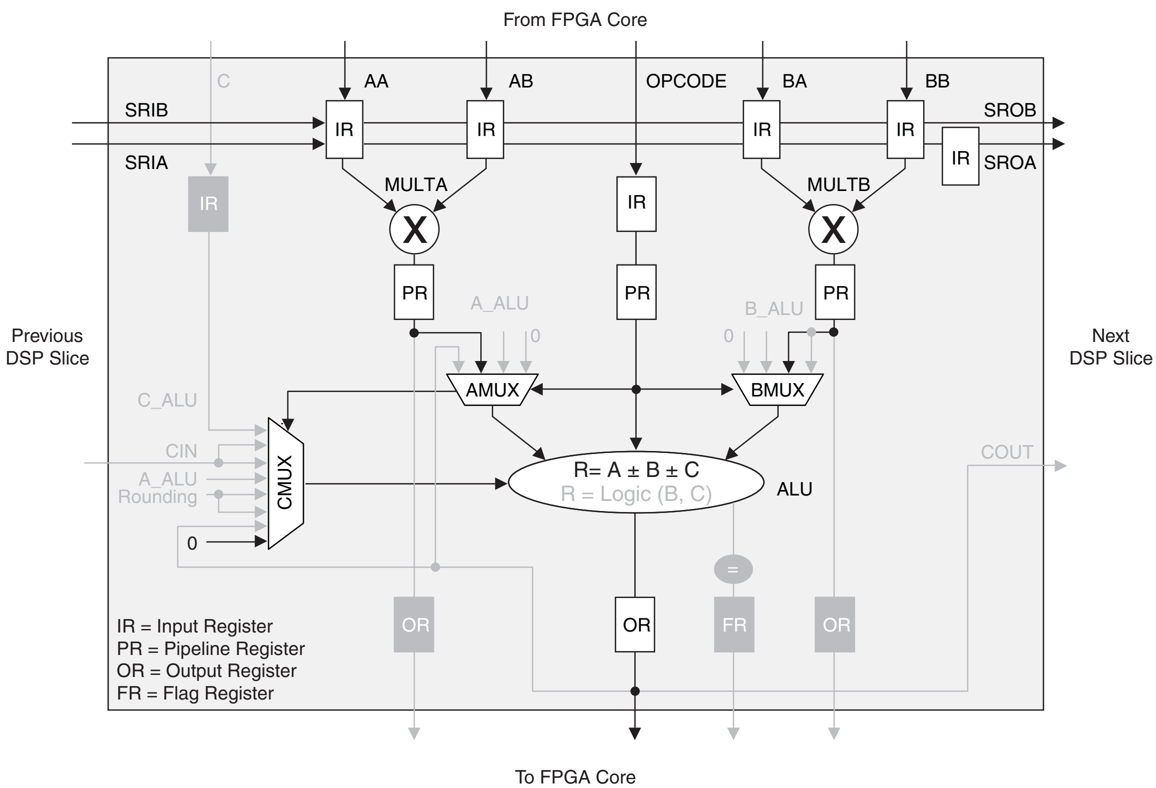
***Figure 2-28. MMAC sysDSP Element***



## MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 2-29 shows the MULTADDSUB sysDSP element.

***Figure 2-29. MULTADDSUB***



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-32. The PAD Labels “T” and “C” distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as LVDS inputs.

***Table 2-11. PIO Signal List***

| Name | Type | Description |
|---|---|---|
| INDD | Input Data | Register bypassed input. This is not the same port as INCK. |
| IPA, INA, IPB, INB | Input Data | Ports to core for input data |
| OPOSA, ONEGA[1], OPOSB, ONEGB[1] | Output Data | Output signals from core. An exception is the ONEGB port, used for tristate logic at the DQS pad. |
| CE | PIO Control | Clock enables for input and output block flip-flops. |
| SCLK | PIO Control | System Clock (PCLK) for input and output/TS blocks. Connected from clock ISB. |
| LSR | PIO Control | Local Set/Reset |
| ECLK1, ECLK2 | PIO Control | Edge clock sources. Entire PIO selects one of two sources using mux. |
| ECLKDQSR[1] | Read Control | From DQS_STROBE, shifted strobe for memory interfaces only. |
| DDRCLKPOL[1] | Read Control | Ensures transfer from DQS domain to SCLK domain. |
| DDRLAT[1] | Read Control | Used to guarantee INDDRX2 gearing by selectively enabling a D-Flip-Flop in datapath. |
| DEL[3:0] | Read Control | Dynamic input delay control bits. |
| INCK | To Clock Distribution and PLL | PIO treated as clock PIO, path to distribute to primary clocks and PLL. |
| TS | Tristate Data | Tristate signal from core (SDR) |
| DQCLK0[1], DQCLK1[1] | Write Control | Two clocks edges, 90 degrees out of phase, used in output gearing. |
| DQSW[2] | Write Control | Used for output and tristate logic at DQS only. |
| DYNDEL[7:0] | Write Control | Shifting of write clocks for specific DQS group, using 6:0 each step is approximately 25ps, 128 steps. Bit 7 is an invert (timing depends on input frequency). There is also a static control for this 8-bit setting, enabled with a memory cell. |
| DCNTL[6:0] | PIO Control | Original delay code from DDR DLL |
| DATAVALID[1] | Output Data | Status flag from DATAVALID logic, used to indicate when input data is captured in IOLOGIC and valid to core. |
| READ | For DQS_Strobe | Read signal for DDR memory interface |
| DQSI | For DQS_Strobe | Unshifted DQS strobe from input pad |
| PRMBDET | For DQS_Strobe | DQSI biased to go high when DQSI is tristate, goes to input logic block as well as core logic. |
| GSRN | Control from routing | Global Set/Reset |

1. Signals available on left/right/top edges only.
2. Selected PIO.

# PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

## Input Register Block

The input register blocks for the PIOs, in the left, right and top edges, contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-33 shows the input register block for the left, right and top edges. The input register block for the bottom edge contains one element to register the input signal and no DDR registers. The following description applies to the input register block for PIOs in the left, right and top edges only.

2. **Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

   LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. **Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**
The sysI/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

   The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bi-directional pads to reduce ringing on the receiving end.

## Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$, $V_{CCIO8}$ and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The $V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas the $V_{CCIO}$ supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. $V_{CCIO}$ supplies should be powered-up before or together with the $V_{CC}$ and $V_{CCAUX}$ supplies.

## Supported sysI/O Standards

The LatticeECP3 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysI/O buffer to support a variety of standards please see TN1177, LatticeECP3 sysIO Usage Guide.

*Table 2-14. Available SERDES Quads per LatticeECP3 Devices*

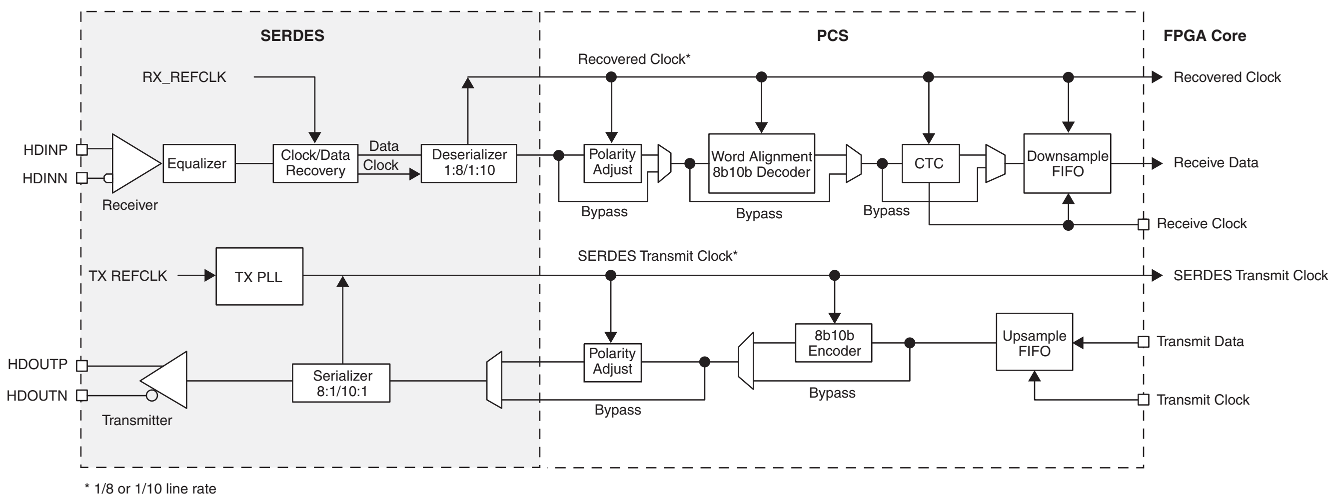
| Package | ECP3-17 | ECP3-35 | ECP3-70 | ECP3-95 | ECP3-150 |
|---|---|---|---|---|---|
| 256 ftBGA | 1 | 1 | — | — | — |
| 328 csBGA | 2 channels | — | — | — | — |
| 484 fpBGA | 1 | 1 | 1 | 1 | |
| 672 fpBGA | — | 1 | 2 | 2 | 2 |
| 1156 fpBGA | — | — | 3 | 3 | 4 |

## SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

*Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block*




## PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

## SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond and ispLEVER design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

# Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

***Table 2-15. LatticeECP3 Primary and Secondary Protocol Support***

| Primary Protocol | Secondary Protocol |
|---|---|
| PCI Express 1.1 | SGMII |
| PCI Express 1.1 | Gigabit Ethernet |
| PCI Express 1.1 | Serial RapidIO Type I |
| PCI Express 1.1 | Serial RapidIO Type II |
| Serial RapidIO Type I | SGMII |
| Serial RapidIO Type I | Gigabit Ethernet |
| Serial RapidIO Type II | SGMII |
| Serial RapidIO Type II | Gigabit Ethernet |
| Serial RapidIO Type II | Serial RapidIO Type I |
| CPRI-3 | CPRI-2 and CPRI-1 |
| 3G-SDI | HD-SDI and SD-SDI |

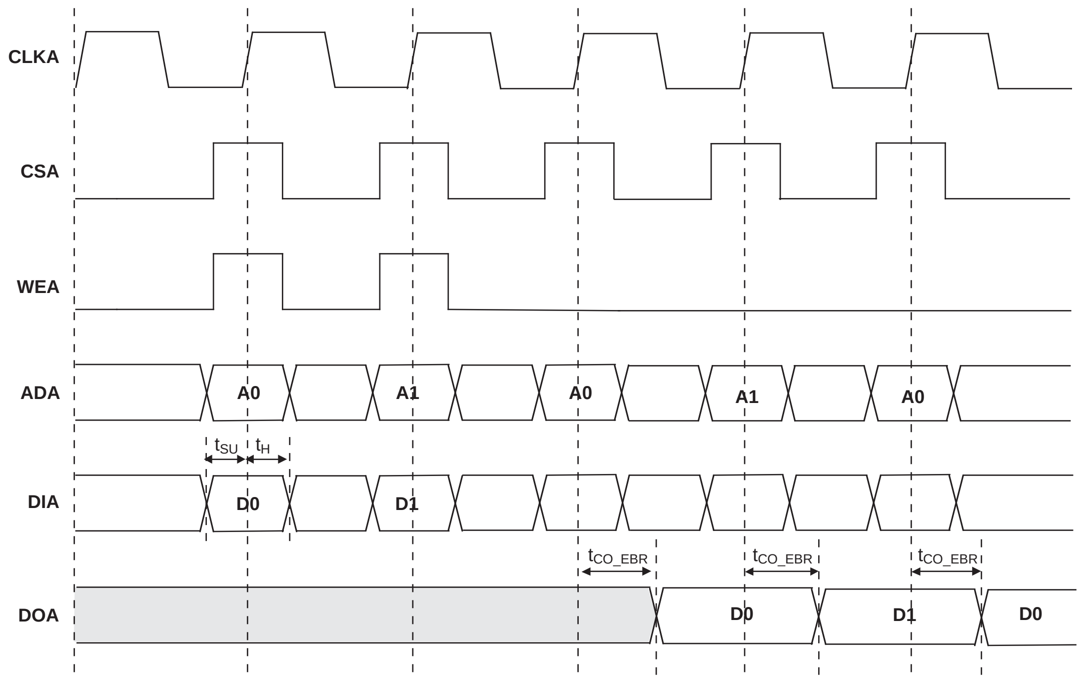
## LatticeECP3 External Switching Characteristics (Continued)[1, 2, 3, 13]

### Over Recommended Commercial Operating Conditions

| Parameter | Description | Device | –8 | | –7 | | –6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | ECP3-70EA/95EA | 0.7 | — | 0.7 | — | 0.8 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | ECP3-70EA/95EA | 1.6 | — | 1.8 | — | 2.0 | — | ns |
| $t_{H\_DELPLL}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | ECP3-70EA/95EA | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | ECP3-35EA | — | 3.2 | — | 3.4 | — | 3.6 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | ECP3-35EA | 0.6 | — | 0.7 | — | 0.8 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | ECP3-35EA | 0.3 | — | 0.3 | — | 0.4 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | ECP3-35EA | 1.6 | — | 1.7 | — | 1.8 | — | ns |
| $t_{H\_DELPLL}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | ECP3-35EA | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | ECP3-17EA | — | 3.0 | — | 3.3 | — | 3.5 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | ECP3-17EA | 0.6 | — | 0.7 | — | 0.8 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | ECP3-17EA | 0.3 | — | 0.3 | — | 0.4 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | ECP3-17EA | 1.6 | — | 1.7 | — | 1.8 | — | ns |
| $t_{H\_DELPLL}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | ECP3-17EA | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| **Generic DDR[12]** | | | | | | | | | |
| **Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Pin for Clock Input** | | | | | | | | | |
| $t_{SUGDDR}$ | Data Setup Before CLK | All ECP3EA Devices | 480 | — | 480 | — | 480 | — | ps |
| $t_{HOGDDR}$ | Data Hold After CLK | All ECP3EA Devices | 480 | — | 480 | — | 480 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | All ECP3EA Devices | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.PLL.Aligned) Using PLLCLKIN Pin for Clock Input** | | | | | | | | | |
| **Data Left, Right, and Top Sides and Clock Left and Right Sides** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | All ECP3EA Devices | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | All ECP3EA Devices | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | All ECP3EA Devices | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.Aligned) Using DLL - CLKIN Pin for Clock Input** | | | | | | | | | |
| **Data Left, Right and Top Sides and Clock Left and Right Sides** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | All ECP3EA Devices | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | All ECP3EA Devices | 0.775 | — | 0.775 | — | 0.775 | — | UI |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | All ECP3EA Devices | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX1 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX1_RX.DQS.Centered) Using DQS Pin for Clock Input** | | | | | | | | | |
| $t_{SUGDDR}$ | Data Setup After CLK | All ECP3EA Devices | 535 | — | 535 | — | 535 | — | ps |
| $t_{HOGDDR}$ | Data Hold After CLK | All ECP3EA Devices | 535 | — | 535 | — | 535 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | All ECP3EA Devices | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX1 Inputs with Clock and Data (<10bits wide) Aligned at Pin (GDDRX1_RX.DQS.Aligned) Using DQS Pin for Clock Input** | | | | | | | | | |
| **Data and Clock Left and Right Sides** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | All ECP3EA Devices | — | 0.225 | — | 0.225 | — | 0.225 | UI |

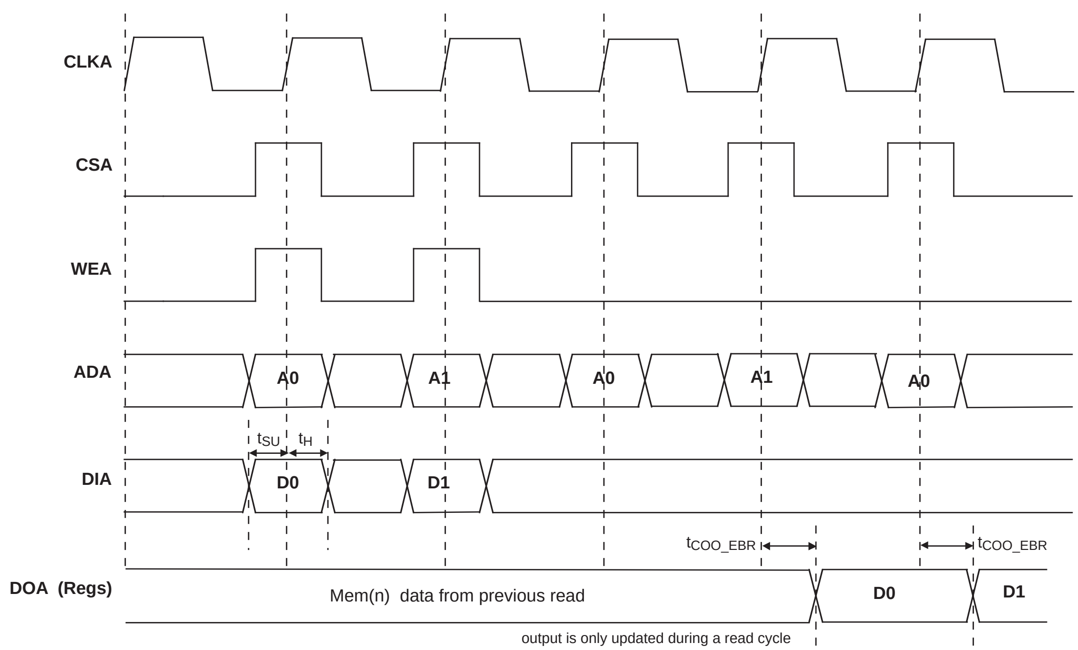
## Timing Diagrams

***Figure 3-9. Read/Write Mode (Normal)***




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

***Figure 3-10. Read/Write Mode with Input and Output Registers***



## LatticeECP3 Family Timing Adders[1, 2, 3, 4, 5, 7] (Continued)

**Over Recommended Commercial Operating Conditions**

| Buffer Type | Description | –8 | –7 | –6 | Units |
|---|---|---|---|---|---|
| RSDS25 | RSDS, VCCIO = 2.5 V | –0.07 | –0.04 | –0.01 | ns |
| PPLVDS | Point-to-Point LVDS, True LVDS, VCCIO = 2.5 V or 3.3 V | –0.22 | –0.19 | –0.16 | ns |
| LVPECL33 | LVPECL, Emulated, VCCIO = 3.3 V | 0.67 | 0.76 | 0.86 | ns |
| HSTL18_I | HSTL_18 class I 8mA drive, VCCIO = 1.8 V | 1.20 | 1.34 | 1.47 | ns |
| HSTL18_II | HSTL_18 class II, VCCIO = 1.8 V | 0.89 | 1.00 | 1.11 | ns |
| HSTL18D_I | Differential HSTL 18 class I 8 mA drive | 1.20 | 1.34 | 1.47 | ns |
| HSTL18D_II | Differential HSTL 18 class II | 0.89 | 1.00 | 1.11 | ns |
| HSTL15_I | HSTL_15 class I 4 mA drive, VCCIO = 1.5 V | 1.67 | 1.83 | 1.99 | ns |
| HSTL15D_I | Differential HSTL 15 class I 4 mA drive | 1.67 | 1.83 | 1.99 | ns |
| SSTL33_I | SSTL_3 class I, VCCIO = 3.3 V | 1.12 | 1.17 | 1.21 | ns |
| SSTL33_II | SSTL_3 class II, VCCIO = 3.3 V | 1.08 | 1.12 | 1.15 | ns |
| SSTL33D_I | Differential SSTL_3 class I | 1.12 | 1.17 | 1.21 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 1.08 | 1.12 | 1.15 | ns |
| SSTL25_I | SSTL_2 class I 8 mA drive, VCCIO = 2.5 V | 1.06 | 1.19 | 1.31 | ns |
| SSTL25_II | SSTL_2 class II 16 mA drive, VCCIO = 2.5 V | 1.04 | 1.17 | 1.31 | ns |
| SSTL25D_I | Differential SSTL_2 class I 8 mA drive | 1.06 | 1.19 | 1.31 | ns |
| SSTL25D_II | Differential SSTL_2 class II 16 mA drive | 1.04 | 1.17 | 1.31 | ns |
| SSTL18_I | SSTL_1.8 class I, VCCIO = 1.8 V | 0.70 | 0.84 | 0.97 | ns |
| SSTL18_II | SSTL_1.8 class II 8 mA drive, VCCIO = 1.8 V | 0.70 | 0.84 | 0.97 | ns |
| SSTL18D_I | Differential SSTL_1.8 class I | 0.70 | 0.84 | 0.97 | ns |
| SSTL18D_II | Differential SSTL_1.8 class II 8 mA drive | 0.70 | 0.84 | 0.97 | ns |
| SSTL15 | SSTL_1.5, VCCIO = 1.5 V | 1.22 | 1.35 | 1.48 | ns |
| SSTL15D | Differential SSTL_15 | 1.22 | 1.35 | 1.48 | ns |
| LVTTL33_4mA | LVTTL 4 mA drive, VCCIO = 3.3V | 0.25 | 0.24 | 0.23 | ns |
| LVTTL33_8mA | LVTTL 8 mA drive, VCCIO = 3.3V | –0.06 | –0.06 | –0.07 | ns |
| LVTTL33_12mA | LVTTL 12 mA drive, VCCIO = 3.3V | –0.01 | –0.02 | –0.02 | ns |
| LVTTL33_16mA | LVTTL 16 mA drive, VCCIO = 3.3V | –0.07 | –0.07 | –0.08 | ns |
| LVTTL33_20mA | LVTTL 20 mA drive, VCCIO = 3.3V | –0.12 | –0.13 | –0.14 | ns |
| LVCMOS33_4mA | LVCMOS 3.3 4 mA drive, fast slew rate | 0.25 | 0.24 | 0.23 | ns |
| LVCMOS33_8mA | LVCMOS 3.3 8 mA drive, fast slew rate | –0.06 | –0.06 | –0.07 | ns |
| LVCMOS33_12mA | LVCMOS 3.3 12 mA drive, fast slew rate | –0.01 | –0.02 | –0.02 | ns |
| LVCMOS33_16mA | LVCMOS 3.3 16 mA drive, fast slew rate | –0.07 | –0.07 | –0.08 | ns |
| LVCMOS33_20mA | LVCMOS 3.3 20 mA drive, fast slew rate | –0.12 | –0.13 | –0.14 | ns |
| LVCMOS25_4mA | LVCMOS 2.5 4 mA drive, fast slew rate | 0.12 | 0.10 | 0.09 | ns |
| LVCMOS25_8mA | LVCMOS 2.5 8 mA drive, fast slew rate | –0.05 | –0.06 | –0.07 | ns |
| LVCMOS25_12mA | LVCMOS 2.5 12 mA drive, fast slew rate | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS25_16mA | LVCMOS 2.5 16 mA drive, fast slew rate | –0.12 | –0.13 | –0.14 | ns |
| LVCMOS25_20mA | LVCMOS 2.5 20 mA drive, fast slew rate | –0.12 | –0.13 | –0.14 | ns |
| LVCMOS18_4mA | LVCMOS 1.8 4 mA drive, fast slew rate | 0.11 | 0.12 | 0.14 | ns |
| LVCMOS18_8mA | LVCMOS 1.8 8 mA drive, fast slew rate | 0.11 | 0.12 | 0.14 | ns |
| LVCMOS18_12mA | LVCMOS 1.8 12 mA drive, fast slew rate | –0.04 | –0.03 | –0.03 | ns |
| LVCMOS18_16mA | LVCMOS 1.8 16 mA drive, fast slew rate | –0.04 | –0.03 | –0.03 | ns |

## SERDES/PCS Block Latency

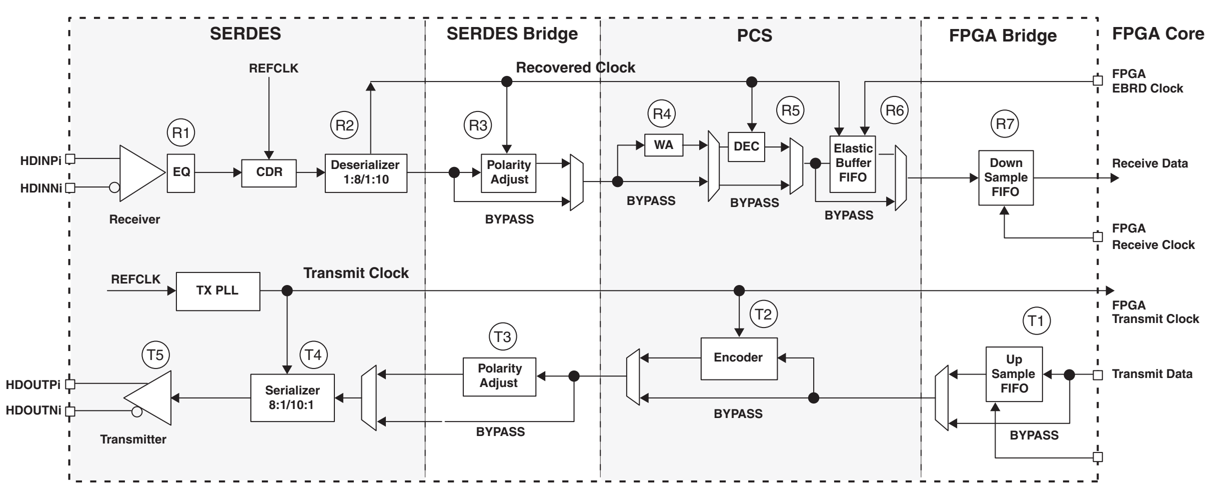
Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

***Table 3-8. SERDES/PCS Latency Breakdown***

| Item | Description | Min. | Avg. | Max. | Fixed | Bypass | Units |
|---|---|---|---|---|---|---|---|
| **Transmit Data Latency[1]** | | | | | | | |
| T1 | FPGA Bridge - Gearing disabled with different clocks | 1 | 3 | 5 | — | 1 | word clk |
| | FPGA Bridge - Gearing disabled with same clocks | — | — | — | 3 | 1 | word clk |
| | FPGA Bridge - Gearing enabled | 1 | 3 | 5 | — | — | word clk |
| T2 | 8b10b Encoder | — | — | — | 2 | 1 | word clk |
| T3 | SERDES Bridge transmit | — | — | — | 2 | 1 | word clk |
| T4 | Serializer: 8-bit mode | — | — | — | 15 + Δ1 | — | UI + ps |
| | Serializer: 10-bit mode | — | — | — | 18 + Δ1 | — | UI + ps |
| T5 | Pre-emphasis ON | — | — | — | 1 + Δ2 | — | UI + ps |
| | Pre-emphasis OFF | — | — | — | 0 + Δ3 | — | UI + ps |
| **Receive Data Latency[2]** | | | | | | | |
| R1 | Equalization ON | — | — | — | Δ1 | — | UI + ps |
| | Equalization OFF | — | — | — | Δ2 | — | UI + ps |
| R2 | Deserializer: 8-bit mode | — | — | — | 10 + Δ3 | — | UI + ps |
| | Deserializer: 10-bit mode | — | — | — | 12 + Δ3 | — | UI + ps |
| R3 | SERDES Bridge receive | — | — | — | 2 | — | word clk |
| R4 | Word alignment | 3.1 | — | 4 | — | — | word clk |
| R5 | 8b10b decoder | — | — | — | 1 | — | word clk |
| R6 | Clock Tolerance Compensation | 7 | 15 | 23 | 1 | 1 | word clk |
| R7 | FPGA Bridge - Gearing disabled with different clocks | 1 | 3 | 5 | — | 1 | word clk |
| | FPGA Bridge - Gearing disabled with same clocks | — | — | — | 3 | 1 | word clk |
| | FPGA Bridge - Gearing enabled | 1 | 3 | 5 | — | — | word clk |

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.

***Figure 3-12. Transmitter and Receiver Latency Block Diagram***



# HDMI (High-Definition Multimedia Interface) Electrical and Timing Characteristics

## AC and DC Characteristics

*Table 3-22. Transmit and Receive[1, 2]*

| Symbol | Description | Spec. Compliance | | Units |
|---|---|---|---|---|
| | | Min. Spec. | Max. Spec. | |
| **Transmit** | | | | |
| Intra-pair Skew | | — | 75 | ps |
| Inter-pair Skew | | — | 800 | ps |
| TMDS Differential Clock Jitter | | — | 0.25 | UI |
| **Receive** | | | | |
| $R_T$ | Termination Resistance | 40 | 60 | Ohms |
| $V_{ICM}$ | Input AC Common Mode Voltage (50-Ohm Setting) | — | 50 | mV |
| TMDS Clock Jitter | Clock Jitter Tolerance | — | 0.25 | UI |

1. Output buffers must drive a translation device. Max. speed is 2 Gbps. If translation device does not modify rise/fall time, the maximum speed is 1.5 Gbps.
2. Input buffers must be AC coupled in order to support the 3.3 V common mode. Generally, HDMI inputs are terminated by an external cable equalizer before data/clock is forwarded to the LatticeECP3 device.

*Figure 3-30. SPI Configuration Waveforms*

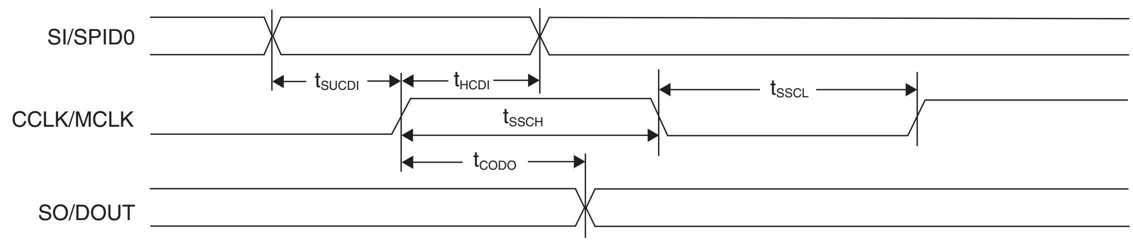
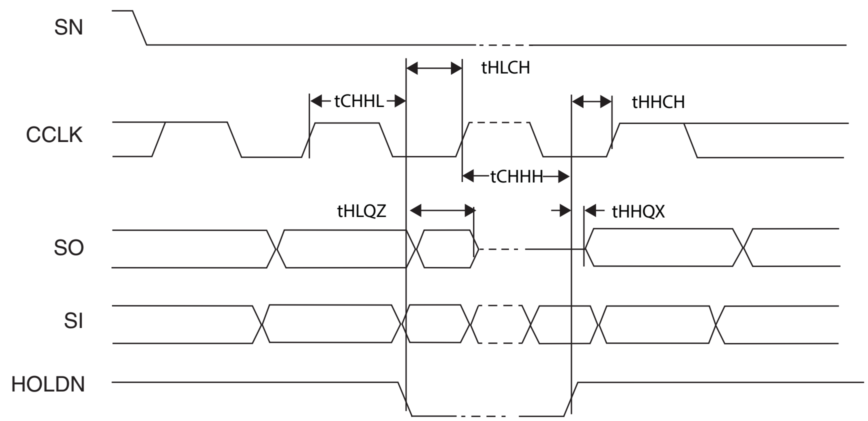


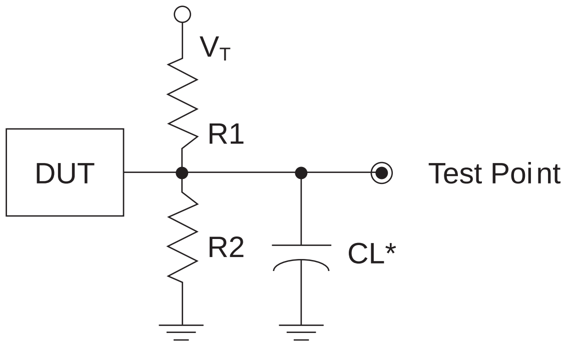

*Figure 3-31. Slave SPI HOLDN Waveforms*



## Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

***Figure 3-33. Output Test Load, LVTTL and LVCMOS Standards***




*CL Includes Test Fixture and Probe Capacitance

***Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces***

| Test Condition | $R_1$ | $R_2$ | $C_L$ | Timing Ref. | $V_T$ |
|---|---|---|---|---|---|
| LVTTL and other LVCMOS settings (L -> H, H -> L) | ∞ | ∞ | 0 pF | LVCMOS 3.3 = 1.5V | — |
| | | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVCMOS 2.5 I/O (Z -> H) | ∞ | 1MΩ | 0 pF | $V_{CCIO}/2$ | — |
| LVCMOS 2.5 I/O (Z -> L) | 1 MΩ | ∞ | 0 pF | $V_{CCIO}/2$ | $V_{CCIO}$ |
| LVCMOS 2.5 I/O (H -> Z) | ∞ | 100 | 0 pF | $V_{OH}$ - 0.10 | — |
| LVCMOS 2.5 I/O (L -> Z) | 100 | ∞ | 0 pF | $V_{OL}$ + 0.10 | $V_{CCIO}$ |

Note: Output test conditions for all other interfaces are determined by the respective standards.

## Pin Information Summary (Cont.)

| Pin Information Summary | | ECP3-95EA | | | ECP3-150EA | |
|---|---|---|---|---|---|---|
| Pin Type | | 484 fpBGA | 672 fpBGA | 1156 fpBGA | 672 fpBGA | 1156 fpBGA |
| Emulated Differential I/O per Bank | Bank 0 | 21 | 30 | 43 | 30 | 47 |
| | Bank 1 | 18 | 24 | 39 | 24 | 43 |
| | Bank 2 | 8 | 12 | 13 | 12 | 18 |
| | Bank 3 | 20 | 23 | 33 | 23 | 37 |
| | Bank 6 | 22 | 25 | 33 | 25 | 37 |
| | Bank 7 | 11 | 16 | 18 | 16 | 24 |
| | Bank 8 | 12 | 12 | 12 | 12 | 12 |
| Highspeed Differential I/O per Bank | Bank 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 6 | 9 | 9 | 9 | 15 |
| | Bank 3 | 9 | 12 | 16 | 12 | 21 |
| | Bank 6 | 11 | 14 | 16 | 14 | 21 |
| | Bank 7 | 9 | 12 | 13 | 12 | 18 |
| | Bank 8 | 0 | 0 | 0 | 0 | 0 |
| Total Single Ended/ Total Differential I/O per Bank | Bank 0 | 42/21 | 60/30 | 86/43 | 60/30 | 94/47 |
| | Bank 1 | 36/18 | 48/24 | 78/39 | 48/24 | 86/43 |
| | Bank 2 | 28/14 | 42/21 | 44/22 | 42/21 | 66/33 |
| | Bank 3 | 58/29 | 71/35 | 98/49 | 71/35 | 116/58 |
| | Bank 6 | 67/33 | 78/39 | 98/49 | 78/39 | 116/58 |
| | Bank 7 | 40/20 | 56/28 | 62/31 | 56/28 | 84/42 |
| | Bank 8 | 24/12 | 24/12 | 24/12 | 24/12 | 24/12 |
| DDR Groups Bonded per Bank | Bank 0 | 3 | 5 | 7 | 5 | 7 |
| | Bank 1 | 3 | 4 | 7 | 4 | 7 |
| | Bank 2 | 2 | 3 | 3 | 3 | 4 |
| | Bank 3 | 3 | 4 | 5 | 4 | 7 |
| | Bank 6 | 4 | 4 | 5 | 4 | 7 |
| | Bank 7 | 3 | 4 | 4 | 4 | 6 |
| | Configuration Bank8 | 0 | 0 | 0 | 0 | 0 |
| SERDES Quads | | 1 | 2 | 3 | 2 | 4 |

1.These pins must remain floating on the board.

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2010 | 01.6 | Architecture | Added Read-Before-Write information. |
| | | DC and Switching Characteristics | Added footnote #6 to Maximum I/O Buffer Speed table. |
| | | | Corrected minimum operating conditions for input and output differential voltages in the Point-to-Point LVDS table. |
| | | Pinout Information | Added pin information for the LatticeECP3-70EA and LatticeECP3-95EA devices. |
| | | Ordering Information | Added ordering part numbers for the LatticeECP3-70EA and LatticeECP3-95EA devices. |
| | | | Removed dual mark information. |
| November 2009 | 01.5 | Introduction | Updated Embedded SERDES features. |
| | | | Added SONET/SDH to Embedded SERDES protocols. |
| | | Architecture | Updated Figure 2-4, General Purpose PLL Diagram. |
| | | | Updated SONET/SDH to SERDES and PCS protocols. |
| | | | Updated Table 2-13, SERDES Standard Support to include SONET/ SDH and updated footnote 2. |
| | | DC and Switching Characterisitcs | Added footnote to ESD Performance table. |
| | | | Updated SERDES Power Supply Requirements table and footnotes. |
| | | | Updated Maximum I/O Buffer Speed table. |
| | | | Updated Pin-to-Pin Peformance table. |
| | | | Updated sysCLOCK PLL Timing table. |
| | | | Updated DLL timing table. |
| | | | Updated High-Speed Data Transmitter tables. |
| | | | Updated High-Speed Data Receiver table. |
| | | | Updated footnote for Receiver Total Jitter Tolerance Specification table. |
| | | | Updated Periodic Receiver Jitter Tolerance Specification table. |
| | | | Updated SERDES External Reference Clock Specification table. |
| | | | Updated PCI Express Electrical and Timing AC and DC Characteristics. |
| | | | Deleted Reference Clock table for PCI Express Electrical and Timing AC and DC Characteristics. |
| | | | Updated SMPTE AC/DC Characteristics Transmit table. |
| | | | Updated Mini LVDS table. |
| | | | Updated RSDS table. |
| | | | Added Supply Current (Standby) table for EA devices. |
| | | | Updated Internal Switching Characteristics table. |
| | | | Updated Register-to-Register Performance table. |
| | | | Added HDMI Electrical and Timing Characteristics data. |
| | | | Updated Family Timing Adders table. |
| | | | Updated sysCONFIG Port Timing Specifications table. |
| | | | Updated Recommended Operating Conditions table. |
| | | | Updated Hot Socket Specifications table. |
| | | | Updated Single-Ended DC table. |
| | | | Updated TRLVDS table and figure. |
| | | | Updated Serial Data Input Specifications table. |
| | | | Updated HDMI Transmit and Receive table. |
| | | Ordering Information | Added LFE3-150EA “TW” devices and footnotes to the Commercial and Industrial tables. |