E. Lattice Semiconductor Corporation - <u>LFE3-95EA-8LFN1156I Datasheet</u>



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Details

Product Status	Active
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-8lfn1156i

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LatticeECP3 Family Data Sheet Architecture

June 2013

Data Sheet DS1021

Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM[™] Embedded Block RAM (EBR) and rows of sys-DSP[™] Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysl/O buffers. The sysl/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

The LatticeECP3 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG[™] port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

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Figure 2-3. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows: WCK is CLK WRE is from LSR

DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2 WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Туре	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

1. See Figure 2-3 for connection details.

2. Requires two PFUs.



Figure 2-4. General Purpose PLL Diagram



Table 2-4 provides a description of the signals in the PLL blocks.

Table 2-4. PLL Blocks Signal Descriptions

Signal	I/O	Description			
CLKI	I	Clock input from external pin or routing			
CLKFB	I	PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic)			
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers			
RSTK	I	"1" to reset K-divider			
WRDEL	I	DPA Fine Delay Adjust input			
CLKOS	0	PLL output to clock tree (phase shifted/duty cycle changed)			
CLKOP	0	PLL output to clock tree (no phase shift)			
CLKOK	0	PLL output to clock tree through secondary clock divider			
CLKOK2	0	PLL output to clock tree (CLKOP divided by 3)			
LOCK	0	"1" indicates PLL LOCK to CLKI			
FDA [3:0]	I	Dynamic fine delay adjustment on CLKOS output			
DRPAI[3:0]	I	Dynamic coarse phase shift, rising edge setting			
DFPAI[3:0]	I	ynamic coarse phase shift, falling edge setting			

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP3 family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay



Table 2-5. DLL Signals

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
CLKOP	0	The primary clock output
CLKOS	0	The secondary clock output with fine delay shift and/or division by 2 or by 4
LOCK	0	Active high phase lock indicator
INCI	I	Incremental indicator from another DLL via CIB.
GRAYI[5:0]	I	Gray-coded digital control bus from another DLL in time reference mode.
DIFF	0	Difference indicator when DCNTL is difference than the internal setting and update is needed.
INCO	0	Incremental indicator to other DLLs via CIB.
GRAYO[5:0]	0	Gray-coded digital control bus to other DLLs via CIB

LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 2-6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

For more information, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide.

Figure 2-6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line



* This signal is not user accessible. It can only be used to feed the slave delay line.



For further information, please refer to TN1182, LatticeECP3 sysDSP Usage Guide.

MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

Figure 2-26. MULT sysDSP Element



To FPGA Core



MMAC DSP Element

The LatticeECP3 supports a MAC with two multipliers. This is called Multiply Multiply Accumulate or MMAC. In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value and with the result of the multiplier operation of operands BA and BB. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-28 shows the MMAC sysDSP element.



Figure 2-28. MMAC sysDSP Element



Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-32. The PAD Labels "T" and "C" distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as LVDS inputs.

Table 2-11. PIO Signal List

Name	Туре	Description
INDD	Input Data	Register bypassed input. This is not the same port as INCK.
IPA, INA, IPB, INB	Input Data	Ports to core for input data
OPOSA, ONEGA ¹ , OPOSB, ONEGB ¹	Output Data	Output signals from core. An exception is the ONEGB port, used for tristate logic at the DQS pad.
CE	PIO Control	Clock enables for input and output block flip-flops.
SCLK	PIO Control	System Clock (PCLK) for input and output/TS blocks. Connected from clock ISB.
LSR	PIO Control	Local Set/Reset
ECLK1, ECLK2	PIO Control	Edge clock sources. Entire PIO selects one of two sources using mux.
ECLKDQSR ¹	Read Control	From DQS_STROBE, shifted strobe for memory interfaces only.
DDRCLKPOL ¹	Read Control	Ensures transfer from DQS domain to SCLK domain.
DDRLAT ¹	Read Control	Used to guarantee INDDRX2 gearing by selectively enabling a D-Flip-Flop in dat- apath.
DEL[3:0]	Read Control	Dynamic input delay control bits.
INCK	To Clock Distribution and PLL	PIO treated as clock PIO, path to distribute to primary clocks and PLL.
TS	Tristate Data	Tristate signal from core (SDR)
DQCLK0 ¹ , DQCLK1 ¹	Write Control	Two clocks edges, 90 degrees out of phase, used in output gearing.
DQSW ²	Write Control	Used for output and tristate logic at DQS only.
DYNDEL[7:0]	Write Control	Shifting of write clocks for specific DQS group, using 6:0 each step is approxi- mately 25ps, 128 steps. Bit 7 is an invert (timing depends on input frequency). There is also a static control for this 8-bit setting, enabled with a memory cell.
DCNTL[6:0]	PIO Control	Original delay code from DDR DLL
DATAVALID ¹	Output Data	Status flag from DATAVALID logic, used to indicate when input data is captured in IOLOGIC and valid to core.
READ	For DQS_Strobe	Read signal for DDR memory interface
DQSI	For DQS_Strobe	Unshifted DQS strobe from input pad
PRMBDET	For DQS_Strobe	DQSI biased to go high when DQSI is tristate, goes to input logic block as well as core logic.
GSRN	Control from routing	Global Set/Reset

1. Signals available on left/right/top edges only.

2. Selected PIO.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs, in the left, right and top edges, contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-33 shows the input register block for the left, right and top edges. The input register block for the bottom edge contains one element to register the input signal and no DDR registers. The following description applies to the input register block for PIOs in the left, right and top edges only.



Figure 2-37. DQS Local Bus



Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

DDR3 Memory Support

LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.



On-Chip Programmable Termination

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 40, 50, or 60 Ohms. External termination to Vtt should be used for DDR2 and DDR3 memory controller implementation.
- Common mode termination of 80, 100, 120 Ohms for differential inputs

Figure 2-39. On-Chip Termination



Programmable resistance (40, 50 and 60 Ohms)
Parallel Single-Ended Input

Differential Input

See Table 2-12 for termination options for input modes.

Table 2-12. On-Chip Termination Options for Input Modes

IO_TYPE	TERMINATE to VTT ^{1, 2}	DIFFERENTIAL TERMINATION RESISTOR ¹
LVDS25	þ	80, 100, 120
BLVDS25	þ	80, 100, 120
MLVDS	þ	80, 100, 120
HSTL18_I	40, 50, 60	þ
HSTL18_II	40, 50, 60	þ
HSTL18D_I	40, 50, 60	þ
HSTL18D_II	40, 50, 60	þ
HSTL15_I	40, 50, 60	þ
HSTL15D_I	40, 50, 60	þ
SSTL25_I	40, 50, 60	þ
SSTL25_II	40, 50, 60	þ
SSTL25D_I	40, 50, 60	þ
SSTL25D_II	40, 50, 60	þ
SSTL18_I	40, 50, 60	þ
SSTL18_II	40, 50, 60	þ
SSTL18D_I	40, 50, 60	þ
SSTL18D_II	40, 50, 60	þ
SSTL15	40, 50, 60	þ
SSTL15D	40, 50, 60	þ

1. TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature. Use of TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in

an I/O bank.

On-chip termination tolerance +/- 20%

2. External termination to VTT should be used when implementing DDR2 and DDR3 memory controller.

There are some restrictions to be aware of when using spread spectrum. When a quad shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the quad is compatible with all protocols within the quad. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LatticeECP3 architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, Serial RapidIO or SGMII channel within the same quad, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, Serial RapidIO and SGMII transmit jitter specifications.

For further information on SERDES, please see TN1176, LatticeECP3 SERDES/PCS Usage Guide.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Device Configuration

All LatticeECP3 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. The sysCONFIG port includes seven I/Os used as dedicated pins with the remaining pins used as dual-use pins. See TN1169, LatticeECP3 sysCONFIG Usage Guide for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure a LatticeECP3 device:

- 1. JTAG
- 2. Standard Serial Peripheral Interface (SPI and SPIm modes) interface to boot PROM memory
- 3. System microprocessor to drive a x8 CPU port (PCM mode)
- 4. System microprocessor to drive a serial slave SPI port (SSPI mode)
- 5. Generic byte wide flash with a MachXO[™] device, providing control and addressing

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

LatticeECP3 devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

			-8		-7		-6		
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-70EA/95EA	0.7	—	0.7	—	0.8	—	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70EA/95EA	1.6	—	1.8	_	2.0	—	ns
t _{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70EA/95EA	0.0	—	0.0	—	0.0	—	ns
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-35EA	_	3.2	—	3.4	—	3.6	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-35EA	0.6	_	0.7	—	0.8	—	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-35EA	0.3	—	0.3	—	0.4	-	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-35EA	1.6	_	1.7	_	1.8	_	ns
t _{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-35EA	0.0	_	0.0	_	0.0	_	ns
t _{COPLL}	Clock to Output - PIO Output Register	ECP3-17EA	_	3.0	—	3.3	—	3.5	ns
t _{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-17EA	0.6	_	0.7	_	0.8	—	ns
t _{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-17EA	0.3	_	0.3	_	0.4	—	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-17EA	1.6	—	1.7	—	1.8	—	ns
t _{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-17EA	0.0	_	0.0	_	0.0	—	ns
Generic DDR ¹²									
Generic DDRX1 In Input	puts with Clock and Data (>10 Bits	Wide) Centered at Pi	n (GDDF	RX1_RX.S	SCLK.Ce	ntered) L	Ising PC	LK Pin fo	or Clock
t _{SUGDDR}	Data Setup Before CLK	All ECP3EA Devices	480	—	480	_	480		ps
t _{HOGDDR}	Data Hold After CLK	All ECP3EA Devices	480	—	480	—	480		ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	—	250	—	250	—	250	MHz
Generic DDRX1 In Clock Input	puts with Clock and Data (>10 Bits	Wide) Aligned at Pin	(GDDR)	(1_RX.SC	CLK.PLL	Aligned)	Using P	LLCLKIN	Pin for
Data Left, Right, a	nd Top Sides and Clock Left and F	Right Sides							
t _{DVACLKGDDR}	Data Setup Before CLK	All ECP3EA Devices	_	0.225		0.225		0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775	_	UI
f _{MAX GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	_	250	—	250	_	250	MHz
Generic DDRX1 In Clock Input	puts with Clock and Data (>10 Bits	Wide) Aligned at Pin	(GDDR)	(1_RX.S0	CLK.Alig	ned) Usiı	ng DLL -	CLKIN P	in for
Data Left, Right ar	d Top Sides and Clock Left and R	ight Sides							
t _{DVACLKGDDR}	Data Setup Before CLK	All ECP3EA Devices	_	0.225	—	0.225	—	0.225	UI
t _{DVECLKGDDR}	Data Hold After CLK	All ECP3EA Devices	0.775	—	0.775	—	0.775		UI
f _{MAX GDDR}	DDRX1 Clock Frequency	All ECP3EA Devices	_	250	—	250	_	250	MHz
Generic DDRX1 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX1_RX.DQS.Centered) Using DQS Pin for Clock									
t _{SUGDDB}	Data Setup After CLK	All ECP3EA Devices	535	_	535		535		ps
tHOGDDR	Data Hold After CLK	All ECP3EA Devices	535	—	535		535	_	ps
f _{MAX GDDB}	DDRX1 Clock Frequency	All ECP3EA Devices	_	250	—	250	_	250	MHz
Generic DDRX1 In	puts with Clock and Data (<10bits	wide) Aligned at Pin (GDDRX	1_RX.DQ	S.Aligne	d) Using	DQS Pin	for Cloc	k Input
Data and Clock Le	ft and Right Sides	`			-				-
t _{DVACI KGDDB}	Data Setup Before CLK	All ECP3EA Devices	—	0.225	_	0.225		0.225	UI
STROLIGED									

Over Recommended Commercial Operating Conditions



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
fMAX GDDB	DDRX1 Clock Frequency	ECP3-70EA/95EA		250		250	_	250	MHz
	Data Valid Before CLK	ECP3-35EA	683	—	688	_	690	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	683	_	688	_	690	_	ps
f _{MAX GDDR}	DDRX1 Clock Frequency	ECP3-35EA	_	250	_	250	_	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	683	—	688	_	690	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	683	—	688	—	690	—	ps
f _{MAX} GDDR	DDRX1 Clock Frequency	ECP3-17EA	_	250	_	250	—	250	MHz
Generic DDRX1 Ou	itput with Clock and Data Aligned	at Pin (GDDRX1_TX.	SCLK.Ali	gned) ¹⁰					
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-150EA	—	335	—	338	—	341	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-150EA		335	_	338	—	341	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA		250	_	250	—	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-70EA/95EA	_	339	_	343	—	347	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-70EA/95EA	_	339	_	343	—	347	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250	—	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-35EA	_	322	_	320	—	321	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-35EA	_	322	_	320	—	321	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	_	250	_	250	—	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-17EA	_	322	_	320	—	321	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-17EA	_	322	_	320	_	321	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA		250	_	250	—	250	MHz
Generic DDRX1 Ou	itput with Clock and Data (<10 Bi	ts Wide) Centered at P	in (GDD	RX1_TX.	DQS.Cen	tered) ¹⁰			
Left and Right Side	es								
t _{DVBGDDR}	Data Valid Before CLK	ECP3-150EA	670	_	670	—	670	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	_	250		250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-70EA/95EA	657	—	652	—	650	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-70EA/95EA	657	—	652	_	650	_	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-35EA	670	—	675	—	676	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	670	—	675	_	676	_	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	_	250	_	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	670	—	670	—	670	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	670	—	670	—	670	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA	_	250	_	250	—	250	MHz
Generic DDRX2 Ou	itput with Clock and Data (>10 Bi	ts Wide) Aligned at Pir	n (GDDR	X2_TX.A	igned)				
Left and Right Side	es								
t _{DIBGDDR}	Data Invalid Before Clock	All ECP3EA Devices		200		210		220	ps
t _{DIAGDDR}	Data Invalid After Clock	All ECP3EA Devices	_	200	_	210	_	220	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	500	_	420	—	375	MHz
Generic DDRX2 Ou	Generic DDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using DQSDLL (GDDRX2_TX.DQSDLL.Centered) ¹¹								
Left and Right Side	es								
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	400		400		431		ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	400		400	—	432		ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	400	_	400	—	375	MHz

Over Recommended Commercial Operating Conditions



Table 3-7. Channel Output Jitter

Description	Frequency	Min.	Тур.	Max.	Units
Deterministic	3.125 Gbps	—	—	0.17	UI, p-p
Random	3.125 Gbps	—	—	0.25	UI, p-p
Total	3.125 Gbps	—	—	0.35	UI, p-p
Deterministic	2.5 Gbps	—	—	0.17	UI, p-p
Random	2.5 Gbps	—	—	0.20	UI, p-p
Total	2.5 Gbps	—	—	0.35	UI, p-p
Deterministic	1.25 Gbps	—	—	0.10	UI, p-p
Random	1.25 Gbps	—	—	0.22	UI, p-p
Total	1.25 Gbps	—	—	0.24	UI, p-p
Deterministic	622 Mbps	—	—	0.10	UI, p-p
Random	622 Mbps	—	—	0.20	UI, p-p
Total	622 Mbps	—	—	0.24	UI, p-p
Deterministic	250 Mbps	—	—	0.10	UI, p-p
Random	250 Mbps	—	—	0.18	UI, p-p
Total	250 Mbps	—	—	0.24	UI, p-p
Deterministic	150 Mbps	—	—	0.10	UI, p-p
Random	150 Mbps	—	—	0.18	UI, p-p
Total	150 Mbps	—		0.24	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.



XAUI/Serial Rapid I/O Type 3/CPRI LV E.30 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-13. Transmit

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
T _{RF}	Differential rise/fall time	20%-80%	_	80	—	ps
Z _{TX_DIFF_DC}	Differential impedance		80	100	120	Ohms
J _{TX_DDJ} ^{2, 3, 4}	Output data deterministic jitter		_	—	0.17	UI
J _{TX_TJ} ^{1, 2, 3, 4}	Total output data jitter		_	—	0.35	UI

1. Total jitter includes both deterministic jitter and random jitter.

2. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Values are measured at 2.5 Gbps.

Table 3-14. Receive and Jitter Tolerance

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	_	_	dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	_	_	dB
Z _{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J _{RX_DJ} ^{1, 2, 3}	Deterministic jitter tolerance (peak-to-peak)		—		0.37	UI
J _{RX_RJ} ^{1, 2, 3}	Random jitter tolerance (peak-to-peak)		—		0.18	UI
J _{RX_SJ} ^{1, 2, 3}	Sinusoidal jitter tolerance (peak-to-peak)		—	_	0.10	UI
J _{RX_TJ} ^{1, 2, 3}	Total jitter tolerance (peak-to-peak)		—	_	0.65	UI
T _{RX_EYE}	Receiver eye opening		0.35			UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.

2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Jitter tolerance parameters are characterized when Full Rx Equalization is enabled.

5. Values are measured at 2.5 Gbps.



Switching Test Conditions

Figure 3-33 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

Figure 3-33. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-23. Te	est Fixture Required	Components,	Non-Terminated Interfaces
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Test Condition	R ₁	R ₂	CL	Timing Ref.	V _T
				LVCMOS 3.3 = 1.5V	
				LVCMOS 2.5 = $V_{CCIO}/2$	
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0 pF	LVCMOS 1.8 = V _{CCIO} /2	
				LVCMOS 1.5 = $V_{CCIO}/2$	_
				LVCMOS 1.2 = V _{CCIO} /2	_
LVCMOS 2.5 I/O (Z -> H)	8	1MΩ	0 pF	V _{CCIO} /2	
LVCMOS 2.5 I/O (Z -> L)	1 MΩ	∞	0 pF	V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H -> Z)	8	100	0 pF	V _{OH} - 0.10	
LVCMOS 2.5 I/O (L -> Z)	100	x	0 pF	V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.



Point-to-Point LVDS (PPLVDS)

Over Recommended Operating Conditions

Description	Min.	Тур.	Max.	Units
Output driver supply $(1/5\%)$	3.14	3.3	3.47	V
	2.25	2.5	2.75	V
Input differential voltage	100	—	400	mV
Input common mode voltage	0.2	—	2.3	V
Output differential voltage	130	—	400	mV
Output common mode voltage	0.5	0.8	1.4	V

RSDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Тур.	Max.	Units
V _{OD}	Output voltage, differential, R _T = 100 Ohms	100	200	600	mV
V _{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I _{RSDS}	Differential driver output current	1	2	6	mA
V _{THD}	Input voltage differential	100	—	-	mV
V _{CM}	Input common mode voltage	0.3	—	1.5	V
T _R , T _F	Output rise and fall times, 20% to 80%	—	500		ps
T _{ODUTY}	Output clock duty cycle	35	50	65	%

Note: Data is for 2 mA drive. Other differential driver current options are available.



Pin Information Summary (Cont.)

Pin Information	n Summary		ECP3-95EA		ECP3-	150EA
Pin Ty	ре	484 fpBGA	672 fpBGA	1156 fpBGA	672 fpBGA	1156 fpBGA
	Bank 0	21	30	43	30	47
	Bank 1	18	24	39	24	43
Emulated	Bank 2	8	12	Figson 1156 fpBGA 672 fpBGA 30 43 30 24 39 24 12 13 12 23 33 23 25 33 25 16 18 16 12 12 12 0 0 0 0 0 0 0 0 0 0 0 0 9 9 9 12 16 12 14 16 14 12 13 12 0 0 0 0/30 86/43 60/30 8/24 78/39 48/24 2/21 44/22 42/21 1/35 98/49 71/35 8/39 98/49 78/39 6/28 62/31 56/28 4/12 24/12 24/12 5 7 5	18	
Differential I/O	Bank 3	20	23	33	23	37
per Bank	Bank 6	22	25	33	25	37
	Bank 7	11	16	18	16	24
	Bank 8	12	12	12	12	12
	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
Highspeed	Bank 2	6	9	9	9	15
Differential I/O	Bank 3	9	12	16	12	21
per Bank	Bank 6	11	14	16	14	21
	Bank 7	9	12	13	12	18
	Bank 8	0	0	0	0	0
	Bank 0	42/21	60/30	86/43	60/30	94/47
	Bank 1	36/18	48/24	78/39	48/24	86/43
Total Single Ended/	Bank 2	28/14	42/21	44/22	42/21	66/33
Total Differential	Bank 3	58/29	71/35	98/49	71/35	116/58
I/O per Bank	Bank 6	67/33	78/39	98/49	78/39	116/58
	Bank 7	40/20	56/28	62/31	56/28	84/42
	Bank 8	24/12	24/12	24/12	24/12	24/12
	Bank 0	3	5	7	5	7
	Bank 1	3	4	7	4	7
	Bank 2	2	3	3	3	4
DDR Groups Bonded	Bank 3	3	4	5	4	7
per Bank	Bank 6	4	4	5	4	7
	Bank 7	3	4	4	4	6
	Configuration Bank8	0	0	0	0	0
SERDES Quads	1	1	2	3	2	4

1. These pins must remain floating on the board.



Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	67

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2 V	-6	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2 V	-7	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2 V	-8	STD	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6LFN484C	1.2 V	-6	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7LFN484C	1.2 V	-7	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8LFN484C	1.2 V	-8	LOW	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2 V	-6	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2 V	-7	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2 V	-8	STD	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6LFN672C	1.2 V	-6	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7LFN672C	1.2 V	-7	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8LFN672C	1.2 V	-8	LOW	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2 V	-6	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2 V	-7	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2 V	-8	STD	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-6LFN1156C	1.2 V	-6	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7LFN1156C	1.2 V	-7	LOW	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8LFN1156C	1.2 V	-8	LOW	Lead-Free fpBGA	1156	COM	92

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.



Industrial

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Power	Package ¹	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6MG328I	1.2 V	-6	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-7MG328I	1.2 V	-7	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-8MG328I	1.2 V	-8	STD	Lead-Free csBGA	328	IND	17
LFE3-17EA-6LMG328I	1.2 V	-6	LOW	Green csBGA	328	IND	17
LFE3-17EA-7LMG328I	1.2 V	-7	LOW	Green csBGA	328	IND	17
LFE3-17EA-8LMG328I	1.2 V	-8	LOW	Green csBGA	328	IND	17
LFE3-17EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	17
LFE3-17EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	17

1. Green = Halogen free and lead free.

Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256I	1.2 V	-6	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7FTN256I	1.2 V	-7	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8FTN256I	1.2 V	-8	STD	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6LFTN256I	1.2 V	-6	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7LFTN256I	1.2 V	-7	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8LFTN256I	1.2 V	-8	LOW	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6FN484I	1.2 V	-6	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7FN484I	1.2 V	-7	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8FN484I	1.2 V	-8	STD	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6LFN484I	1.2 V	-6	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7LFN484I	1.2 V	-7	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8LFN484I	1.2 V	-8	LOW	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	33
LFE3-35EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	33

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.



Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW ¹	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW ¹	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149

1. Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

• The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.

• The SERDES XRES pin on the TW device passes CDM testing at 250V.