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Details

Product Status	Not For New Designs
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	295
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95ea-9fn484i

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LatticeECP3 Family Data Sheet Architecture

June 2013

Data Sheet DS1021

Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM[™] Embedded Block RAM (EBR) and rows of sys-DSP[™] Digital Signal Processing slices, as shown in Figure 2-1. The LatticeECP3-150 has four rows of DSP slices; all other LatticeECP3 devices have two rows of DSP slices. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2 Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysl/O buffers. The sysl/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

The LatticeECP3 registers in PFU and sysl/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG[™] port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2 V as their core voltage.

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Figure 2-4. General Purpose PLL Diagram



Table 2-4 provides a description of the signals in the PLL blocks.

Table 2-4. PLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	0	PLL output to clock tree (phase shifted/duty cycle changed)
CLKOP	0	PLL output to clock tree (no phase shift)
CLKOK	0	PLL output to clock tree through secondary clock divider
CLKOK2	0	PLL output to clock tree (CLKOP divided by 3)
LOCK	0	"1" indicates PLL LOCK to CLKI
FDA [3:0]	I	Dynamic fine delay adjustment on CLKOS output
DRPAI[3:0]	I	Dynamic coarse phase shift, rising edge setting
DFPAI[3:0]	I	Dynamic coarse phase shift, falling edge setting

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP3 family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay



chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.



Figure 2-5. Delay Locked Loop Diagram (DLL)

* This signal is not user accessible. This can only be used to feed the slave delay line.



For further information, please refer to TN1182, LatticeECP3 sysDSP Usage Guide.

MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-26 shows the MULT sysDSP element.

Figure 2-26. MULT sysDSP Element



To FPGA Core



MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 2-29 shows the MULTADDSUB sysDSP element.

Figure 2-29. MULTADDSUB





ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

Resources Available in the LatticeECP3 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Device	DSP Slices	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP3-17	12	48	24	6
ECP3-35	32	128	64	16
ECP3-70	64	256	128	32
ECP3-95	64	256	128	32
ECP3-150	160	640	320	80

Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family

Table 2-10. Embedded SRAM in the LatticeECP3 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP3-17	38	700
ECP3-35	72	1327
ECP3-70	240	4420
ECP3-95	240	4420
ECP3-150	372	6850







Note: Simplified diagram does not show CE/SET/REST details.

Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysl/O buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDRX2 gearing of output logic. ODDRX2 gearing is used in DDR3 memory interfaces. The PIO blocks on the bottom contain the SDR registers but do not support generic DDR.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.



Figure 2-38. LatticeECP3 Banks



LatticeECP3 devices contain two types of sysI/O buffer pairs.

1. Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)

The sysl/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input. Only the top edge buffers have a programmable PCI clamp.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

The top and bottom sides are ideal for general purpose I/O, PCI, and inputs for LVDS (LVDS outputs are only allowed on the left and right sides). The top side can be used for the DDR3 ADDR/CMD signals.

The I/O pins located on the top and bottom sides of the device (labeled PTxxA/B or PBxxA/B) are fully hot socketable. Note that the pads in Banks 3, 6 and 8 are wrapped around the corner of the device. In these banks, only the pads located on the top or bottom of the device are hot socketable. The top and bottom side pads can be identified by the Lattice Diamond tool.



On-Chip Programmable Termination

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 40, 50, or 60 Ohms. External termination to Vtt should be used for DDR2 and DDR3 memory controller implementation.
- Common mode termination of 80, 100, 120 Ohms for differential inputs

Figure 2-39. On-Chip Termination



Programmable resistance (40, 50 and 60 Ohms)
Parallel Single-Ended Input

Differential Input

See Table 2-12 for termination options for input modes.

Table 2-12. On-Chip Termination Options for Input Modes

IO_TYPE	TERMINATE to VTT ^{1, 2}	DIFFERENTIAL TERMINATION RESISTOR ¹
LVDS25	þ	80, 100, 120
BLVDS25	þ	80, 100, 120
MLVDS	þ	80, 100, 120
HSTL18_I	40, 50, 60	þ
HSTL18_II	40, 50, 60	þ
HSTL18D_I	40, 50, 60	þ
HSTL18D_II	40, 50, 60	þ
HSTL15_I	40, 50, 60	þ
HSTL15D_I	40, 50, 60	þ
SSTL25_I	40, 50, 60	þ
SSTL25_II	40, 50, 60	þ
SSTL25D_I	40, 50, 60	þ
SSTL25D_II	40, 50, 60	þ
SSTL18_I	40, 50, 60	þ
SSTL18_II	40, 50, 60	þ
SSTL18D_I	40, 50, 60	þ
SSTL18D_II	40, 50, 60	þ
SSTL15	40, 50, 60	þ
SSTL15D	40, 50, 60	þ

1. TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature. Use of TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in

an I/O bank.

On-chip termination tolerance +/- 20%

2. External termination to VTT should be used when implementing DDR2 and DDR3 memory controller.



Please see TN1177, LatticeECP3 sysIO Usage Guide for on-chip termination usage and value ranges.

Equalization Filter

Equalization filtering is available for single-ended inputs on both true and complementary I/Os, and for differential inputs on the true I/Os on the left, right, and top sides. Equalization is required to compensate for the difficulty of sampling alternating logic transitions with a relatively slow slew rate. It is considered the most useful for the Input DDRX2 modes, used in DDR3 memory, LVDS, or TRLVDS signaling. Equalization filter acts as a tunable filter with settings to determine the level of correction. In the LatticeECP3 devices, there are four settings available: 0 (none), 1, 2 and 3. The default setting is 0. The equalization logic resides in the sysI/O buffers, the two bits of setting is set uniquely in each input IOLOGIC block. Therefore, each sysI/O can have a unique equalization setting within a DQS-12 group.

Hot Socketing

LatticeECP3 devices have been carefully designed to ensure predictable behavior during power-up and powerdown. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. Please refer to the Hot Socketing Specifications in the DC and Switching Characteristics in this data sheet.

SERDES and PCS (Physical Coding Sublayer)

LatticeECP3 devices feature up to 16 channels of embedded SERDES/PCS arranged in quads at the bottom of the devices supporting up to 3.2Gbps data rate. Figure 2-40 shows the position of the quad blocks for the LatticeECP3-150 devices. Table 2-14 shows the location of available SERDES Quads for all devices.

The LatticeECP3 SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express 1.1
- Ethernet (XAUI, GbE 1000 Base CS/SX/LX and SGMII)
- Serial RapidIO
- SMPTE SDI (3G, HD, SD)
- CPRI
- SONET/SDH (STS-3, STS-12, STS-48)

Each quad contains four dedicated SERDES for high speed, full duplex serial data transfer. Each quad also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in quads, multiple baud rates can be supported within a quad with the use of dedicated, per channel \div 1, \div 2 and \div 11 rate dividers. Additionally, multiple quads can be arranged together to form larger data pipes.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, please refer to TN1176, LatticeECP3 SERDES/PCS Usage Guide.

There are some restrictions to be aware of when using spread spectrum. When a quad shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the quad is compatible with all protocols within the quad. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LatticeECP3 architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, Serial RapidIO or SGMII channel within the same quad, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, Serial RapidIO and SGMII transmit jitter specifications.

For further information on SERDES, please see TN1176, LatticeECP3 SERDES/PCS Usage Guide.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Device Configuration

All LatticeECP3 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. The sysCONFIG port includes seven I/Os used as dedicated pins with the remaining pins used as dual-use pins. See TN1169, LatticeECP3 sysCONFIG Usage Guide for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure a LatticeECP3 device:

- 1. JTAG
- 2. Standard Serial Peripheral Interface (SPI and SPIm modes) interface to boot PROM memory
- 3. System microprocessor to drive a x8 CPU port (PCM mode)
- 4. System microprocessor to drive a serial slave SPI port (SSPI mode)
- 5. Generic byte wide flash with a MachXO[™] device, providing control and addressing

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

LatticeECP3 devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.



LatticeECP3 Supply Current (Standby)^{1, 2, 3, 4, 5, 6}

			Тур	Typical	
Symbol	Parameter	Device	-6L, -7L, -8L	-6, -7, -8	Units
		ECP-17EA	29.8	49.4	mA
		ECP3-35EA	53.7	89.4	mA
I _{CC}	Core Power Supply Current	ECP3-70EA	137.3	230.7	mA
		ECP3-95EA	137.3	230.7	mA
		ECP3-150EA	219.5	370.9	mA
		ECP-17EA	18.3	19.4	mA
		ECP3-35EA	19.6	23.1	mA
I _{CCAUX}	Auxiliary Power Supply Current	ECP3-70EA	26.5	32.4	mA
		ECP3-95EA	26.5	32.4	mA
		ECP3-150EA	37.0	45.7	mA
	PLL Power Supply Current (Per PLL)	ECP-17EA	0.0	0.0	mA
		ECP3-35EA	0.1	0.1	mA
ICCPLL		ECP3-70EA	0.1	0.1	mA
		ECP3-95EA	0.1	0.1	mA
		ECP3-150EA	0.1	0.1	mA
		ECP-17EA	1.3	1.4	mA
		ECP3-35EA	1.3	1.4	mA
I _{CCIO}	Bank Power Supply Current (Per Bank)	ECP3-70EA	1.4	1.5	mA
		ECP3-95EA	1.4	1.5	mA
		ECP3-150EA	1.4	1.5	mA
I _{CCJ}	JTAG Power Supply Current	All Devices	2.5	2.5	mA
		ECP-17EA	6.1	6.1	mA
		ECP3-35EA	6.1	6.1	mA
I _{CCA}	Iransmit, Receive, PLL and Reference Clock Buffer Power Supply	ECP3-70EA	18.3	18.3	mA
		ECP3-95EA	18.3	18.3	mA
		ECP3-150EA	24.4	24.4	mA

Over Recommended Operating Conditions

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{\mbox{CCIO}}$ or GND.

3. Frequency 0 MHz.

4. Pattern represents a "blank" configuration data file.

5. $T_J = 85$ °C, power supplies at nominal voltage.

6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool.



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

						6			
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
fMAX GDDB	DDRX1 Clock Frequency	ECP3-70EA/95EA		250		250	_	250	MHz
	Data Valid Before CLK	ECP3-35EA	683	—	688	_	690	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	683	_	688	_	690	_	ps
f _{MAX GDDR}	DDRX1 Clock Frequency	ECP3-35EA	_	250	_	250	_	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	683	—	688	_	690	_	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	683	—	688	—	690	—	ps
f _{MAX} GDDR	DDRX1 Clock Frequency	ECP3-17EA	_	250	_	250	—	250	MHz
Generic DDRX1 Ou	itput with Clock and Data Aligned	at Pin (GDDRX1_TX.	SCLK.Ali	gned) ¹⁰					
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-150EA	—	335	—	338	—	341	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-150EA		335	_	338	—	341	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA		250	_	250	—	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-70EA/95EA	_	339	_	343	_	347	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-70EA/95EA	_	339	_	343	_	347	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250	_	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-35EA	_	322	_	320	_	321	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-35EA	_	322	_	320	_	321	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	_	250	_	250	_	250	MHz
t _{DIBGDDR}	Data Invalid Before Clock	ECP3-17EA	_	322	_	320	_	321	ps
t _{DIAGDDR}	Data Invalid After Clock	ECP3-17EA	_	322	_	320	_	321	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA		250	_	250	—	250	MHz
Generic DDRX1 Ou	itput with Clock and Data (<10 Bi	ts Wide) Centered at P	in (GDD	RX1_TX.	DQS.Cen	tered) ¹⁰			
Left and Right Side	es								
t _{DVBGDDR}	Data Valid Before CLK	ECP3-150EA	670	_	670	—	670	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-150EA	670	—	670	—	670	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	_	250		250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-70EA/95EA	657	—	652	—	650	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-70EA/95EA	657	—	652	_	650	_	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70EA/95EA	_	250	_	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-35EA	670	—	675	—	676	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-35EA	670	—	675	_	676	_	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-35EA	_	250	_	250	—	250	MHz
t _{DVBGDDR}	Data Valid Before CLK	ECP3-17EA	670	—	670	—	670	—	ps
t _{DVAGDDR}	Data Valid After CLK	ECP3-17EA	670	—	670	—	670	—	ps
f _{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-17EA	_	250	_	250	—	250	MHz
Generic DDRX2 Ou	itput with Clock and Data (>10 Bi	ts Wide) Aligned at Pir	n (GDDR	X2_TX.A	igned)				
Left and Right Side	es								
t _{DIBGDDR}	Data Invalid Before Clock	All ECP3EA Devices		200		210		220	ps
t _{DIAGDDR}	Data Invalid After Clock	All ECP3EA Devices	_	200	_	210	_	220	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	500	_	420	—	375	MHz
Generic DDRX2 Ou	Itput with Clock and Data (>10 Bi	ts Wide) Centered at P	in Using		L (GDDF	X2_TX.D	QSDLL.	Centered)11
Left and Right Side	es								
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	400		400		431		ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	400		400	—	432		ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	400	_	400	—	375	MHz

Over Recommended Commercial Operating Conditions



LatticeECP3 External Switching Characteristics (Continued)^{1, 2, 3, 13}

Over Recommended Commercial	Operating Conditions
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			-	-8	-	-7	-	-6	
Parameter	Description	Device	Min.	Max.	Min.	Max.	Min.	Max.	Units
Generic DDRX2 Ou	tput with Clock and Data (>10 Bits	Wide) Centered at Pir	n Using I	PLL (GDI	DRX2_TX	.PLL.Cer	ntered) ¹⁰		
Left and Right Side	es								
t _{DVBGDDR}	Data Valid Before CLK	All ECP3EA Devices	285	—	370	_	431	—	ps
t _{DVAGDDR}	Data Valid After CLK	All ECP3EA Devices	285	—	370	_	432	—	ps
f _{MAX_GDDR}	DDRX2 Clock Frequency	All ECP3EA Devices	_	500	—	420	—	375	MHz
Memory Interface		•							
DDR/DDR2 I/O Pin	Parameters (Input Data are Strobe	Edge Aligned, Output	ut Strobe	e Edge is	Data Ce	ntered)4			
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	—	0.225		0.225		0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	—	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	_	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	_	UI
f _{MAX_DDR}	DDR Clock Frequency	All ECP3 Devices	95	200	95	200	95	166	MHz
f _{MAX_DDR2}	DDR2 clock frequency	All ECP3 Devices	125	266	125	200	125	166	MHz
DDR3 (Using PLL f	or SCLK) I/O Pin Parameters	•							
t _{DVADQ}	Data Valid After DQS (DDR Read)	All ECP3 Devices	_	0.225		0.225		0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	All ECP3 Devices	0.64	—	0.64	_	0.64	—	UI
t _{DQVBS}	Data Valid Before DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	—	UI
t _{DQVAS}	Data Valid After DQS	All ECP3 Devices	0.25	—	0.25	_	0.25	—	UI
f _{MAX_DDR3}	DDR3 clock frequency	All ECP3 Devices	300	400	266	333	266	300	MHz
DDR3 Clock Timing	9								
t _{CH} (avg) ⁹	Average High Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{CL} (avg) ⁹	Average Low Pulse Width	All ECP3 Devices	0.47	0.53	0.47	0.53	0.47	0.53	UI
t _{JIT} (per, lck) ⁹	Output Clock Period Jitter During DLL Locking Period	All ECP3 Devices	-90	90	-90	90	-90	90	ps
t _{JIT} (cc, lck) ⁹	Output Cycle-to-Cycle Period Jit- ter During DLL Locking Period	All ECP3 Devices	_	180	—	180	—	180	ps

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond or ispLEVER software.

2. General I/O timing numbers based on LVCMOS 2.5, 12mA, Fast Slew Rate, 0pf load.

3. Generic DDR timing numbers based on LVDS I/O.

4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.

5. DDR3 timing numbers based on SSTL15.

6. Uses LVDS I/O standard.

7. The current version of software does not support per bank skew numbers; this will be supported in a future release.

8. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.

9. Using settings generated by IPexpress.

10. These numbers are generated using best case PLL located in the center of the device.

11. Uses SSTL25 Class II Differential I/O Standard.

12. All numbers are generated with ispLEVER 8.1 software.

13. For details on -9 speed grade devices, please contact your Lattice Sales Representative.



Gigabit Ethernet/Serial Rapid I/O Type 1/SGMII/CPRI LV E.12 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-17. Transmit

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
T _{RF}	Differential rise/fall time	20%-80%	_	80		ps
Z _{TX_DIFF_DC}	Differential impedance		80	100	120	Ohms
J _{TX_DDJ} ^{3, 4, 5}	Output data deterministic jitter		_	—	0.10	UI
J _{TX_TJ} ^{2, 3, 4, 5}	Total output data jitter			_	0.24	UI

1. Rise and fall times measured with board trace, connector and approximately 2.5 pf load.

2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.

3. Jitter values are measured with each CML output AC coupled into a 50-Ohm impedance (100-Ohm differential impedance).

4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

5. Values are measured at 1.25 Gbps.

Table 3-18. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
RL _{RX_DIFF}	Differential return loss	From 100 MHz to 1.25 GHz	10			dB
RL _{RX_CM}	Common mode return loss	From 100 MHz to 1.25 GHz	6			dB
Z _{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J _{RX_DJ} ^{1, 2, 3, 4, 5}	Deterministic jitter tolerance (peak-to-peak)		_	_	0.34	UI
J _{RX_RJ} ^{1, 2, 3, 4, 5}	Random jitter tolerance (peak-to-peak)		-		0.26	UI
J _{RX_SJ} ^{1, 2, 3, 4, 5}	Sinusoidal jitter tolerance (peak-to-peak)		-		0.11	UI
J _{RX_TJ} ^{1, 2, 3, 4, 5}	Total jitter tolerance (peak-to-peak)		_	_	0.71	UI
T _{RX_EYE}	Receiver eye opening		0.29	_	_	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.

2. Jitter values are measured with each high-speed input AC coupled into a 50-Ohm impedance.

3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

5. Values are measured at 1.25 Gbps.



Point-to-Point LVDS (PPLVDS)

Over Recommended Operating Conditions

Description	Min.	Тур.	Max.	Units
Output driver supply $(1/-5\%)$	3.14	3.3	3.47	V
	2.25	2.5	2.75	V
Input differential voltage	100	—	400	mV
Input common mode voltage	0.2	—	2.3	V
Output differential voltage	130	—	400	mV
Output common mode voltage	0.5	0.8	1.4	V

RSDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Тур.	Max.	Units
V _{OD}	Output voltage, differential, R _T = 100 Ohms	100	200	600	mV
V _{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I _{RSDS}	Differential driver output current	1	2	6	mA
V _{THD}	Input voltage differential	100	—	-	mV
V _{CM}	Input common mode voltage	0.3	—	1.5	V
T _R , T _F	Output rise and fall times, 20% to 80%	—	500		ps
T _{ODUTY}	Output clock duty cycle	35	50	65	%

Note: Data is for 2 mA drive. Other differential driver current options are available.



Pin Information Summary (Cont.)

Pin Information Sun		ECP3-17EA		ECP3-35EA			
Pin Type	256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	
	Bank 0	13	10	18	13	21	24
	Bank 1	7	5	12	7	18	18
	Bank 2	2	2	4	1	8	8
Emulated Differential I/O per	Bank 3	4	2	13	5	20	19
Dank	Bank 6	5	1	13	6	22	20
	Bank 7	6	9	10	6	11	13
	Bank 8	12	12	12	12	12	12
	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	3	3	6	6
Highspeed Differential I/O per	Bank 3	5	4	9	4	9	12
Dank	Bank 6	5	4	9	4	11	12
	Bank 7	5	6	8	5	9	10
	Bank 8	0	0	0	0	0	0
	Bank 0	26/13	20/10	36/18	26/13	42/21	48/24
	Bank 1	14/7	10/5	24/12	14/7	36/18	36/18
	Bank 2	8/4	9/4	14/7	8/4	28/14	28/14
Differential I/O per Bank	Bank 3	18/9	12/6	44/22	18/9	58/29	63/31
	Bank 6	20/10	11/5	44/22	20/10	67/33	65/32
	Bank 7	23/11	30/15	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
	Bank 0	2	1	3	2	3	4
	Bank 1	1	0	2	1	3	3
	Bank 2	0	0	1	0	2	2
DDR Groups Bonded per	Bank 3	1	0	3	1	3	4
Bank ²	Bank 6	1	0	3	1	4	4
	Bank 7	1	2	2	1	3	3
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads	1	1	1	1	1	1	

These pins must remain floating on the board.
 Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.



Part Number	Voltage	Grade ¹	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6LFN672I	1.2 V	-6	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7LFN672I	1.2 V	-7	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8LFN672I	1.2 V	-8	LOW	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-6LFN1156I	1.2 V	-6	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7LFN1156I	1.2 V	-7	LOW	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8LFN1156I	1.2 V	-8	LOW	Lead-Free fpBGA	1156	IND	149

1. For ordering information on -9 speed grade devices, please contact your Lattice Sales Representative.

Part Number	Voltage	Grade	Power	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW ¹	1.2 V	-8	STD	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW ¹	1.2 V	-6	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW ¹	1.2 V	-7	STD	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW ¹	1.2 V	-8	STD	Lead-Free fpBGA	1156	IND	149

1. Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

• The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.

• The SERDES XRES pin on the TW device passes CDM testing at 250V.



Date	Version	Section	Change Summary
			Updated Frequency to 150 Mbps in Table 3-11 Periodic Receiver Jitter Tolerance Specification
December 2010	01.7EA	Multiple	Data sheet made final. Removed "preliminary" headings.
			Removed data for 70E and 95E devices. A separate data sheet is available for these specific devices.
			Updated for Lattice Diamond design software.
		Introduction	Corrected number of user I/Os
		Architecture	Corrected the package type in Table 2-14 Available SERDES Quad per LatticeECP3 Devices.
			Updated description of General Purpose PLL
			Added additional information in the Flexible Quad SERDES Architecture section.
			Added footnotes and corrected the information in Table 2-16 Selectable master Clock (MCCLK) Frequencies During Configuration (Nominal).
			Updated Figure 2-16, Per Region Secondary Clock Selection.
			Updated description for On-Chip Programmable Termination.
			Added information about number of rows of DSP slices.
			Updated footnote 2 for Table 2-12, On-Chip Termination Options for Input Modes.
			Updated information for sysIO buffer pairs.
			Corrected minimum number of General Purpose PLLs (was 4, now 2).
		DC and Switching Characteristics	Regenerated sysCONFIG Port Timing figure.
			Added ${\rm t}_{\rm W}$ (clock pulse width) in External Switching Characteristics table.
			Corrected units, revised and added data, and corrected footnote 1 in External Switching Characteristics table.
			Added Jitter Transfer figures in SERDES External Reference Clock section.
			Corrected capacitance information in the DC Electrical Characteristics table.
			Corrected data in the Register-to-Register Performance table.
			Corrected GDDR Parameter name HOGDDR.
			Corrected RSDS25 -7 data in Family Timing Adders table.
			Added footnotes 10-12 to DDR data information in the External Switch- ing Characteristics table.
			Corrected titles for Figures 3-7 (DDR/DDR2/DDR3 Parameters) and 3-8 (Generic DDR/DDRX2 Parameters).
			Updated titles for Figures 3-5 (MLVDS25 (Multipoint Low Voltage Differ- ential Signaling)) and 3-6 (Generic DDRX1/DDRX2 (With Clock and Data Edges Aligned)).
			Updated Supply Current table.
			Added GDDR interface information to the External Switching and Characteristics table.
			Added footnote to sysIO Recommended Operating Conditions table.
			Added footnote to LVDS25 table.
			Corrected DDR section footnotes and references.
			Corrected Hot Socketing support from "top and bottom banks" to "top and bottom I/O pins".
		Pinout Information	Updated description for VTTx.



Date	Version	Section	Change Summary
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
			Updated Device Configuration text section.
			Corrected software default value of MCCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
			Corrected footnote 2 in sysIO Recommended Operating Conditions table.
			Added added footnote 7 for t _{SKEW_PRIB} to External Switching Characteristics table.
			Added 2-to-1 Gearing text section and table.
			Updated External Reference Clock Specification (refclkp/refclkn) table.
			LatticeECP3 sysCONFIG Port Timing Specifications - updated t _{DINIT} information.
			Added sysCONFIG Port Timing waveform.
			Serial Input Data Specifications table, delete Typ data for $V_{RX-DIFF-S}$.
			Added footnote 4 to sysCLOCK PLL Timing table for t _{PFD} .
			Added SERDES/PCS Block Latency Breakdown table.
			External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.
			Added SERDES External Reference Clock Waveforms.
			Updated Serial Output Timing and Levels table.
			Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".
			Updated timing information
			Updated SERDES minimum frequency.
			Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Out- put Jitter, Typical Building Block Function Performance, Register-to- Register Performance, and Power Supply Requirements.
			Updated Serial Input Data Specifications table.
			Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables.
			Updated Pin Information Summary tables and added footnote 1.
February 2009	01.0	_	Initial release.