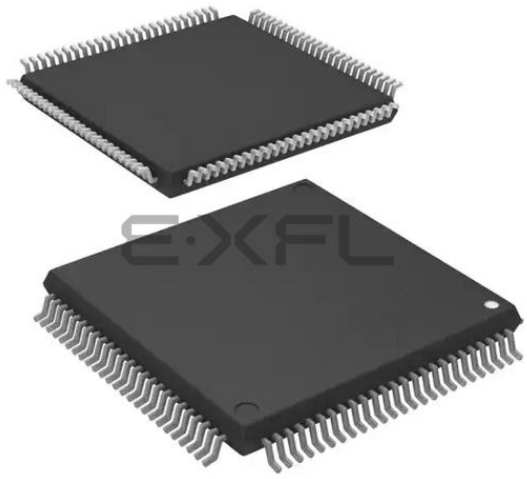
Renesas Electronics America Inc - R5F2L3A8CNFP#31 Datasheet



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Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	88
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l3a8cnfp-31

7.5.5 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCIOBSEL1	TRCIOBSEL0	—	—	—	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA pin select bit	0: TRCIOA pin not used 1: TRCIOA pin used	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	TRCIOBSEL0	TRCIOB pin select bit	b5 b4 0 0: TRCIOB pin not used 0 1: P4_5 assigned 1 0: P4_6 assigned 1 1: P4_7 assigned	R/W
b5	TRCIOBSEL1			R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

The TRCPSR0 register selects whether to use the timer RC input. To use the input pins for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation.

7.5.16 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT7SEL0	INT6SEL0	INT5SEL0	INT4SEL0	INT3SEL0	INT2SEL0	INT1SEL0	INT0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0SEL0	$\overline{\text{INT0}}$ pin select bit	0: P3_0 assigned 1: P11_0 assigned	R/W
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	0: P3_1 assigned 1: P11_1 assigned	R/W
b2	INT2SEL0	$\overline{\text{INT2}}$ pin select bit	0: P3_2 assigned 1: P11_2 assigned	R/W
b3	INT3SEL0	$\overline{\text{INT3}}$ pin select bit	0: P3_3 assigned 1: P11_3 assigned	R/W
b4	INT4SEL0	$\overline{\text{INT4}}$ pin select bit	0: P3_4 assigned 1: P11_4 assigned	R/W
b5	INT5SEL0	$\overline{\text{INT5}}$ pin select bit	0: P3_5 assigned 1: P11_5 assigned	R/W
b6	INT6SEL0	$\overline{\text{INT6}}$ pin select bit	0: P3_6 assigned 1: P11_6 assigned	R/W
b7	INT7SEL0	$\overline{\text{INT7}}$ pin select bit	0: P3_7 assigned 1: P11_7 assigned	R/W

The INTSR register selects which pin is assigned as the $\overline{\text{INTi}}$ (i = 0 to 7) input. To use the $\overline{\text{INTi}}$, set this register. Set the INTSR register before setting the $\overline{\text{INTi}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INTi}}$ operation.

11. Protection

The protection function protects important registers from being easily overwritten if a program runs out of control. The registers protected by the PRCR register are as follows:

- Registers protected by PRC0 bit: Registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3
- Registers protected by PRC1 bit: Registers PM0 and PM1
- Registers protected by PRC3 bit: Registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C

11.1 Register

11.1.1 Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	—	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled 1: Write enabled (1)	R/W
b1	PRC1	Protect bit 1	Enables writing to registers PM0 and PM1. 0: Write disabled 1: Write enabled (1)	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled 1: Write enabled (1)	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:

1. Bits PRC0, PRC1, and PRC3 are not set to 0 even after setting them to 1 (write enabled) and writing to the SFR areas. Set these bits to 0 by a program.

16.2.1 DTC Control Register j (DTCCRj) (j = 0 to 23)

Address See **Table 16.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	MODE	Transfer mode select bit	0: Normal mode 1: Repeat mode	R/W
b1	RPTSEL	Repeat area select bit (1)	0: Transfer destination is the repeat area. 1: Transfer source is the repeat area.	R/W
b2	SAMOD	Source address control bit (2)	0: Fixed 1: Incremented	R/W
b3	DAMOD	Destination address control bit (2)	0: Fixed 1: Incremented	R/W
b4	CHNE	Chain transfer enable bit (3)	0: Chain transfers disabled 1: Chain transfers enabled	R/W
b5	RPTINT	Repeat mode interrupt enable bit (1)	0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. This bit is valid when the MODE bit is 1 (repeat mode).
2. Settings of bits SAMOD and DAMOD are invalid for the repeat area.
3. Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

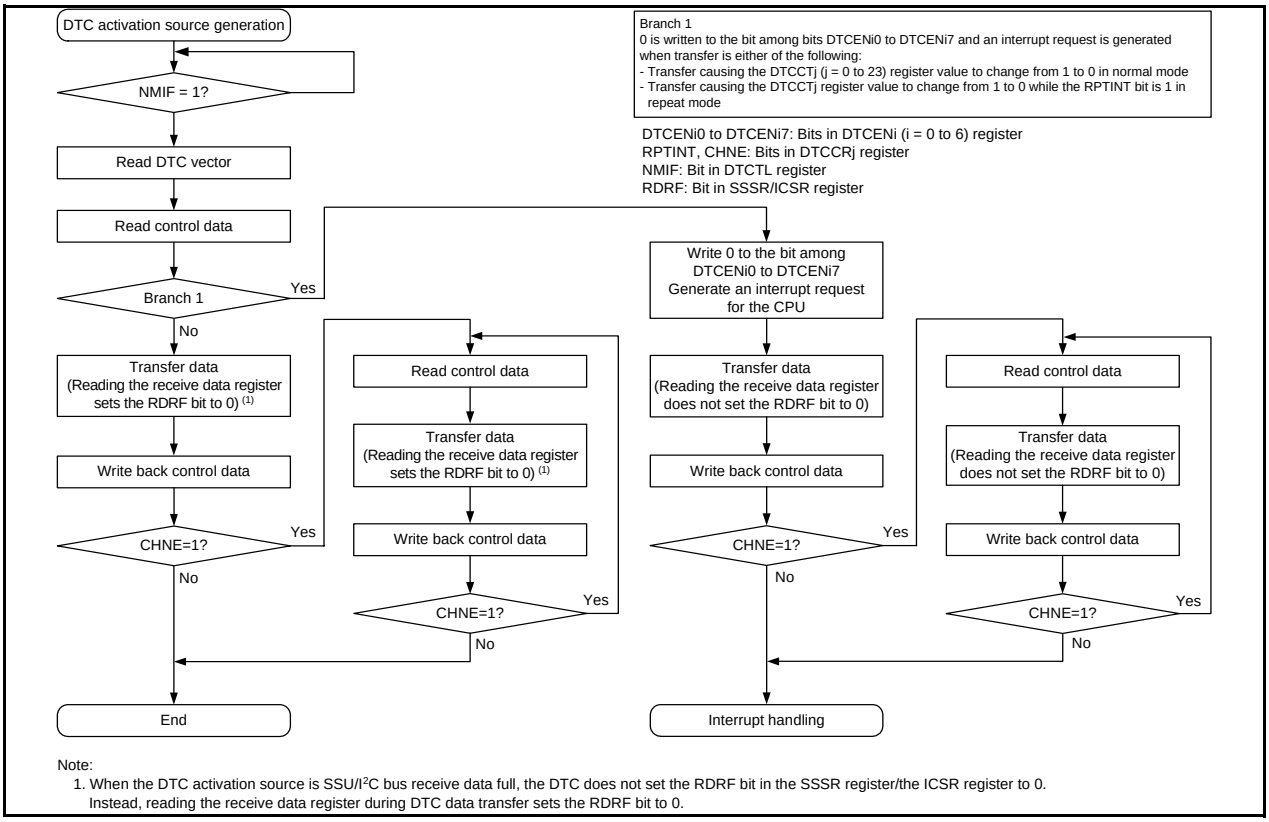
16.2.2 DTC Block Size Register j (DTBLSj) (j = 0 to 23)

Address See **Table 16.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

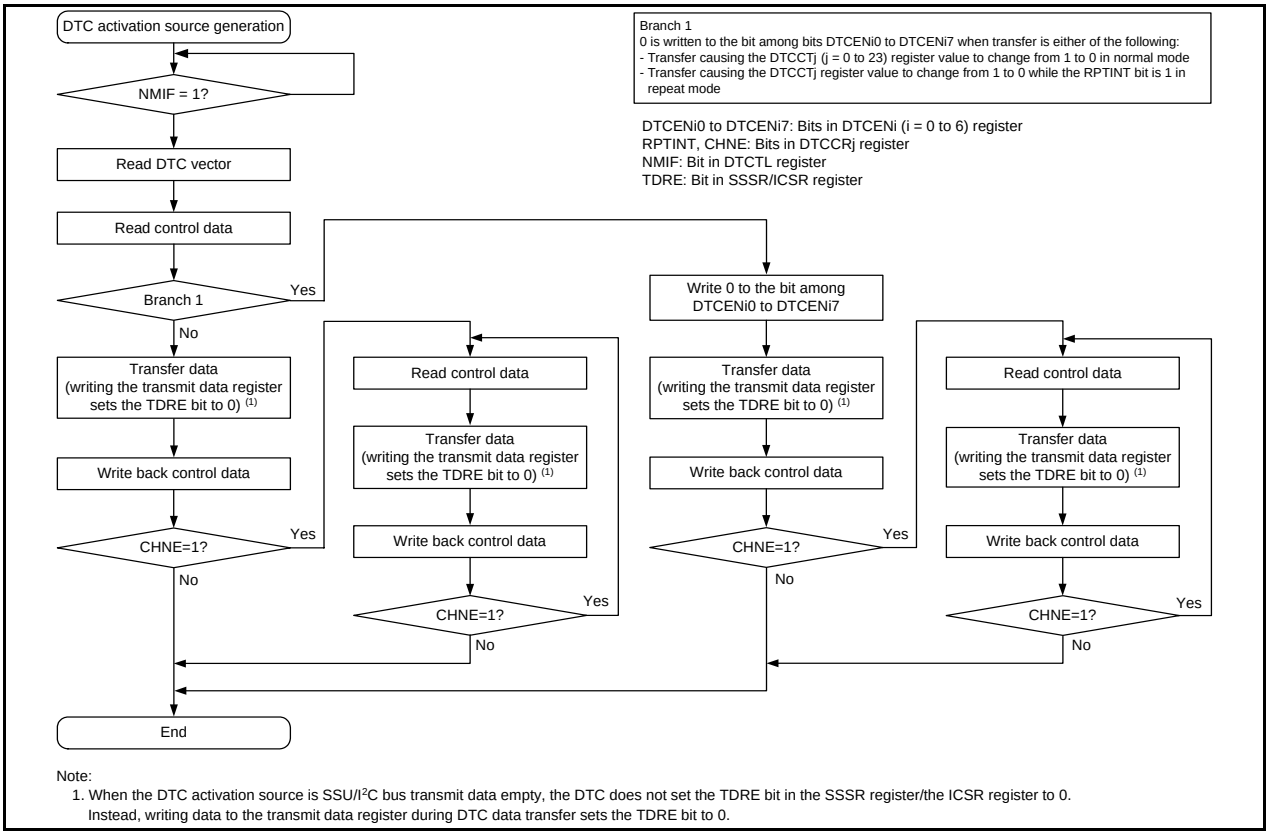
Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the size of the data block to be transferred by one activation.	00h to FFh (1)	R/W

Note:
1. When the DTBLS register is set to 00h, the block size is 256 bytes.



Note:
1. When the DTC activation source is SSU/I²C bus receive data full, the DTC does not set the RDRF bit in the SSSR register/the ICSR register to 0. Instead, reading the receive data register during DTC data transfer sets the RDRF bit to 0.

Figure 16.5 DTC Internal Operation Flowchart When DTC Activation Source is SSU/I²C bus Receive Data Full



Note:
1. When the DTC activation source is SSU/I²C bus transmit data empty, the DTC does not set the TDRE bit in the SSSR register/the ICSR register to 0. Instead, writing data to the transmit data register during DTC data transfer sets the TDRE bit to 0.

Figure 16.6 DTC Internal Operation Flowchart When DTC Activation Source is SSU/I²C bus Transmit Data Empty

21.4.11 Timer RD Control Register i (TRDCRi) (i = 0 or 1) for Output Compare Function

Address 0140h (TRDCR0), 0150h (TRDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) or fC2 (2) 1 1 0: fOCO40M 1 1 1: fOCO-F (5)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (3)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bit	b7 b6 b5 0 0 0: Clear disabled (free-running operation) 0 0 1: Clear by compare match with the TRDGRAi register 0 1 0: Clear by compare match with the TRDGRBi register 0 1 1: Synchronous clear (clear simultaneously with other timer RDi counter) (4) 1 0 0: Do not set. 1 0 1: Clear by compare match with the TRDGRCi register 1 1 0: Clear by compare match with the TRDGRDi register 1 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the ITCLKi bit in the TRDECR register is set to 0 (TRDCLK input) and the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. This setting is enabled when the ITCLKi bit in the TRDECR register is set to 1 (fC2) in timer mode.
3. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input or fC2), the ITCLKi bit in the TRDECR is set to 0 (TRDCLK input), and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
4. This setting is enabled when the SYNC bit in the TRDMR register is set to 1 (registers TRD0 and TRD1 operate synchronously).
5. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

21.4.21 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi

The TRDGRCi register can be used for output control of the TRDIOAi pin, and the TRDGRDi register can be used for output control of the TRDIOBi pin. Therefore, each pin output can be controlled as follows:

- TRDIOAi output is controlled by the values of registers TRDGRAi and TRDGRCi.
- TRDIOBi output is controlled by the values of registers TRDGRBi and TRDGRDi.

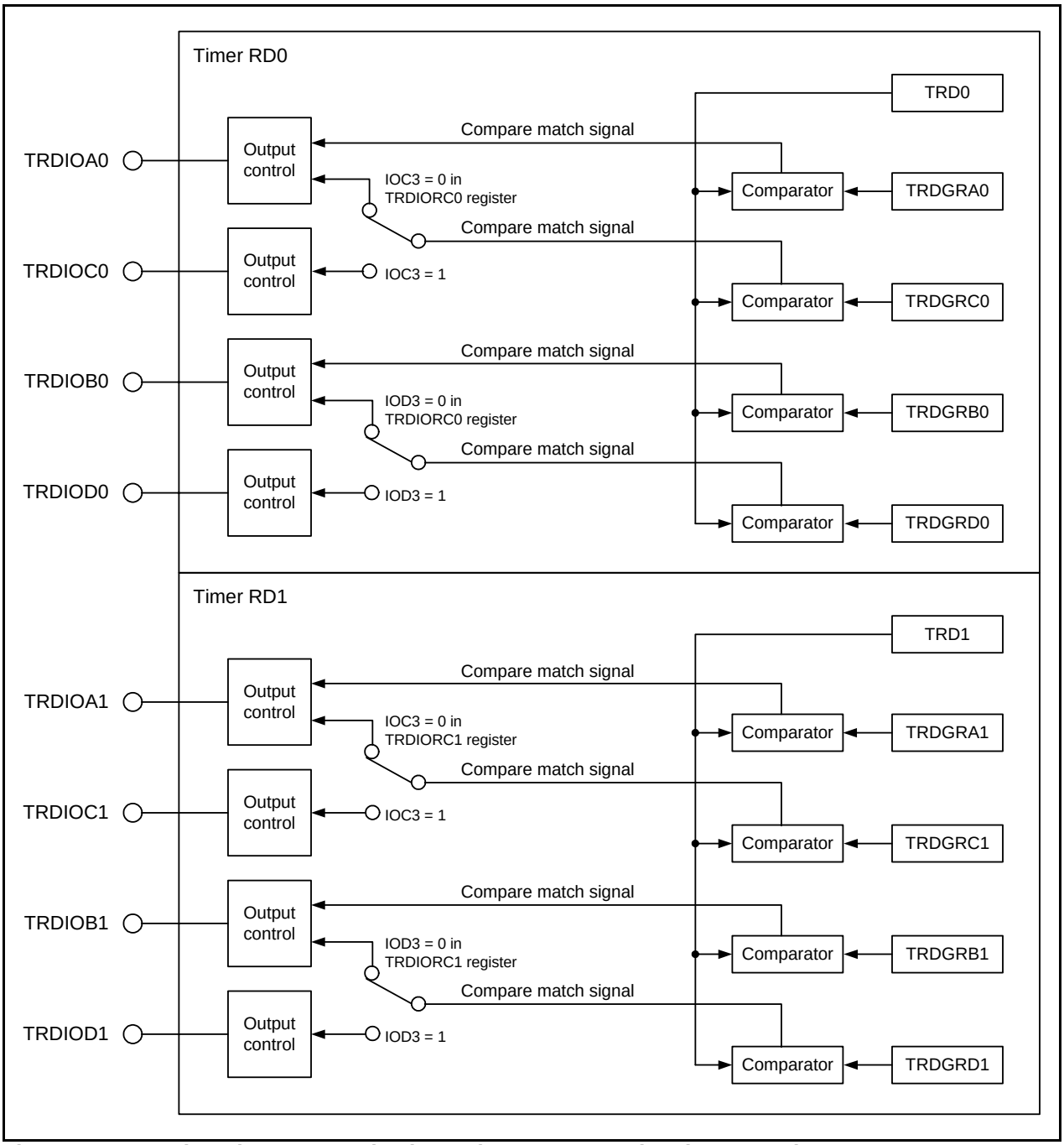


Figure 21.12 Changing Output Pins in Registers TRDGRCi and TRDGRDi

Change output pins in registers TRDGRCi and TRDGRDi as follows:

- Select 0 (change TRDGRji register output pin) by the IOj3 (j = C or D) bit in the TRDIORCi register.
- Set the BFji bit in the TRDMR register to 0 (general register).
- Set different values in registers TRDGRCi and TRDGRAi. Also, set different values in registers TRDGRDi and TRDGRBi.

21.5.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I^2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2, 3)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (4)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (5)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:

1. Stop the SSU and the I^2C bus functions before setting to standby. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I^2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. Stop the timer RD function before setting to standby. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0135h to 015Fh) is disabled.
3. To set the MSTTRD bit to 1 (standby), set bits TCK2 to TCK0 in the TRDCRi (i = 0 or 1) register to 000b (f1).
4. Stop the timer RC function before setting to standby. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
5. Stop the timer RG function before setting to standby. When the MSTTRG bit is set to 1 (standby), any access to the timer RG associated registers (addresses 0170h to 017Fh) is disabled.

21.6.17 A/D Trigger Generation

A compare match signal with registers TRDi (i = 0 or 1) and TRDGRji (j = A, B, C, or D) can be used as the conversion start trigger of the A/D converter.
The TRDADCR register is used to select which compare match is used.

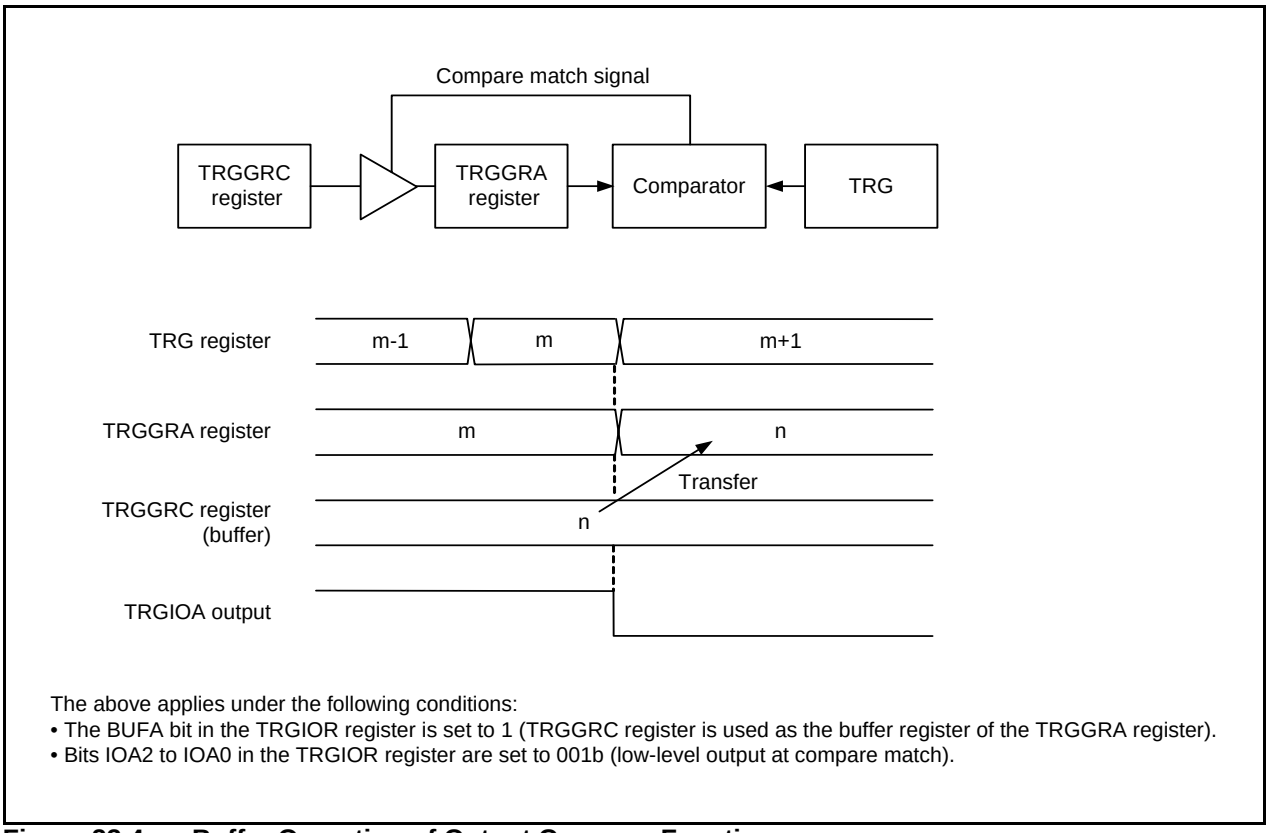


Figure 23.4 Buffer Operation of Output Compare Function

23.8 Timer RG Interrupt

Timer RG generates a timer RG interrupt request from four sources. The timer RG interrupt uses the single TRGIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 23.13 lists the Registers Associated with Timer RG Interrupt, and Figure 23.21 is a Block Diagram of Timer RG Interrupt.

Table 23.13 Registers Associated with Timer RG Interrupt

Timer RG Status Register	Timer RG Interrupt Enable Register	Timer RG Interrupt Control Register
TRGSR	TRGIER	TRGIC

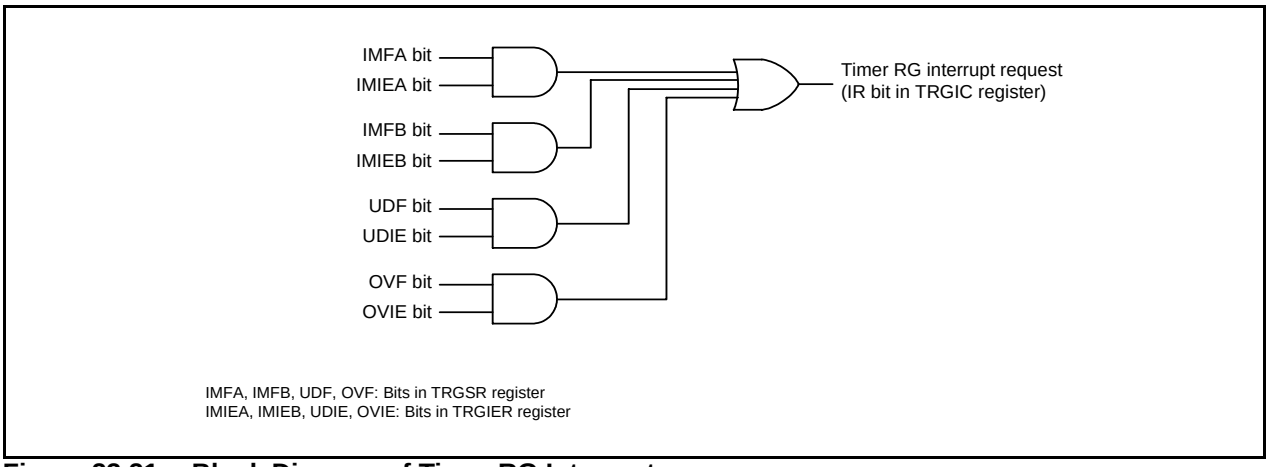


Figure 23.21 Block Diagram of Timer RG Interrupt

Like other maskable interrupts, the timer RG interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RG interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRGIC register is set to 1 (interrupt requested) when a bit in the TRGSR register is set to 1 and the corresponding bit in the TRGIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when either the bit in the TRGSR register or the corresponding bit in the TRGIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained even if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRGIER register are set to 1, use the TRGSR register to determine the source of the interrupt request.
- The bits in the TRGSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **23.2.5 Timer RG Status Register (TRGSR)**, for the procedure for setting these bits to 0.

Refer to **23.2.4 Timer RG Interrupt Enable Register (TRGIER)**, for details of the TRGIER register.
Refer to **12.3 Interrupt Control**, for details of the TRGIC register and **12.1.5.2 Relocatable Vector Tables**, for information on interrupt vectors.

Table 24.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode (1)

Register	Bit	Function
UiTB	b0 to b7	Set data transmission.
UiRB	b0 to b7	Receive data can be read.
	OER	Overrun error flag
UiBRG	b0 to b7	Set the transfer rate.
UiMR	SMD2 to SMD0	Set to 001b.
	CKDIR	Select an internal clock or external clock.
UiC0	CLK0, CLK1	Select the count source for the UiBRG register.
	TXEPT	Transmit register empty flag
	NCH	Select the output format of the TXDi pin.
	CKPOL	Select the transfer clock polarity.
	UFORM	Select LSB first or MSB first.
UiC1	TE	Set to 1 to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UiIRS	Select the UARTi transmit interrupt source.
	UiRRM	Set to 1 to use continuous receive mode.

i = 0 or 1

Note:

1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 25.11 Registers Used and Settings in I²C Mode (2)

Register	Bit	Function	
		Master	Slave
U2SMR4	STAREQ	Set to 1 to generate a start condition.	Set to 0.
	RSTAREQ	Set to 1 to generate a restart condition.	Set to 0.
	STPREQ	Set to 1 to generate a stop condition.	Set to 0.
	STSPSEL	Set to 1 to output each condition.	Set to 0.
	ACKD	Select ACK or NACK.	Select ACK or NACK.
	ACKC	Set to 1 to output ACK data.	Set to 1 to output ACK data.
	SCLHI	Set to 1 to stop SCL2 output when a stop condition is detected.	Set to 0.
	SWC9	Set to 0.	Set to 1 to hold SCL2 low at the falling edge of the 9th bit of clock.
URXDF	DF2EN	Set to 0.	Set to 0.
U2SMR5	MP	Set to 0.	Set to 0.

25.5.7 Initialization of Transmission/Reception

When a start condition is detected while the STAC bit is set to 1 (UART2 initialization enabled), the serial interface operates as described below.

- The transmit shift register is initialized, and the contents of the U2TB register are transferred to the transmit shift register. In this way, the serial interface starts sending data when the next clock pulse is applied. However, the UART2 output value does not change state and remains the same as when a start condition was detected until the first bit of data is output in synchronization with the input clock.
- The receive shift register is initialized, and the serial interface starts receiving data when the next clock pulse is applied.
- The SWC bit is set to 1 (SCL wait output enabled). Consequently, the SCL2 pin is pulled low at the falling edge of the 9th clock.

Note that when UART2 transmission/reception is started using this function, the TI bit does not change state. Select the external clock as the transfer clock to start UART2 transmission/reception with this setting.

29.4.2 Slave Mode

Figure 29.5 shows an Operating Example during Header Field Reception in slave mode. Figures 29.6 through 29.8 show examples of Header Field Reception Flowchart.
During header field reception, the hardware LIN operates as follows:

(1) When 1 is written to the LSTART bit in the LINCR register for the hardware LIN, Synch Break detection is enabled.
(2) When a low-level signal is input for a duration equal to or longer than the period set in timer RA, the hardware LIN detected it as a Synch Break. At this time, the SBDCT flag in the LINST register is set to 1. If the SBIE bit in the LINCR register is set to 1, a timer RA interrupt is generated. Then the hardware LIN transits to the Synch Field measurement.
(3) The hardware LINA receives a Synch Field (55h) and measures the period of the start bit and bits 0 to 6 is using timer RA. At this time, whether to input the Synch Field signal to RXD0 of UART0 can be selected by the SBE bit in the LINCR register.
(4) When the Synch Field measurement is completed, the SFDCT flag in the LINST register is set to 1. If the SFIE bit in the LINCR register is set to 1, a timer RA interrupt is generated.
(5) After the Synch Field measurement is completed, a transfer rate is calculated from the timer RA count value. The rate is set in UART0 and registers TRAPRE and TRA for timer RA are set again. Then the hardware LIN receives an ID field via UART0.
(6) After the hardware LIN completes receiving the ID field, it performs communication for a response field.

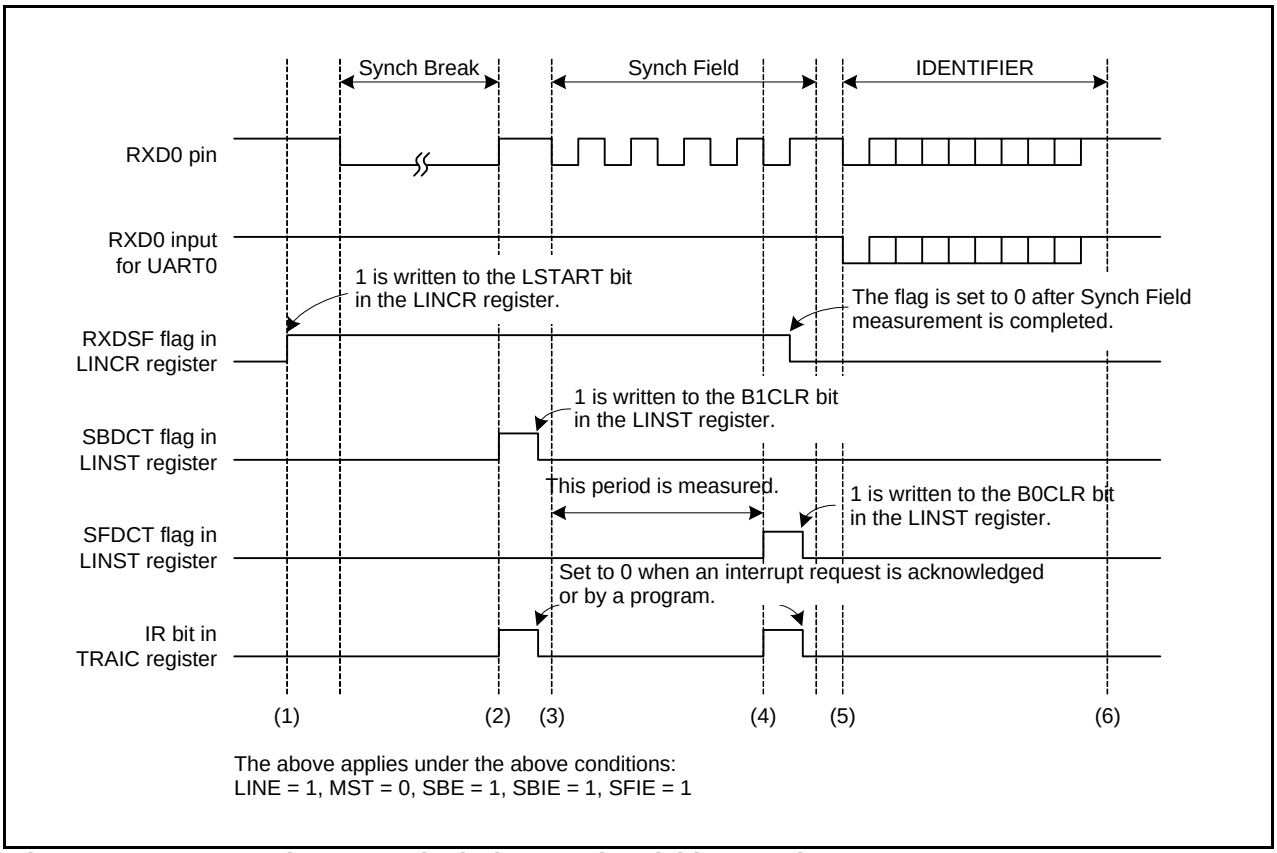


Figure 29.5 Operating Example during Header Field Reception

32.2 Registers

32.2.1 Comparator B Control Register 0 (INTCMP)

Address 01F8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3COUT	—	—	INT3CP0	INT1COUT	—	—	INT1CP0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT1CP0	Comparator B1 operation enable bit	0: Comparator B1 operation disabled 1: Comparator B1 operation enabled	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	INT1COUT	Comparator B1 monitor flag	0: IVCMP1 < IVREF1 or comparator B1 operation disabled 1: IVCMP1 > IVREF1	R
b4	INT3CP0	Comparator B3 operation enable bit	0: Comparator B3 operation disabled 1: Comparator B3 operation enabled	R/W
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	INT3COUT	Comparator B3 monitor flag	0: IVCMP3 < IVREF3 or comparator B3 operation disabled 1: IVCMP3 > IVREF3	R

32.2.2 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	INT2PL	INT2EN	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{\text{INT1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{\text{INT1}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT2EN	$\overline{\text{INT2}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{\text{INT2}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT3EN	$\overline{\text{INT3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{\text{INT3}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **12.8.4 Changing Interrupt Sources**.

33.4.1 Segment Output Pin Selection

All of the segment output pins SEG0 to SEG55 and common output pins COM0 to COM7 are shared with I/O ports. Since all these pins function as I/O ports after a reset, set the corresponding LSEi bit (i = 00 to 59) to 1 for the pins to be used as segment output and common output for LCD displays. Set the corresponding LSEi bit to 0 (I/O port) for the pins not to be used as segment output and common output. If these pins are not used as I/O ports, perform unassigned pin handling for I/O ports (refer to **Table 7.25 Unassigned Pin Handling**).

33.4.2 LCD Clock Selection

Either f32, f4 or fC-LCD is selected as the LCD clock source by setting bits LCKS0 and LCKS1. The division ratio is selected from a range of divide-by-1 to divide-by-64 by setting bits LPSC0 to LPSC2.

33.4.3 LCD Data Display Control

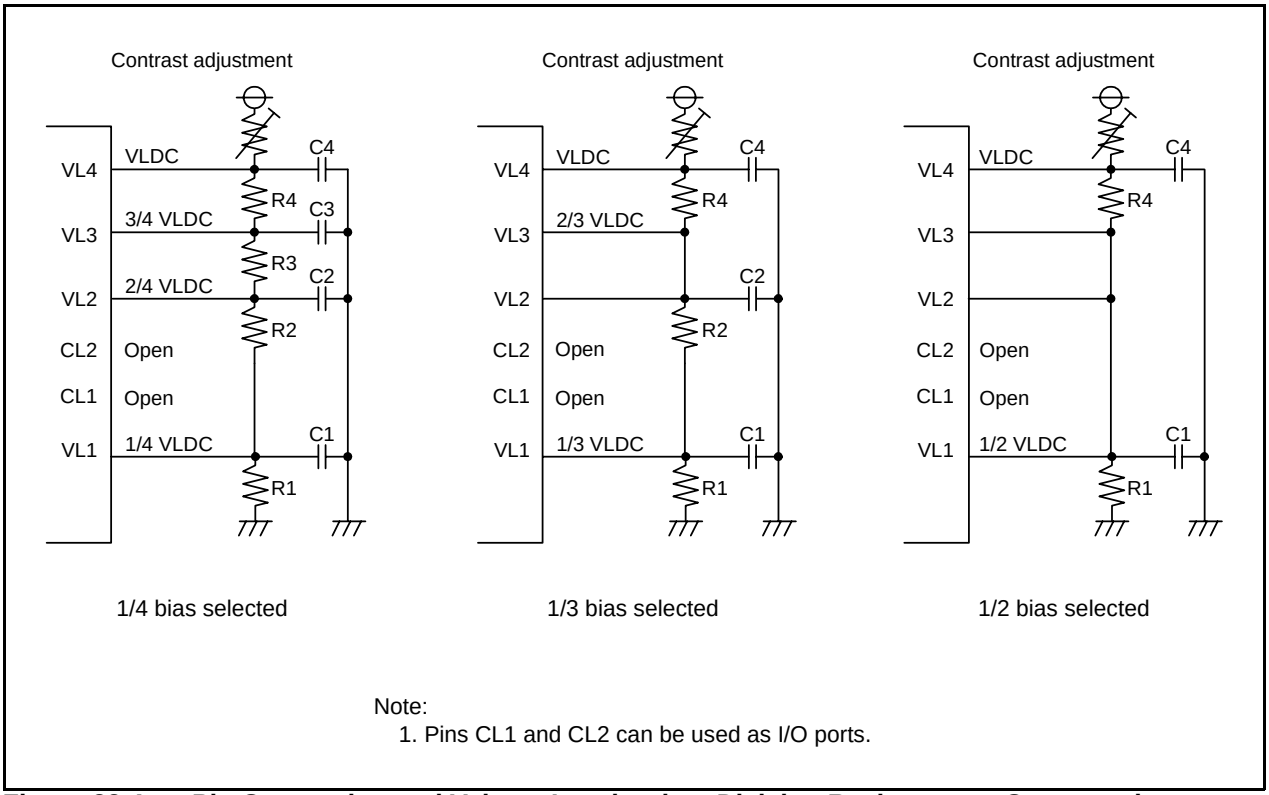
The LCD data display control function is used to blink or to invert an LCD display. This function is enabled by setting the LDSPC bit to 1. A display is blinked by setting the LRVRS bit to 0 and inverted by setting the bit to 1. The interval for blinking or inverting is selected by bits LDFR0 to LDFR2.

33.4.4 Bias Control

The bias is controlled by connecting external division resistors to LCD power supply pins VL1 to VL4 or by using the voltage multiplier. Figure 33.4 shows the Pin Connection and Voltage Levels when Division Resistors are Connected Externally. Figure 33.5 shows the Pin Connection and Voltage Levels when Voltage Multiplier is Used.

To connect division resistors externally, set the LVUPE bit to 0. Leave pins CL1 and CL2 open by setting the LSE60 bit to 1. These pins can also be used as I/O ports by setting the LSE60 bit to 0.

To use the voltage multiplier, set the LVUPE bit to 1. Select the reference voltage VL1 for the voltage multiplier to input externally or generate one internally by using the LVURS bit. Connect the voltage multiplier capacitor between pins CL1 and CL2. To generate the voltage internally, select the VL1 voltage value by setting bits LVLS0 to LVLS3. The wait time for the voltage multiplier is selected from the count source × 8 to count source × 64 using bits LVW0 and LVW1.



Note:
1. Pins CL1 and CL2 can be used as I/O ports.

Figure 33.4 Pin Connection and Voltage Levels when Division Resistors are Connected Externally

36. Usage Notes

36.1 Notes on Clock Generation Circuit

36.1.1 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 in the OCD register to 00b.

36.1.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

36.1.3 XCIN Clock

To use the XCIN clock, set the CM03 bit to 1 once and then set it to 0 (XCIN clock oscillates). To use the VL1 internally-generated voltage in the LCD drive control circuit, set the LVURS bit in the LCR1 register to 1 (VL1 internally-generated voltage) after the above setting.

36.1.4 Notes on Using Pins P12_0 and P12_1

The P12_0 pin is shared with the XIN pin, and the P12_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the XIN clock.

REVISION HISTORY	R8C/L35C Group, R8C/L36C Group, R8C/L38C Group, R8C/L3AC Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	May 25, 2010	727	34.4.3 b0 to b2 revised
		736	Table 34.5 revised, 34.4.11.1 revised
		737	34.4.11.3 revised, Figure 34.8 Note 1 revised
		738	Figure 34.9 revised
		753 to 754, 810 to 811	Tables 34.10 to 34.11 and Tables 36.3 to 36.4 "NMI" deleted
		756	Table 35.1 Note 2 added
		759	Table 35.3 "OCVREF" added
		766	Table 35.15 Note 3 added
		813	36.21.1 revised, 36.22 added
		816 to 819	Appendix 1 Package Dimensions revised
1.01	Mar 31, 2011	—	TN-R8C-A015A/E reflected
		—	TN-R8C-A016A/E reflected
		B-6, B-7	0248h to 026Fh, 02A8h to 02CFh revised
		2	Table 1.1 "Timer" revised
		3, 76	Table 1.2, Table 7.2 Note 2 revised
		3, 687	Table 1.3, Table 34.1 Note 1 revised
		6	Table 1.6 "Flash Memory" revised
		11 to 14	Figures 1.5 to 1.8 revised
		20 to 22	Tables 1.11 to 1.13 "Voltage Detection Circuit" deleted
		23, 24	Tables 1.14 and 1.15 title "for R8C/L3AC Group" added
		28	3. "The internal ROM ... with address 0FFFFh." deleted
		38 to 40	Tables 4.10 to 4.12 revised
		57	Table 6.1 "Voltage Monitor 0" revised
		63, 151	6.2.4, 10.2.6 Notes 1, 2, 3, 4 revised
		66, 67	6.2.7, 6.2.8 Note 2 revised
		80	Figure 7.3 "P12_1/XOUT" revised
		85, 246	7.5.3, 18.2.5 b2 to b7 revised
		95, 574, 605	7.5.14, 27.2.2, 28.2.2 b1 to b7 revised
		124	Table 9.1 Note 2 revised
		125	Figure 9.1 revised
		127, 146	9.2.1, 10.2.1 b1 and b2, Note 6 revised
		128, 147	9.2.2, 10.2.2 Notes 2 and 6 revised
		129, 148	9.2.3, 10.2.3 b2, Note 4 revised
		130, 149	9.2.4, 10.2.4 Note 4 revised
		139	9.6.4 revised
		142	Figure 9.5 title revised
		143, 779	9.8.1, 37.1.1 "bits OCD1 to OCD0 ..." → "bits OCD1 to OCD0 in the OCD register ..."
		144	Table 10.1 "Power-off mode" revised
		153	Table 10.2 revised, Notes 1 and 2 added
		154	10.3.2 revised
		155	10.4.2 revised, 10.4.3 added

Rev.	Date	Description	
		Page	Summary
1.01	Mar 31, 2011	675	30.9 revised
		676, 807	30.10, 37.18 "ADi register" → "ADi (i = 0 to 7) register"
		721	Table 34.3 "FMT5, and FMT4" → "FST5, and FST4", "Conditions for entering program-suspend" → "Conditions for entering erase-suspend"
		723	34.4.1 FST5 Bit: "auto-erase" → "auto-erasure"
		725	34.4.2 CMDRST Bit: "erase command" → "block erase command", "block erasure command" → "block erase command"
		737	34.4.11.3 "Block erase commands" → "Program commands"
		743	34.4.11.6 "... any address ..." → "... any block ..."
		744	Figure 34.18 "Write D0h to the starting block address" → "Write D0h to any block address", "This commanded is ..." → "This command is ..."
		745	Table 34.6 revised
		748	Figure 34.20 revised
		758	Table 35.3 "t_{CONV}", "t_{SAMP}" revised
		767, 769, 771	Tables 35.18, 35.20, 35.22 "High-Speed" → "High-Speed (fOCO-F)"
		813	37. (1) "on-ship debbugger" → "on-chip debbugger"