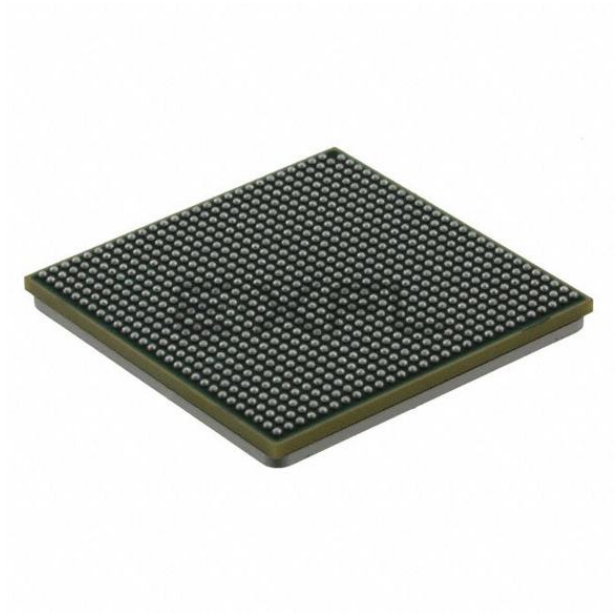

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR2, DDR3
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	Cryptography
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc8536eavtaqg

This table provides the pin-out listing for the 783 FC-PBGA package.

Table 1. Pinout Listing

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
PCI					
PCI1_AD[31:0]	Muxed Address / data	AB15,Y17,AA17,AC15, AB17,AC16,AA18, AD17,AE17,AB18, AB19,AE18,AC19, AF18,AE19,AC20, AF23,AE23,AC23, AH24,AH23,AG24, AE24,AG25,AD24, AG27,AC24,AF25, AG26,AF26,AE25, AD26	I/O	OV_{DD}	29
$\overline{\text{PCI1\_C\_BE[3:0]}}$	Command/Byte Enable	AD18, AD20,AD22, AH25	I/O	OV_{DD}	29
PCI1_PAR	Parity	AC22	I/O	OV_{DD}	29
$\overline{\text{PCI1\_FRAME}}$	Frame	AE20	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_TRDY}}$	Target Ready	AF21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_IRDY}}$	Initiator Ready	AB20	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_STOP}}$	Stop	AD21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_DEVSEL}}$	Device Select	AC21	I/O	OV_{DD}	2,29
PCI1_IDSEL	Init Device Select	AE16	I	OV_{DD}	29
$\overline{\text{PCI1\_PERR}}$	Parity Error	AB21	I/O	OV_{DD}	2,29
$\overline{\text{PCI1\_SERR}}$	System Error	AF22	I/O	OV_{DD}	2,4,29
$\overline{\text{PCI1\_REQ}}$[4:3]/GPIO[1:0]	Request	AE15,Y15	I	OV_{DD}	—
$\overline{\text{PCI1\_REQ}}$[2:1]	Request	AF13,W16	I	OV_{DD}	29
$\overline{\text{PCI1\_REQ}}$[0]	Request	AA16	I/O	OV_{DD}	29
$\overline{\text{PCI1\_GNT}}$[4:3]/GPIO[3:2]	Grant	AC14, AA15	O	OV_{DD}	—
$\overline{\text{PCI1\_GNT}}$[2:1]	Grant	AF14,Y16	O	OV_{DD}	5,9,25,29
$\overline{\text{PCI1\_GNT}}$[0]	Grant	W18	I/O	OV_{DD}	29
PCI1_CLK	PCI Clock	AH26	I	OV_{DD}	29

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
LAD[0:31]	Muxed data / address	K22,L21,L22,K23,K24, L24,L25,K25,L28,L27, K28,K27,J28,H28,H27, G27,G26,F28,F26,F25, E28,E27,E26,F24,E24, C26,G24,E23,G23,F22, G22,G21	I/O	BV_{DD}	5,9,29
LDP[0:3]	Data parity	K26,G28,B27,E25	I/O	BV_{DD}	29
LA[27]	Burst address	L19	O	BV_{DD}	5,9,29
LA[28:31]	Port address	K16,K17,H17,G17	O	BV_{DD}	5,7,9,29
$\overline{\text{LCS}}$[0:4]	Chip selects	K18,G19,H19,H20,G16	O	BV_{DD}	29
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	Chips selects / DMA Request	H16	I/O	BV_{DD}	1,29
$\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$	Chips selects / DMA Ack	J16	O	BV_{DD}	1,29
$\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$	Chips selects / DMA Done	L18	O	BV_{DD}	1,29
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/$\overline{\text{LFWE}}$	Write enable / Byte select	J22	O	BV_{DD}	5,9,29
$\overline{\text{LWE[1:3]}}$/$\overline{\text{LBS[1:3]}}$	Write enable / Byte select	H22,H23,H21	O	BV_{DD}	5,9,29
LBCTL	Buffer control	J25	O	BV_{DD}	5,8,9,29
LALE	Address latch enable	J26	O	BV_{DD}	5,8,9,29
LGPL0/LFCLE	UPM general purpose line 0 / FLash command latch enable	J20	O	BV_{DD}	5,9,29
LGPL1/LFALE	UPM general purpose line 1 / Flash address latch enable	K20	O	BV_{DD}	5,9,29
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM general purpose line 2 / Output enable/Flash read enable	G20	O	BV_{DD}	5,8,9,29
LGPL3/$\overline{\text{LFWP}}$	UPM general purpose line 3 / Flash write protect	H18	O	BV_{DD}	5,9,29
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT /LPBSE/LFRB	UPM general purpose line 4 / Target Ack/Wait/SDRAM parity byte select/Flash Ready-busy	L20	I/O	BV_{DD}	29, 33
LGPL5	UPM general purpose line 5 / Amux	K19	O	BV_{DD}	5,9,29
LCLK[0:2]	Local bus clock	H24,J24,H25	O	BV_{DD}	29
LSYNC_IN	Synchronization	D27	I	BV_{DD}	29
LSYNC_OUT	Local bus DLL	D28	O	BV_{DD}	29
DMA					
$\overline{\text{DMA\_DACK}}$[0:1] /GPIO[10:11]	DMA Acknowledge	AD6,AE10	O	OV_{DD}	—

Table 1. Pinout Listing (continued)

Signal	Signal Name	Package Pin Number	Pin Type	Power Supply	Notes
JTAG					
TCK	Test clock	AG28	I	OV_{DD}	—
TDI	Test data in	AH28	I	OV_{DD}	12
TDO	Test data out	AF28	O	OV_{DD}	11
TMS	Test mode select	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	Test reset	AH21	I	OV_{DD}	12
DFT					
L1_TSTCLK	L1 test clock	AA21	I	OV_{DD}	19
L2_TSTCLK	L2 test clock	AA20	I	OV_{DD}	19
$\overline{\text{LSSD\_MODE}}$	LSSD Mode	AC25	I	OV_{DD}	19
$\overline{\text{TEST\_SEL}}$	Test select	AA13	I	OV_{DD}	19
Power Management					
ASLEEP	Asleep	AG20	O	OV_{DD}	9,16,22
POWER_OK	Power OK	AC26	I	OV_{DD}	—
POWER_EN	Power enable	AE27	O	OV_{DD}	—
Power and Ground Signals					
OVDD	General I/O supply	Y18,AG2,AD4,AB16, AF6,AC18,AB13,AD10, AE14,AD16,AD25, AF27,AE22,AF11, AF20,AF24	—	OV_{DD}	—
LVDD	GMAC 1 I/O supply	AA7, AA4	Power for TSEC1 interfaces	LV_{DD}	—
TVDD	GMAC 3 I/O supply	V4,U7	Power for TSEC3 interfaces	TV_{DD}	—
GVDD	SSTL2 DDR supply	B1,B11,C7,C9,C14, C17,D4,D6,R3,D15,E2, E8,C24,E18,F5,E14, C21,G3,G7,G9,G11, H5,H12,E22,F15,J10, K3,K12,K14,H14,D20, E11,M1,N5	Power for DDR DRAM I/O	GV_{DD}	—
BVDD	Local bus I/O supply	L23,J18,J23,J19,F20, F23,H26,J21	Power for Local Bus	BV_{DD}	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Core power supply for SerDes transceivers		SV_{DD}	1.0 ± 50 mV	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}	1.0 ± 50 mV	V	—
DDR SDRAM Controller I/O supply voltage	DDR2 SDRAM Interface	GV_{DD}	1.8 V ± 90 mV	V	3
	DDR3 SDRAM Interface		1.5 V ± 75 mV		
Three-speed Ethernet I/O voltage		LV_{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	5
		TV_{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, system control and power management, I^2C, USB, eSDHC, eSPI and JTAG I/O voltage, MII management voltage		OV_{DD}	3.3 V ± 165 mV	V	4
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2 and DDR3 SDRAM Interface signals	MV_{IN}	GND to GV_{DD}	V	3
	DDR2 and DDR3 SDRAM Interface reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	5
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	PCI, Local bus, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	4
Operating Temperature range	Commercial	T_A T_J	T_A= 0 (min) to T_J= 90(max)	°C	6
	Industrial standard temperature range		T_A= 0 (min) to T_J= 105 (max)		
	Extended temperature range		T_A= -40 (min) to T_J= 105 (max)		

Notes:

1. VDD = 1.0 V for 600 to 1333 MHz, 1.1 V for 1500 MHz,
2. This voltage is the input to the filter discussed in Section 3.2.1, "PLL Power Supply Filtering," and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.
3. **Caution**: MVIN must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution**: OVIN must not exceed OVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution**: L/TVIN must not exceed L/TVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.

2.3 Power Characteristics

The estimated power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III chips is shown in the following table.

Table 5. Power Dissipation [5]

Power Mode	Core Frequency	CCB Frequency	DDR Frequency	V_{DD} Platform	V_{DD} Core [5]	Junction Temperature	Core Power		Platform Power[9]		Notes
	(MHz)	(MHz)	(MHz)	(V)	(V)	(°C)	mean[7]	Max	mean[7]	Max	
Maximum (A)	600	400	400	1.0	1.0	105 /90	—	4.1/3.3	—	4.7/3.7	1, 3, 8
Thermal (W)							—	3.7/2.9	—	4.7/3.7	1, 4, 8
Typical (W)						65	1.5	—	1.5	—	1, 2
Doze (W)							1.2	1.9	1.4	1.9	1
Nap (W)							0.8	1.5	1.4	1.9	1
Sleep (W)							0.8	1.5	1.0	1.6	1
Deep Sleep (W)						35	0	0	0.6	1.1	6
Maximum (A)	800	400	400	1.0	1.0	105 / 90	—	4.5/3.7	—	4.7/3.7	1, 3, 8
Thermal (W)							—	3.9/3.1	—	4.7/3.7	1, 4, 8
Typical (W)						65	1.7	—	1.5	—	1, 2
Doze (W)							1.3	2.1	1.4	1.9	1
Nap (W)							0.8	1.5	1.4	1.9	1
Sleep (W)							0.8	1.5	1.0	1.6	1
Deep Sleep (W)						35	0	0	0.6	1.1	1,6
Maximum (A)	1000	400	400	1.0	1.0	105 / 90	—	4.8/4.0	—	4.7/3.7	1, 3, 8
Thermal (W)							—	4.1/3.3	—	4.7/3.7	1, 4, 8
Typical (W)						65	1.9	—	1.5	—	1, 2
Doze (W)							1.4	2.2	1.4	1.9	1
Nap (W)							0.8	1.6	1.4	1.9	1
Sleep (W)							0.8	1.6	1.0	1.6	1
Deep Sleep (W)						35	0	0	0.6	1.1	1, 6

Table 5. Power Dissipation (continued)[5]

Power Mode	Core Frequency (MHz)	CCB Frequency (MHz)	DDR Frequency (MHz)	V_{DD} Platform (V)	V_{DD} Core [5] (V)	Junction Temperature (°C)	Core Power mean[7]	Core Power Max	Platform Power[9] mean[7]	Platform Power[9] Max	Notes
Maximum (A)	1250	500	500	1.0	1.0	105 / 90	—	5.3/4.4	—	5.0/4.0	1, 3, 8
Thermal (W)							—	4.4/3.6	—	5.0/4.0	1, 4, 8
Typical (W)						65	2.2		1.7		1
Doze (W)							1.6	2.4	1.5	2.1	1
Nap (W)							0.8	1.6	1.5	2.1	1
Sleep (W)							0.8	1.6	1.1	1.7	1
Deep Sleep (W)						35	0	0	0.6	1.2	1, 6
Maximum (A)	1333	533	667	1.0	1.0	105 / 90	—	5.4/4.6	—	5.2/4.1	1, 3, 8
Thermal (W)							—	4.5/3.7	—	5.2/4.1	1, 4, 8
Typical (W)						65	2.3		1.8	—	1, 2
Doze (W)							1.7	2.5	1.6	2.1	1
Nap (W)							0.8	1.6	1.6	2.1	1
Sleep (W)							0.8	1.6	1.2	1.7	1
Deep Sleep (W)						35	0	0	0.6	1.2	1, 6

This table provides the DDR capacitance when GV_{DD}(type) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V (for DDR2), f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.
2. This parameter is sampled. GV_{DD} = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.175 V.

This table provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter/Condition		Symbol	Min	Max	Unit	Note
Current draw for $MV_{REF}n$	DDR2 SDRAM	I_{MVREFn}	—	1500	μA	1
	DDR3 SDRAM			1250		

1.The voltage regulator for MV_{REF} must be able to supply up to 1500 μA or 1250 uA current for DDR2 or DDR3 respectively.

2.6.2 DDR2 and DDR3 SDRAM Interface AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM Controller interface. The DDR controller supports both DDR2 and DDR3 memories. Please note that although the minimum data rate for most off-the-shelf DDR3 DIMMs available is 800 MHz, JEDEC specification does allow the DDR3 to run at the data rate as low as 606 MHz. Unless otherwise specified, the AC timing specifications described in this section for DDR3 is applicable for data rate between 606 MHz and 667 MHz, as long as the DC and AC specifications of the DDR3 memory to be used are compliant to both JEDEC specifications as well as the specifications and requirements described in this document.

2.6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

These tables provide the input AC timing specifications for the DDR controller.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%

Parameter		Symbol	Min	Max	Unit
AC input low voltage	667	V_{ILAC}	—	MV_{REF} – 0.20	V
	<=533		—	MV_{REF} – 0.25	V
AC input high voltage	667	V_{IHAC}	MV_{REF} + 0.20	—	V
	<=533		MV_{REF} + 0.25	—	V

Table 19. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol [1]	Min	Max	Unit	Notes
<= 667 MHz		$0.9 \times t_{MCK}$			7
MDQS epilogue end	t_{DDKHME}			ns	6
<= 667 MHz		$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$		7

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR2 and DDR3 frequency is 667 MHz

NOTE

For the ADDR/CMD setup and hold specifications in Table 19, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

2.8 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the chip.

2.8.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.8.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	2
Maximum baud rate	CCB clock/16	baud	2,3
Oversample rate	16	—	4

Notes:

2. CCB clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

2.9 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

When operating in SGMII mode, the eTSEC EC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ pins.

2.9.3.1 DC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.20, "High-Speed Serial Interfaces."

2.9.3.2 AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Please note that SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 38. SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10 (8)	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	2,3

Notes:

1. 8 ns applies only when 125 MHz SerDes2 reference clock frequency is selected via cfg_srds_sgmii_refclk during POR.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10E-12.
3. Total peak-to-peak deterministic jitter "Dj" should be less than or equal to 50 ps.

2.9.3.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 31 shows the SGMII Receiver Input Compliance Mask eye diagram.

Table 42. SGMII Receive AC Timing Specifications

At recommended operating conditions with $X2V_{DD}$ = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal Jitter Tolerance	JSIN	0.1	—	—	UI p-p	1
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	2
AC Coupling Capacitor	C_{TX}	5	—	200	nF	3

Notes:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the chip transmitter outputs.

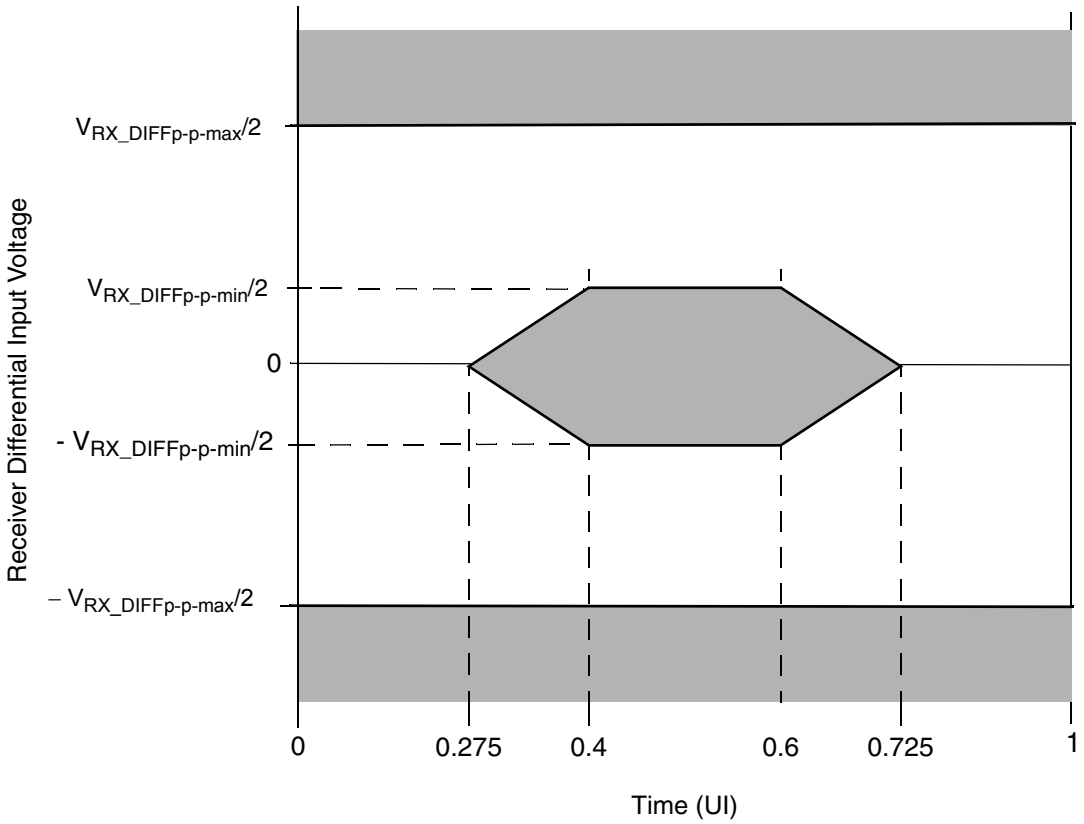


Figure 31. SGMII Receiver Input Compliance Mask

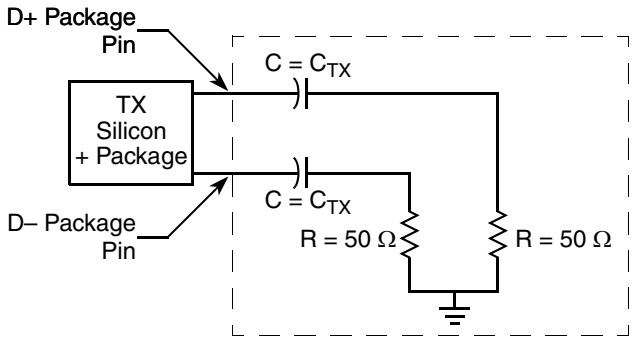


Figure 32. SGMII AC Test/Measurement Load

2.9.4 eTSEC IEEE 1588 AC Specifications

This figure shows the data and command output timing diagram.

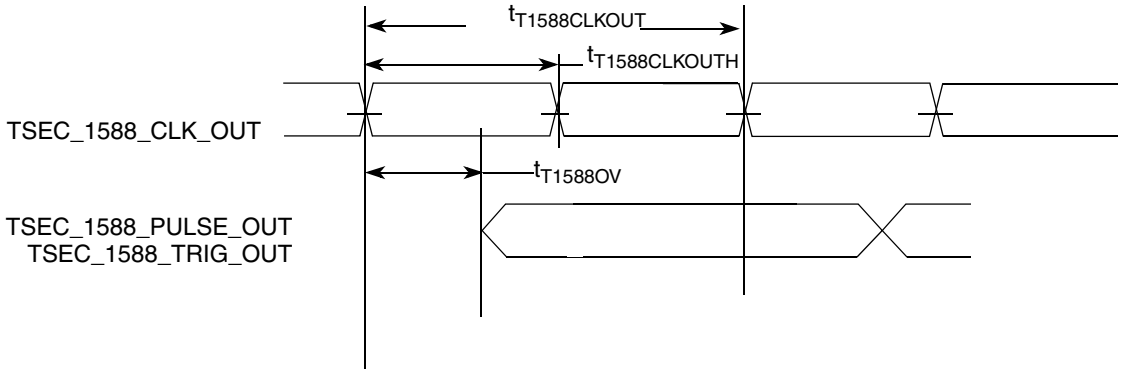


Figure 33. eTSEC IEEE 1588 Output AC timing

[1] The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

This figure provides the data and command input timing diagram.

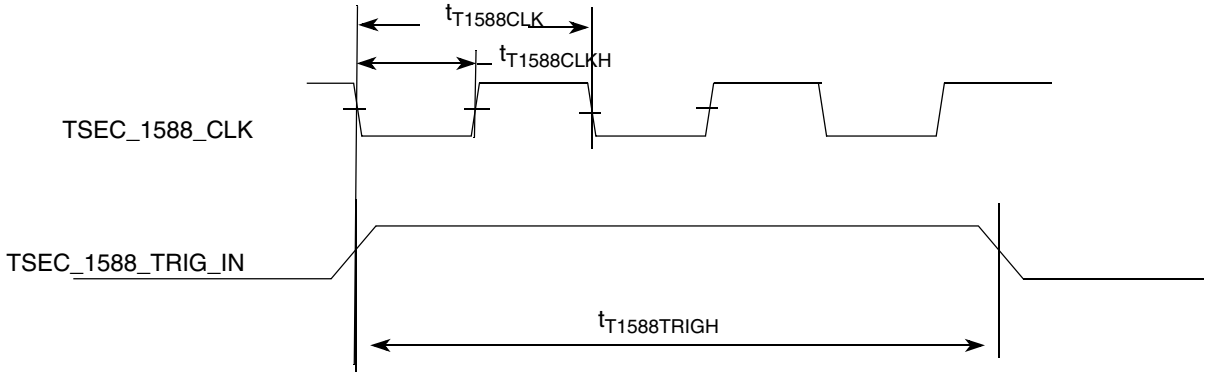


Figure 34. eTSEC IEEE 1588 Input AC timing

Table 45. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OVDD is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
EC_MDIO to EC_MDC hold time	t_{MDDXKH}	0	—	—	ns	—
EC_MDC rise time	t_{MDCR}	—	—	10	ns	—
EC_MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual EC_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of chip's MIIMCFG register, based on the platform (CCB) clock running for the chip. The formula is: Platform Frequency (CCB)/(2*Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f_{MDC} = 533/(2*4*8) = 533/64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f_{CCB}), the EC_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB}/64$ and minimum $f_{MDC} = f_{CCB}/448$. See the MPC8536E reference manual's MIIMCFG register section for more detail.
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods +/-3ns. For example, with a platform clock of 333MHz, the min/max delay is 48ns +/-3ns. Similarly, if the platform clock is 400MHz, the min/max delay is 40ns +/-3ns).
5. t_{CLKplb_clk} is the platform (CCB) clock
6. EC_MDC to EC_MDIO Data valid t_{MDKHDV} is a function of clock period and max delay time t_{MDKHDX}. (Min Setup = Cycle time - Max Hold)

This figure shows the MII management AC timing diagram.

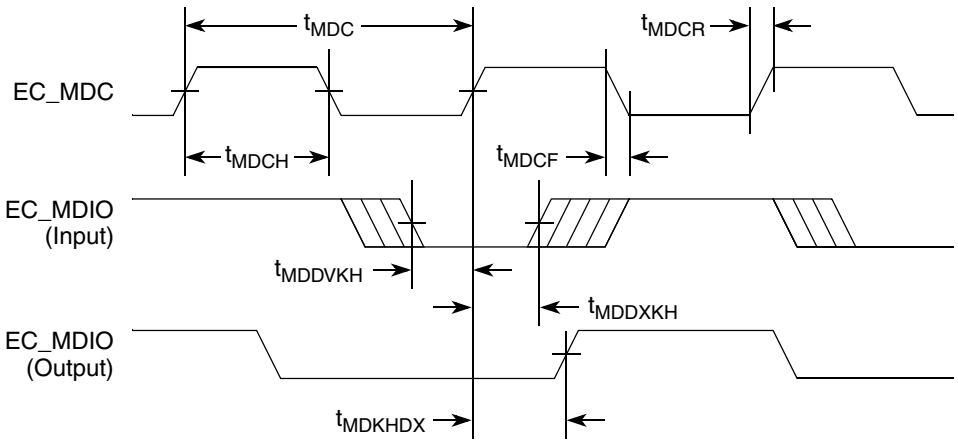


Figure 35. MII Management Interface Timing Diagram

2.11 USB

This section provides the AC and DC electrical specifications for the USB interface of the chip.

Table 64. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 63).

Parameter	Symbol [1]	Min	Max	Unit	Notes
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When the chip acts as the I²C bus master while transmitting, the chip drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. For details of the I²C frequency calculation, refer to *Determining the I²C Frequency Divider Ratio for SCL* (AN2919). Note that the I²C Source Clock Frequency is half of the CCB clock frequency for the chip.
3. The maximum t_{I2DVKH} has only to be met if the chip does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

This figure provides the AC test load for the I²C.

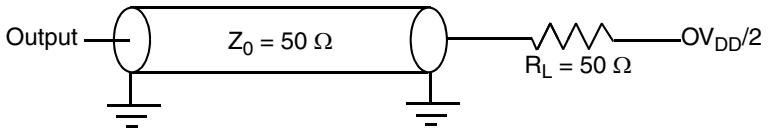


Figure 51. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

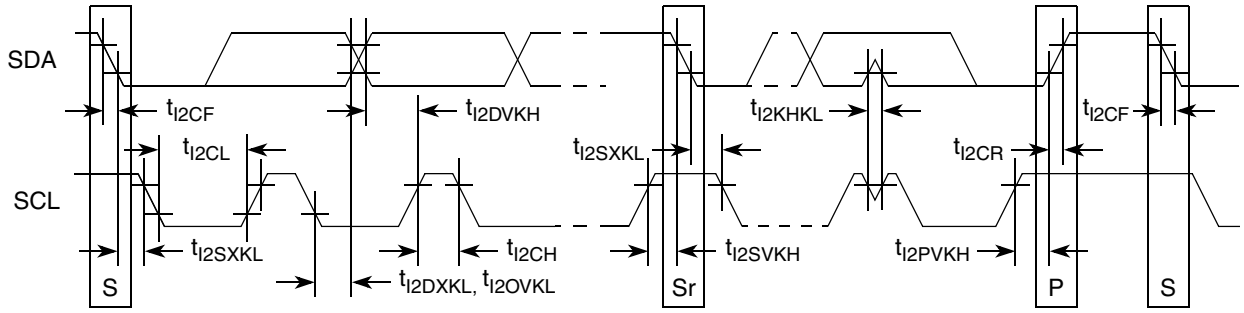


Figure 52. I²C Bus AC Timing Diagram

2.19 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the chip.

2.19.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 67. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [2] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

2.19.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. This table provides the PCI AC timing specifications at 66 MHz.

Table 68. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4
Input setup to SYSCLK	t_{PCIVKH}	3.0	—	ns	2, 5
Input hold from SYSCLK	t_{PCIXKH}	0	—	ns	2, 5
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	10 × t_{SYS}	—	clocks	6, 7
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	7

2.20.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the chip's SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400mV and 1600mV differential peak-peak (or between 200mV and 800mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800mV and greater than 200mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 2.20.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 59 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SnGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SnGND). Figure 60 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SDn_REF_CLK input amplitude (single-ended swing) must be between 400mV and 800mV peak-peak (from Vmin to Vmax) with $\overline{\text{SDn\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SDn_REF_CLK input average voltage must be between 200 and 400 mV. Figure 61 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SDn\_REF\_CLK}}$) through the same source impedance as the clock input (SDn_REF_CLK) in use.

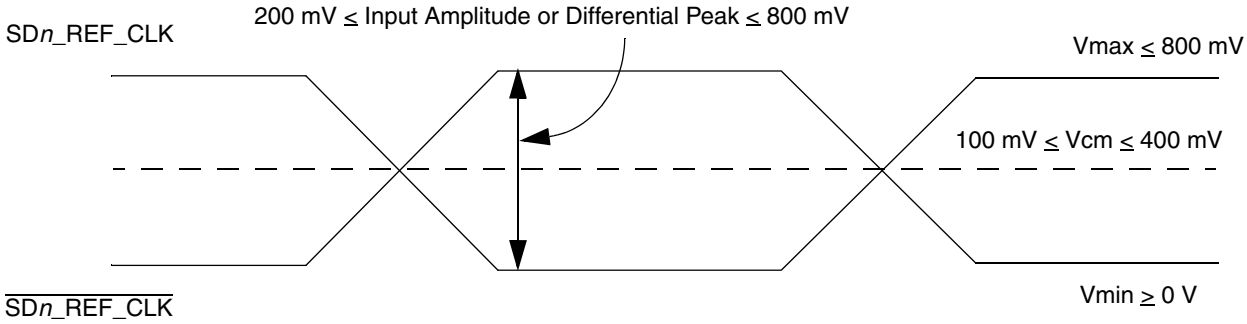


Figure 59. Differential Reference Clock Input DC Requirements (External DC-Coupled)

2.24.1 Thermal Characteristics

This table provides the package thermal characteristics.

Table 79. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	23	°C/W	1, 2
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	18	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JA}$	18	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JA}$	14	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	10	°C/W	3
Junction-to-case thermal	—	$R_{\theta JC}$	< 0.1	°C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 °C/W

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.For system thermal modeling, the chip's thermal model without a lid is shown in Figure 72 The substrate is modeled as a block 29 x 29 x 1.2 mm with an in-plane conductivity of 19.8 W/m•K and a through-plane conductivity of 1.13 W/m•K. The solder balls and air are modeled as a single block 29 x 29 x 0.5 mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 9.6 x 9.57 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 7.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

2.24.2 Recommended Thermal Model

This table shows the chip's thermal model.

Table 80. Thermal Model

Conductivity	Value	Units
Die (9.6x9.6 × 0.85 mm)		
Silicon	Temperature dependent	—
Bump/Underfill (9.6 x 9.6 × 0.07 mm) Collapsed Thermal Resistance		
Kz	7.5	W/m•K
Substrate (29 × 29 × 1.2 mm)		
Kx	19.8	W/m•K
Ky	19.8	
Kz	1.13	

This figure shows the PLL power supply filter circuit.

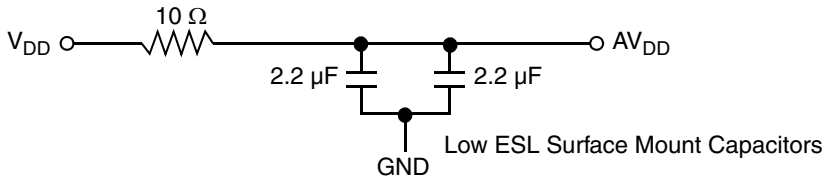
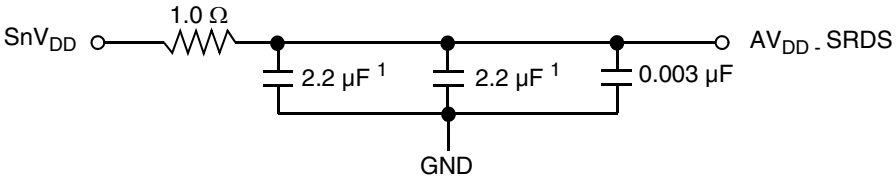


Figure 75. Chip PLL Power Supply Filter Circuit

The AV_{DD}_SRDS*n* signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 76. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS*n* balls. The 0.003-µF capacitor is closest to the balls, followed by the 1-µF capacitor, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up

Figure 76. SerDes PLL Power Supply Filter Circuit

Note the following:

- AV_{DD} should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

3.3 Pin States in Deep Sleep State

In all low power mode by default, all input and output pads remain driven as per normal functional operation. The inputs remain enabled.

The exception is that in Deep Sleep mode, GCR[DEEPSLEEP_Z] can be used to tristate a subset of output pads, and disable the receivers of input pads as defined in Table 1. See the *MPC8536E PowerQUICC III Integrated Processor Reference Manual* for details.

3.4 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, this chip can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the chip. These decoupling capacitors should receive their power from separate V_{DD},TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors must be placed directly under the chip using a standard escape pattern as much as possible. If some caps are to be placed surrounding the part it should be routed with short and large trace to minimize the inductance.

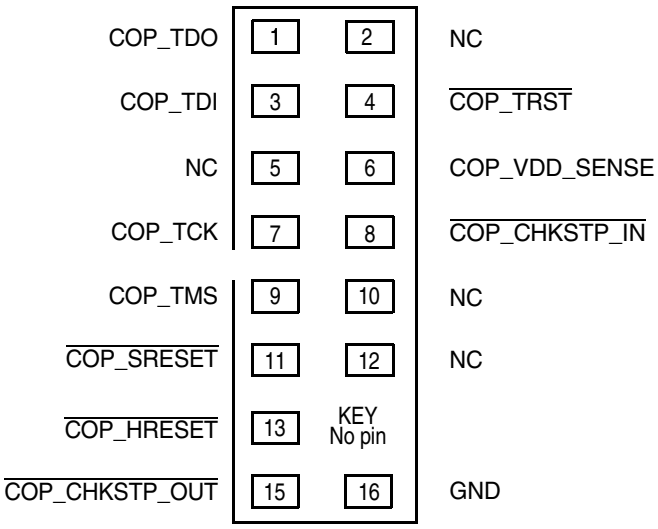


Figure 79. COP Connector Physical Pinout

3.11 Guidelines for High-Speed Interface Termination

3.11.1 SerDes1 Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins. See SerDes1 in Table 1 for details.

The following pins must be left unconnected (float):

- SD1_TX[7:0]
- $\overline{\text{SD1\_TX[7:0]}}$
- Reserved pins T22, T23

The following pins must be connected to XGND:

- SD1_RX[7:0]
- $\overline{\text{SD1\_RX[7:0]}}$
- SD1_REF_CLK
- $\overline{\text{SD1\_REF\_CLK}}$

The POR configuration pin cfg_io_ports[0:2] on TSEC3_TXD[6:3] can be used to power down SerDes 1 block for power saving. Note that both SVDD and XVDD must remain powered.

3.11.2 SerDes 1 Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD1_TX[7:0]
- $\overline{\text{SD1\_TX[7:0]}}$
- Reserved pins: T22, T23

4.1 Part Numbering Nomenclature

This table shows the part numbering nomenclature.

Table 82. Part Numbering Nomenclature

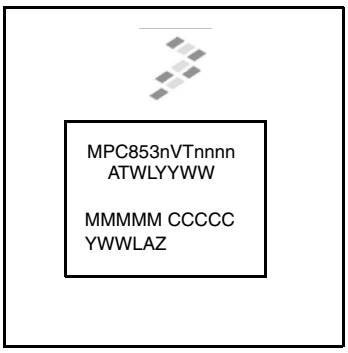
MPC	*nnnn*	*E*	*C*	*VT*	*AA*	*X*	*R*
Product Code	**Part Identifier**	**Security Engine**	**Tiers and Temperature Range**	**Package [1]**	**Processor Frequency [2]**	**DDR Frequency[3]**	**Revision Level**
MPC	8536	E = included	• A = Commercial tier standard temperature range (0° to 90°C) • B or Blank = industrial tier standard temperature range (0° to 105°C) • C = Industrial tier extended temperature range (–40° to 105°C)	• VT = FC-PBGA (Pb-free)[4] • PX = plastic standard • VJ = lead-free FC-PBGAs[5]	• AK = 600 MHz • AN = 800 MHz • AQ = 1000 MHz • AT = 1250 MHz • AU = 1333 MHz • AV = 1500 MHz	• G = 400 MHz • H = 500 MHz • J = 533 MHz • L = 667 MHz	Blank = Ver. 1.0 or 1.1 (SVR = 0x803F0090, 0x803F0091) A = Ver. 1.2 • (SVR = 0x803F0092)
		Blank = not included					Blank = Ver. 1.0 or 1.1 (SVR = 0x80370090, 0x80370091) A = Ver. 1.2 • (SVR = 0x80370092)

Notes:

1. See Section 5, “Package Information,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. See Table 84 for the corresponding maximum platform frequency.
4. The VT part number is ROHS-compliant, with the permitted exception of the C4 die bumps.
5. The VJ part number is entirely lead-free, including the C4 die bumps.

4.2 Part Marking

Parts are marked as in the example shown in the following figure.



FC-PBGA

Notes:

MMMMM is the 5-digit mask number.
ATWLYYWW is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 80. Part Marking for FC-PBGA