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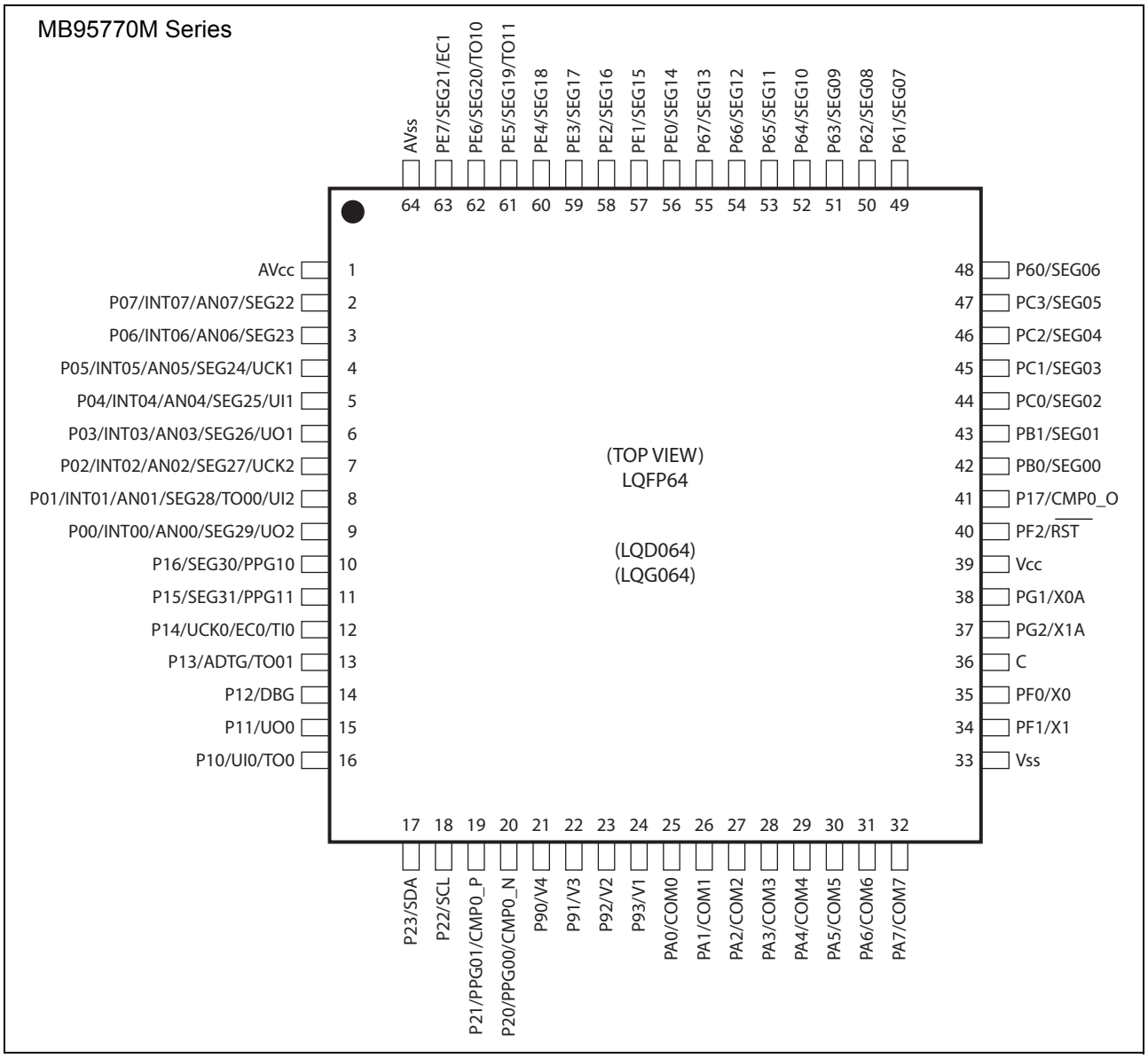
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy95f778jpmc2-g-une2


MB95770M Series
AVss
PE7/SEG21/EC1
PE6/SEG20/TO10
PE5/SEG19/TO11
PE4/SEG18
PE3/SEG17
PE2/SEG16
PE1/SEG15
PE0/SEG14
P67/SEG13
P66/SEG12
P65/SEG11
P64/SEG10
P63/SEG09
P62/SEG08
P61/SEG07
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
AVcc 1
P07/INT07/AN07/SEG22 2
P06/INT06/AN06/SEG23 3
P05/INT05/AN05/SEG24/UCK1 4
P04/INT04/AN04/SEG25/UI1 5
P03/INT03/AN03/SEG26/UO1 6
P02/INT02/AN02/SEG27/UCK2 7
P01/INT01/AN01/SEG28/TO00/UI2 8
P00/INT00/AN00/SEG29/UO2 9
P16/SEG30/PPG10 10
P15/SEG31/PPG11 11
P14/UCK0/EC0/TI0 12
P13/ADTG/TO01 13
P12/DBG 14
P11/UO0 15
P10/UI0/TO0 16
(TOP VIEW)
LQFP64
(LQD064)
(LQG064)
48 P60/SEG06
47 PC3/SEG05
46 PC2/SEG04
45 PC1/SEG03
44 PC0/SEG02
43 PB1/SEG01
42 PB0/SEG00
41 P17/CMP0_O
40 PF2/RST
39 Vcc
38 PG1/X0A
37 PG2/X1A
36 C
35 PF0/X0
34 PF1/X1
33 Vss
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
P23/SDA
P22/SCL
P21/PPG01/CMP0_P
P20/PPG00/CMP0_N
P90/V4
P91/V3
P92/V2
P93/V1
PA0/COM0
PA1/COM1
PA2/COM2
PA3/COM3
PA4/COM4
PA5/COM5
PA6/COM6
PA7/COM7

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
57	PC5	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG07		LCDC SEG07 output pin				
58	PC6	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG08		LCDC SEG08 output pin				
59	PC7	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG09		LCDC SEG09 output pin				
60	P60	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG10		LCDC SEG10 output pin				
61	P61	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG11		LCDC SEG11 output pin				
62	P62	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG12		LCDC SEG12 output pin				
63	P63	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG13		LCDC SEG13 output pin				
64	P64	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG14		LCDC SEG14 output pin				
65	P65	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG15		LCDC SEG15 output pin				
66	P66	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG16		LCDC SEG16 output pin				
67	P67	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG17		LCDC SEG17 output pin				
68	P43	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG18		LCDC SEG18 output pin				
69	P42	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG19		LCDC SEG19 output pin				
70	P41	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG20		LCDC SEG20 output pin				
71	P40	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG21		LCDC SEG21 output pin				
72	PE0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG22		LCDC SEG22 output pin				
73	PE1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG23		LCDC SEG23 output pin				
74	PE2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG24		LCDC SEG24 output pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
21	P90	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V4		LCD drive power supply pin				
22	P91	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V3		LCD drive power supply pin				
23	P92	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V2		LCD drive power supply pin				
24	P93	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V1		LCD drive power supply pin				
25	PA0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM0		LCDC COM0 output pin				
26	PA1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM1		LCDC COM1 output pin				
27	PA2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM2		LCDC COM2 output pin				
28	PA3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM3		LCDC COM3 output pin				
29	PA4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM4		LCDC COM4 output pin				
30	PA5	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM5		LCDC COM5 output pin				
31	PA6	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM6		LCDC COM6 output pin				
32	PA7	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM7		LCDC COM7 output pin				
33	V_{SS}	—	Power supply pin (GND)	—	—	—	—
34	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
35	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
36	C	—	Decoupling capacitor connection pin	—	—	—	—
37	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				

15. Areas For Specific Applications

The general-purpose register area and vector table area are used for the specific applications.

- General-purpose register area (Addresses: 0x0100 to 0x01FF)
  - This area contains the auxiliary registers used for 8-bit arithmetic operations, transfer, etc.
  - As this area forms part of the RAM area, it can also be used as conventional RAM.
  - When the area is used as general-purpose registers, general-purpose register addressing enables high-speed access with short instructions.

- Non-volatile register data area (Addresses: 0xFFBB to 0xFFBF)
  - The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register. For details, refer to “CHAPTER 28 NON-VOLATILE REGISTER (NVR) INTERFACE” in “New 8FX MB95710M/770M Series Hardware Manual”

- Vector table area (Addresses: 0xFFC0 to 0xFFFF)
  - This area is used as the vector table for vector call instructions (CALLV), interrupts, and resets.
  - The top of the Flash memory area is allocated to the vector table area. The start address of a service routine is set to an address in the vector table in the form of data.

  “Interrupt Source Table” lists the vector table addresses corresponding to vector call instructions, interrupts, and resets.
  For details, refer to “CHAPTER 4 RESET”, “CHAPTER 5 INTERRUPTS”, and “A.2 Special Instruction ■ Special Instruction ● CALLV #vct” in “APPENDIX” in “New 8FX MB95710M/770M Series Hardware Manual”.

- Direct bank pointer and access area

Direct bank pointer (DP[2:0])	Operand-specified dir	Access area
0bXXX (It does not affect mapping.)	0x0000 to 0x007F	0x0000 to 0x007F
0b000 (Initial value)	0x0090 to 0x00FF	0x0090 to 0x00FF
0b001	0x0080 to 0x00FF	0x0100 to 0x017F
0b010		0x0180 to 0x01FF
0b011		0x0200 to 0x027F
0b100		0x0280 to 0x02FF*
0b101		0x0300 to 0x037F
0b110		0x0380 to 0x03FF
0b111		0x0400 to 0x047F

*: Due to the memory size limit, the available access area is up to “0x028F” in MB95F714J/F714M/F774J/F774M.

16. I/O Map (MB95710M Series)

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E	PDR2	Port 2 data register	R/W	0b00000000
0x000F	DDR2	Port 2 direction register	R/W	0b00000000
0x0010, 0x0011	—	(Disabled)	—	—
0x0012	PDR4	Port 4 data register	R/W	0b00000000
0x0013	DDR4	Port 4 direction register	R/W	0b00000000
0x0014	PDR5	Port 5 data register	R/W	0b00000000
0x0015	DDR5	Port 5 direction register	R/W	0b00000000
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018 to 0x001B	—	(Disabled)	—	—
0x001C	PDR9	Port 9 data register	R/W	0b00000000
0x001D	DDR9	Port 9 direction register	R/W	0b00000000
0x001E	PDRA	Port A data register	R/W	0b00000000
0x001F	DDRA	Port A direction register	R/W	0b00000000
0x0020	PDRB	Port B data register	R/W	0b00000000
0x0021	DDRB	Port B direction register	R/W	0b00000000
0x0022	PDRC	Port C data register	R/W	0b00000000
0x0023	DDRC	Port C direction register	R/W	0b00000000
0x0024, 0x0025	—	(Disabled)	—	—

Address	Register abbreviation	Register name	R/W	Initial value
0x0026	PDRE	Port E data register	R/W	0b00000000
0x0027	DDRE	Port E direction register	R/W	0b00000000
0x0028	PDRF	Port F data register	R/W	0b00000000
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	—	(Disabled)	—	—
0x002D	PUL1	Port 1 pull-up register	R/W	0b00000000
0x002E	PUL2	Port 2 pull-up register	R/W	0b00000000
0x002F, 0x0030	—	(Disabled)	—	—
0x0031	PUL5	Port 5 pull-up register	R/W	0b00000000
0x0032 to 0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C	PC11	8/16-bit PPG timer 11 control register	R/W	0b00000000
0x003D	PC10	8/16-bit PPG timer 10 control register	R/W	0b00000000
0x003E	TMCSRH0	16-bit reload timer control status register (upper) ch. 0	R/W	0b00000000
0x003F	TMCSRL0	16-bit reload timer control status register (lower) ch. 0	R/W	0b00000000
0x0040 to 0x0047	—	(Disabled)	—	—
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C, 0x004D	—	(Disabled)	—	—
0x004E	LVDC	LVD control register	R/W	0b00000100
0x004F	LCDCC2	LCDC control register 2	R/W	0b00010100
0x0050	CMR0	Comparator control register ch. 0	R/W	0b00000001

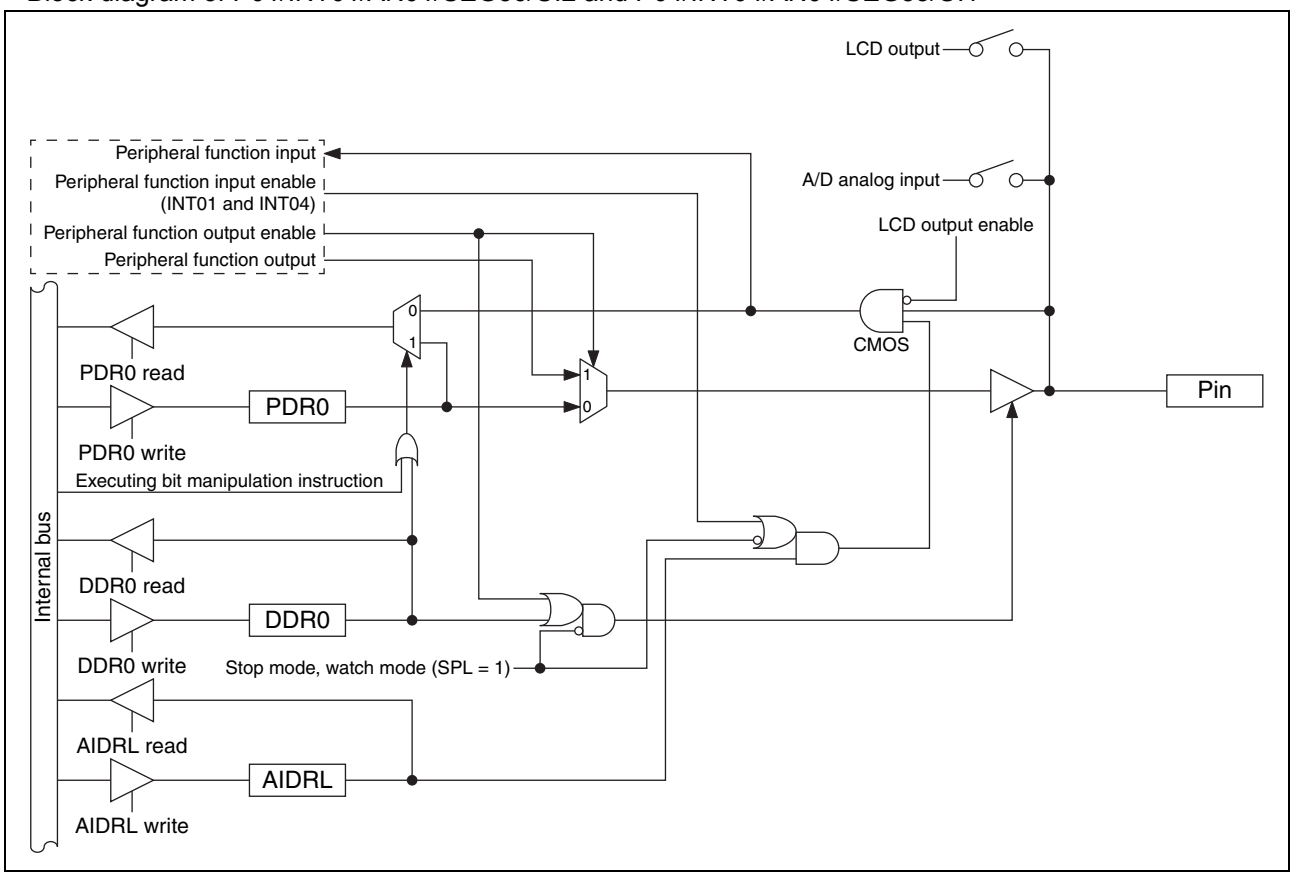
18. I/O Ports (MB95710M Series)

- List of port registers

Register name		Read/Write	Initial value
Port 0 data register	PDR0	R, RM/W	0b00000000
Port 0 direction register	DDR0	R/W	0b00000000
Port 1 data register	PDR1	R, RM/W	0b00000000
Port 1 direction register	DDR1	R/W	0b00000000
Port 2 data register	PDR2	R, RM/W	0b00000000
Port 2 direction register	DDR2	R/W	0b00000000
Port 4 data register	PDR4	R, RM/W	0b00000000
Port 4 direction register	DDR4	R/W	0b00000000
Port 5 data register	PDR5	R, RM/W	0b00000000
Port 5 direction register	DDR5	R/W	0b00000000
Port 6 data register	PDR6	R, RM/W	0b00000000
Port 6 direction register	DDR6	R/W	0b00000000
Port 9 data register	PDR9	R, RM/W	0b00000000
Port 9 direction register	DDR9	R/W	0b00000000
Port A data register	PDRA	R, RM/W	0b00000000
Port A direction register	DDRA	R/W	0b00000000
Port B data register	PDRB	R, RM/W	0b00000000
Port B direction register	DDRB	R/W	0b00000000
Port C data register	PDRC	R, RM/W	0b00000000
Port C direction register	DDRC	R/W	0b00000000
Port E data register	PDRE	R, RM/W	0b00000000
Port E direction register	DDRE	R/W	0b00000000
Port F data register	PDRF	R, RM/W	0b00000000
Port F direction register	DDRF	R/W	0b00000000
Port G data register	PDRG	R, RM/W	0b00000000
Port G direction register	DDRG	R/W	0b00000000
Port 1 pull-up register	PUL0	R/W	0b00000000
Port 2 pull-up register	PUL1	R/W	0b00000000
Port 5 pull-up register	PUL5	R/W	0b00000000
Port G pull-up register	PULG	R/W	0b00000000
A/D input disable register (lower)	AIDRL	R/W	0b00000000

R/W : Readable/writable (The read value is the same as the write value.)
R, RM/W : Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)

• Block diagram of P01/INT01/AN01/SEG36/UI2 and P04/INT04/AN04/SEG33/UI1



18.1.3 Port 0 registers

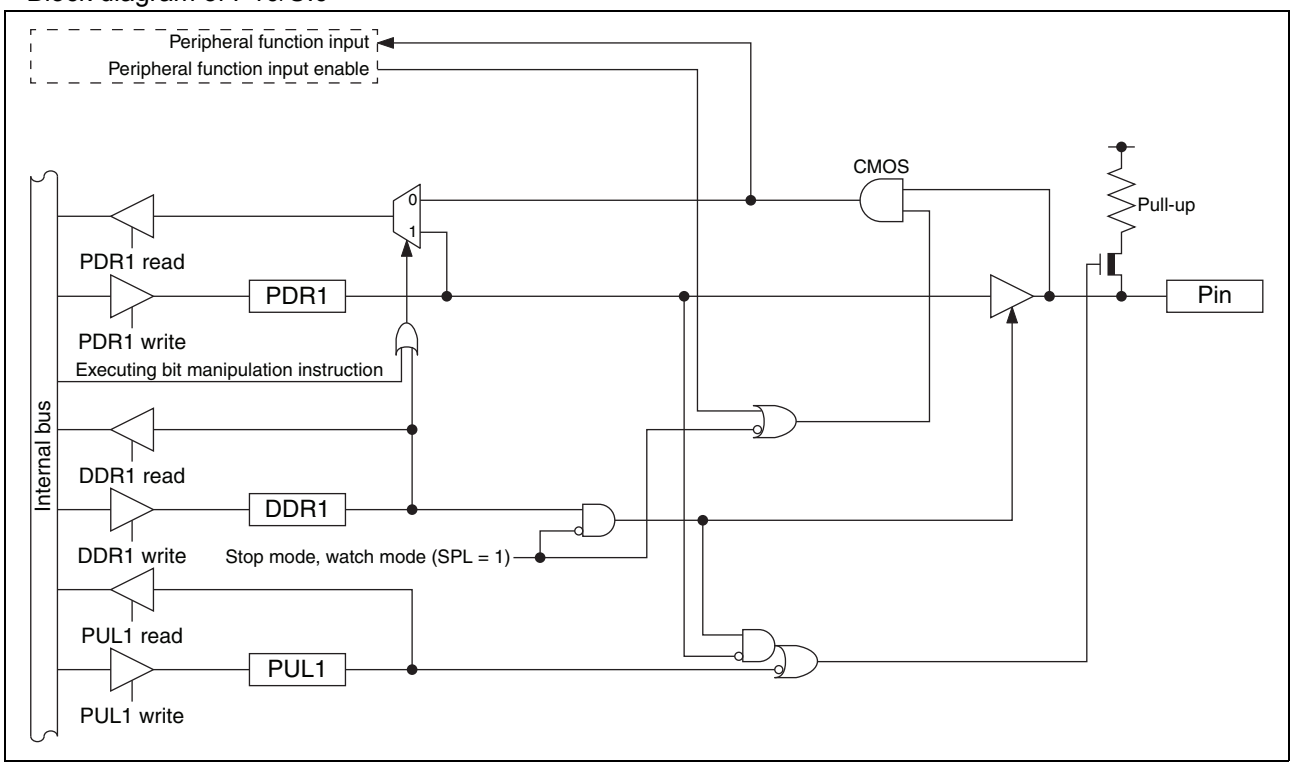
• Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR0	0	Pin state is “L” level.	PDR0 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR0 value is “1”.	As output port, outputs “H” level.
DDR0	0	Port input enabled		
	1	Port output enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

• Correspondence between registers and pins for port 0

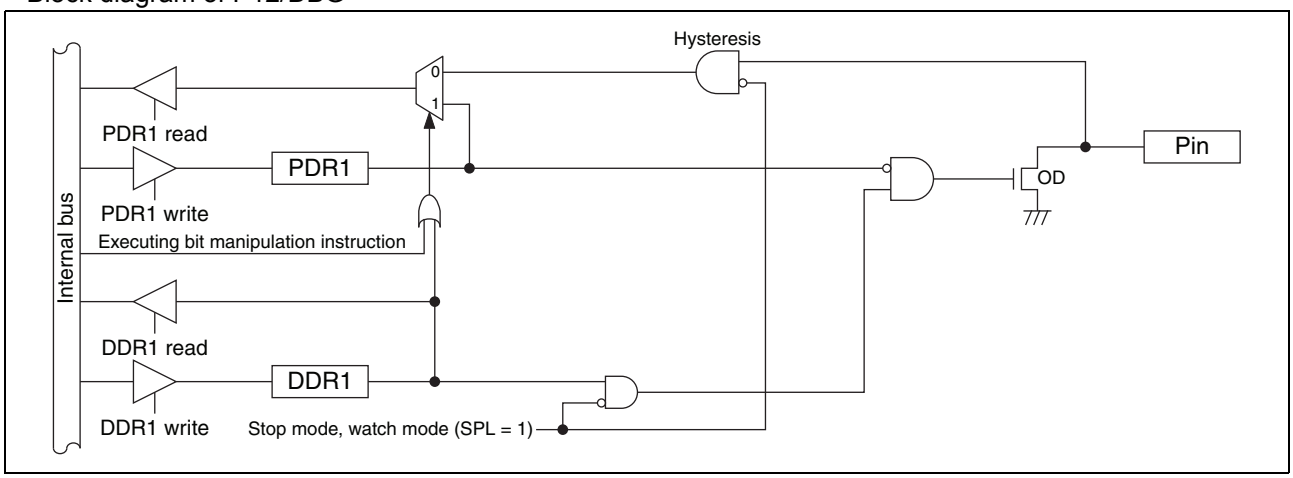
	Correspondence between related register bits and pins							
Pin name	P07	P06	P05	P04	P03	P02	P01	P00
PDR0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR0								
AIDRL								

- Block diagram of P10/UI0

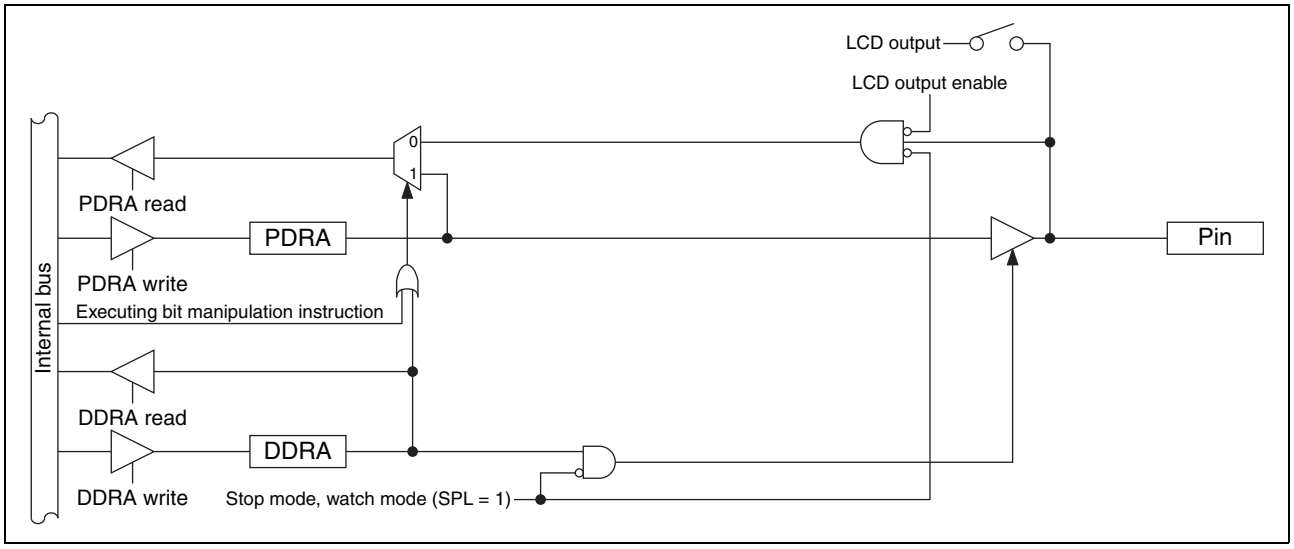


- P12/DBG pin
  This pin has the following peripheral function:
  - DBG input pin (DBG)

- Block diagram of P12/DBG



- Block diagram of PA0/COM0, PA1/COM1, PA2/COM2, PA3/COM3, PA4/COM4, PA5/COM5, PA6/COM6 and PA7/COM7



18.8.3 Port A registers

- Port A register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRA	0	Pin state is “L” level.	PDRA value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRA value is “1”.	As output port, outputs “H” level.
DDRA	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port A

	Correspondence between related register bits and pins							
Pin name	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PDRA	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDRA								

19.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.1.1 Port 0 configuration

Port 0 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 0 data register (PDR0)
- Port 0 direction register (DDR0)
- A/D input disable register (lower) (AIDRL)

19.1.2 Block diagrams of port 0

- P00/INT00/AN00/SEG29/UO2 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT00)
  - 8/12-bit A/D converter analog input pin (AN00)
  - LCDC SEG29 output pin (SEG29)
  - UART/SIO ch. 2 data output pin (UO2)

- P02/INT02/AN02/SEG27/UCK2 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT02)
  - 8/12-bit A/D converter analog input pin (AN02)
  - LCDC SEG27 output pin (SEG27)
  - UART/SIO ch. 2 clock I/O pin (UCK2)

- P03/INT03/AN03/SEG26/UO1 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT03)
  - 8/12-bit A/D converter analog input pin (AN03)
  - LCDC SEG26 output pin (SEG26)
  - UART/SIO ch. 1 data output pin (UO1)

- P05/INT05/AN05/SEG24/UCK1 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT05)
  - 8/12-bit A/D converter analog input pin (AN05)
  - LCDC SEG24 output pin (SEG24)
  - UART/SIO ch. 1 clock I/O pin (UCK1)

- P06/INT06/AN06/SEG23 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT06)
  - 8/12-bit A/D converter analog input pin (AN06)
  - LCDC SEG23 output pin (SEG23)

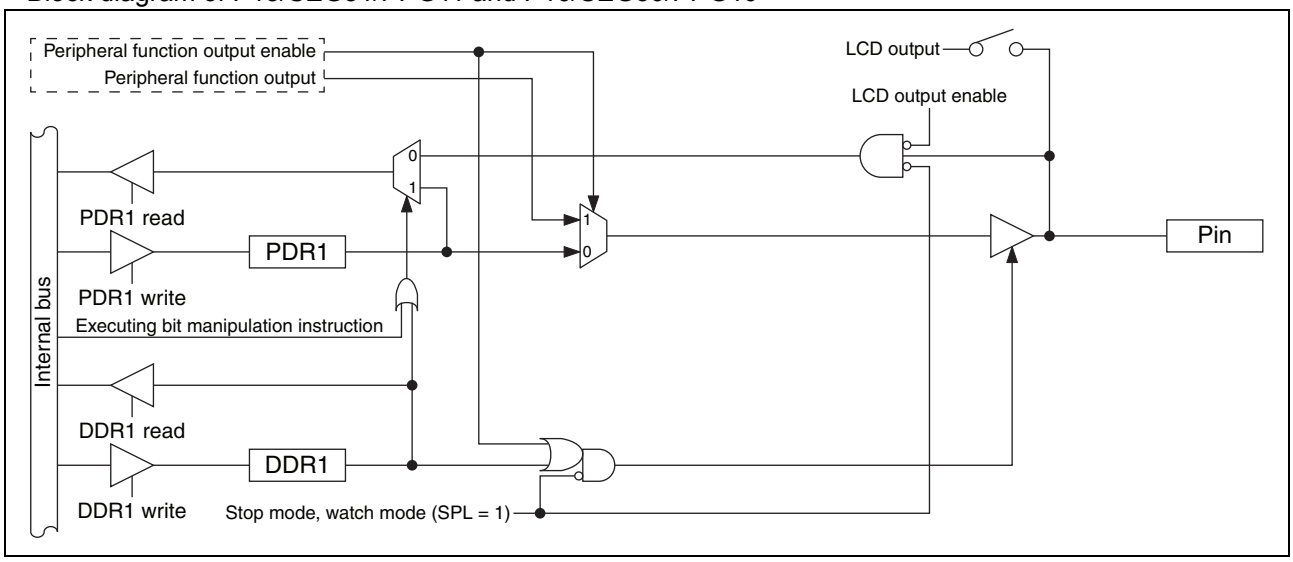
- P07/INT07/AN07/SEG22 pin

  This pin has the following peripheral functions:
  - External interrupt input pin (INT07)
  - 8/12-bit A/D converter analog input pin (AN07)
  - LCDC SEG22 output pin (SEG22)

- P15/SEG31/PPG11 pin
  This pin has the following peripheral functions:
  - LCDC SEG31 output pin (SEG31)
  - 8/16-bit PPG ch. 1 output pin (PPG11)

- P16/SEG30/PPG10 pin
  This pin has the following peripheral functions:
  - LCDC SEG30 output pin (SEG30)
  - 8/16-bit PPG ch. 1 output pin (PPG10)

- Block diagram of P15/SEG31/PPG11 and P16/SEG30/PPG10



19.2.3 Port 1 registers

- Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port 1

	Correspondence between related register bits and pins							
Pin name	P17	P16	P15	P14	P13	P12	P11	P10
PDR1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR1								
PUL1		-	-			-		

22. Electrical Characteristics

22.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	–2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average current	I_{OLAV}	—	4	mA	Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average current	I_{OHAV}	—	–4	mA	Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{stg}	–55	+150	°C	

*1: These parameters are based on the condition that V_{SS} is 0.0 V.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Specific pins: P00 to P07, P10, P11, P13 to P16, P20 to P22, P40 to P43, P50 to P53, P60 to P67, P90 to P94, PA0 to PA7, PB0 to PB4, PC0 to PC7, PE0 to PE7, PF0, PF1, PG1, PG2 (P40 to P43, P50 to P53, P94, PB2 to PB4 and PC4 to PC7 are only available on the MB95710M Series.)

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL}	All output pins	I_{OL} = 4 mA*4	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	–5	—	+5	µA	When the internal pull-up resistor is disabled
Internal pull-up resistor	R_{PULL}	P10, P11, P13, P14, P17, P20, P21, P50 to P53*2, PG1, PG2	V_I = 0 V	75	100	150	kΩ	When the internal pull-up resistor is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

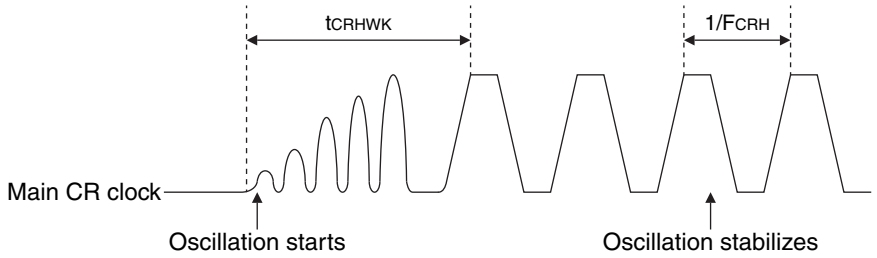
22.4 AC Characteristics

22.4.1 Clock Timing

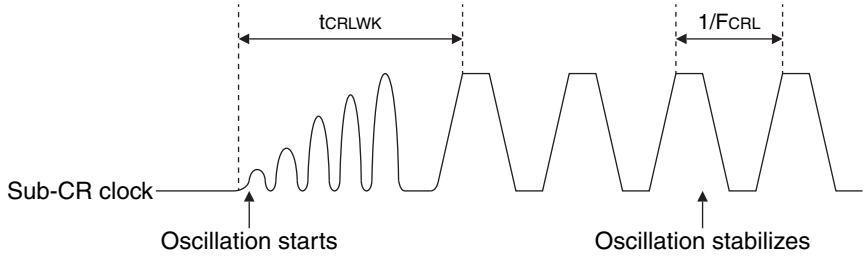
(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency		X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	—	1	—	32.5	MHz	When the main external clock is used
	F_{CH}	X0, X1	—	4	—	8.13	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 2
				4	—	6.5	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 2.5
				4	—	5.41	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 3
				4	—	4.06	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 4
	F_{CRH}	—	—	3.92	4	4.08	MHz	Operating conditions • The main CR clock is used. • 0 °C ≤ T_A ≤ +70 °C
				3.8	4	4.2	MHz	Operating conditions • The main CR clock is used. • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
	F_{MCRPLL}	—	—	7.84	8	8.16	MHz	Operating conditions • PLL multiplication rate: 2 • 0 °C ≤ T_A ≤ +70 °C
				7.6	8	8.4	MHz	Operating conditions • PLL multiplication rate: 2 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				9.8	10	10.2	MHz	Operating conditions • PLL multiplication rate: 2.5 • 0 °C ≤ T_A ≤ +70 °C
				9.5	10	10.5	MHz	Operating conditions • PLL multiplication rate: 2.5 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				11.76	12	12.24	MHz	Operating conditions • PLL multiplication rate: 3 • 0 °C ≤ T_A ≤ +70 °C
				11.4	12	12.6	MHz	Operating conditions • PLL multiplication rate: 3 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C

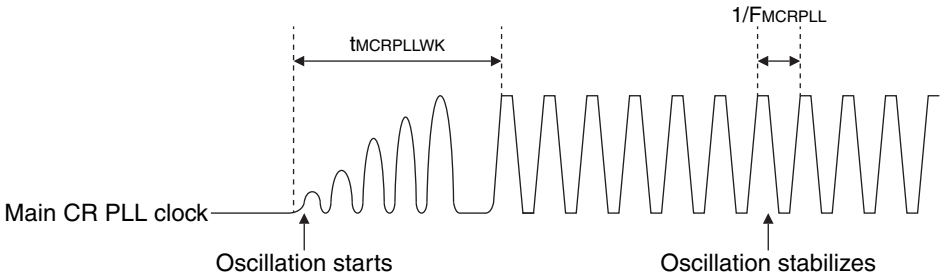
- Input waveform generated when an internal clock (main CR clock) is used



- Input waveform generated when an internal clock (sub-CR clock) is used



- Input waveform generated when an internal clock (main CR PLL clock) is used



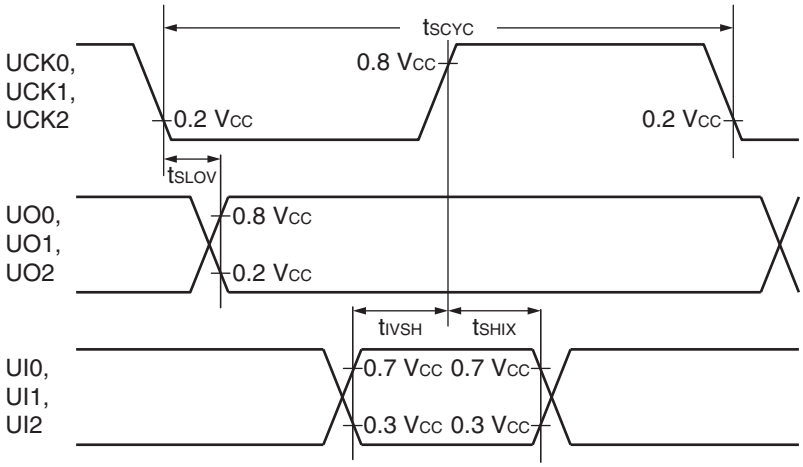
22.4.8 UART/SIO, Serial I/O Timing

(V_{CC} = 3.0 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0, UCK1, UCK2	Internal clock operation output pin: C_L = 80 pF + 1 TTL	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UCK1, UCK2, UO0, UO1, UO2		–190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0, UCK1, UCK2	External clock operation output pin: C_L = 80 pF + 1 TTL	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0, UCK1, UCK2		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UCK1, UCK2, UO0, UO1, UO2		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



22.6 Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.3*1	1.6*2	s	The time of writing “0x00” prior to erasure is excluded.
Sector erase time (24 Kbyte sector and 32 Kbyte sector)	—	0.6*1	3.1*2	s	The time of writing “0x00” prior to erasure is excluded.
Byte writing time	—	17	272	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	1.8	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85 °C Number of program/erase cycles: 1000 or below
	10*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 1001 to 10000 inclusive
	5*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 10001 or above

*1: V_{CC} = 5.5 V, T_A = +25 °C, 0 cycle
*2: V_{CC} = 1.8 V, T_A = +85 °C, 100000 cycles
*3: These values were converted from the result of a technology reliability assessment. (These values were converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85 °C.)

Document History Page

Document Title: MB95710M Series, MB95770M Series, New 8FX 8-bit Microcontrollers Document Number: 002-09307				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	YSKA	07/31/2013	Migrated Spansion DS702-00019-1v0-E to Cypress and assigned document number 002-09307. No change to document contents or format.
*A	5511943	YSKA	11/08/2016	Updated to Cypress template
*B	5633448	HTER	03/07/2017	Changed the package codes as the following from “FPT-80P-M37” to “LQH080” from “FPT-64P-M38” to “LQD064” from “FPT-64P-M39” to “LQG064” in chapter: 1.Product Line-up (Page 6, 9) 2.Packages And Corresponding Products (Page 9) 4.Pin Assignment (Page 11 to 12) 25.Ordering Information (Page 167) 26.Package Dimensions (Page 168 to 170). Changed the Part numbers from “MB95F778JPMC2-G-SNE2” to “MB95F778JPMC2-G-UNE2” in chapter 25.Ordering Information (Page 167).
*C	5772061	YSAT	06/15/2017	Adapted new Cypress logo
*D	5900838	HUAL	09/29/2017	Modified from “MB95F718JPMC-G-SNE2” to “MB95F718JPMC-G-UNE2” in 25.Ordering Information (Page 167).

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