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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, POR, PWM, WDT
Number of I/O	74
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f714mpmc-g-sne2

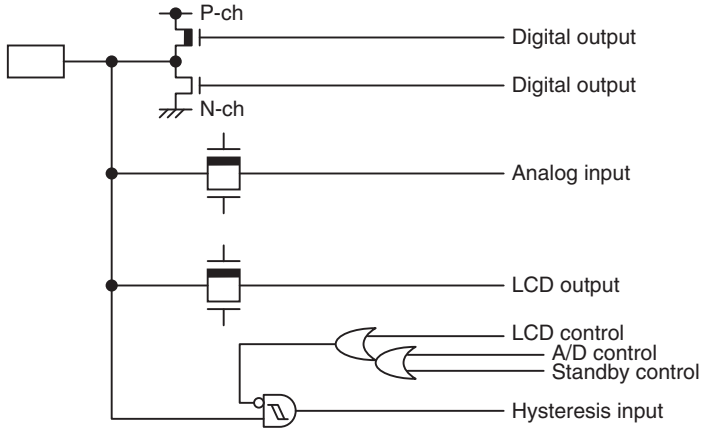
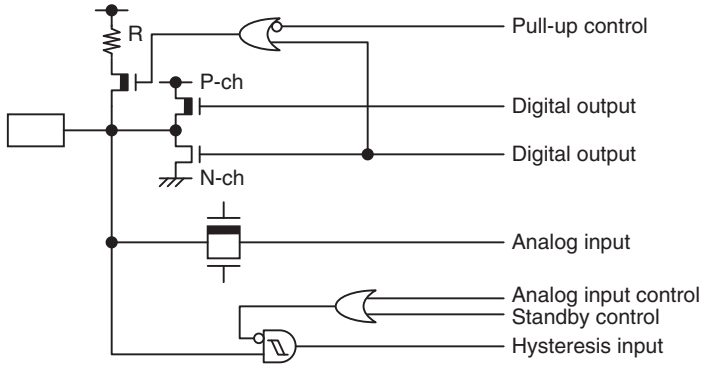
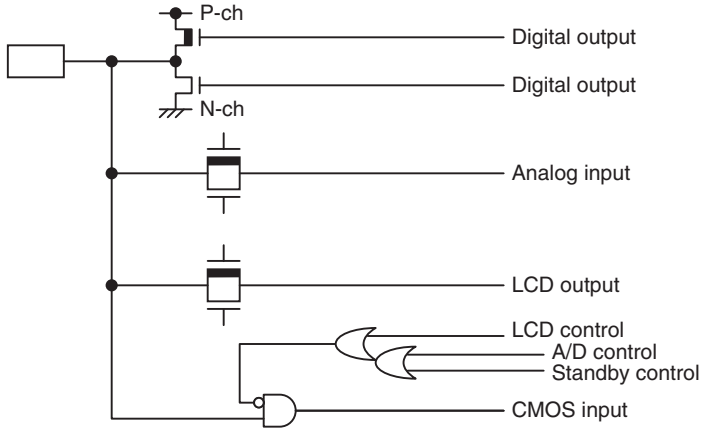
Contents

1. Product Line-up

1.1 MB95710M Series

Part number / Parameter	MB95F714J	MB95F716J	MB95F718J	MB95F714M	MB95F716M	MB95F718M
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation and the subclock oscillation.					
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	512 bytes	1 Kbyte	2 Kbyte	512 bytes	1 Kbyte	2 Kbyte
Power-on reset	Yes					
Low-voltage detection reset	Yes			No		
Reset input	Selected through software			With dedicated reset input		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O port : 75 • CMOS I/O : 71 • N-ch open drain : 4			• I/O port : 74 • CMOS I/O : 71 • N-ch open drain : 3		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (min) • The sub-CR clock can be used as the source clock of the software watchdog timer.					
Wild register	It can be used to replace 3 bytes of data.					
8/12-bit A/D converter	8 channels					
	8-bit or 12-bit resolution can be selected.					
8/16-bit composite timer	2 channels					
	• The timer can be configured as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
External interrupt	8 channels					
	• Interrupt by edge detection (The rising edge, falling edge, and both edges can be selected.) • It can be used to wake up the device from different standby modes.					
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).					

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
21	P90	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V4		LCD drive power supply pin				
22	P91	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V3		LCD drive power supply pin				
23	P92	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V2		LCD drive power supply pin				
24	P93	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V1		LCD drive power supply pin				
25	PA0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM0		LCDC COM0 output pin				
26	PA1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM1		LCDC COM1 output pin				
27	PA2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM2		LCDC COM2 output pin				
28	PA3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM3		LCDC COM3 output pin				
29	PA4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM4		LCDC COM4 output pin				
30	PA5	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM5		LCDC COM5 output pin				
31	PA6	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM6		LCDC COM6 output pin				
32	PA7	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM7		LCDC COM7 output pin				
33	V_{SS}	—	Power supply pin (GND)	—	—	—	—
34	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
35	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
36	C	—	Decoupling capacitor connection pin	—	—	—	—
37	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				

Type	Circuit	Remarks
S		• CMOS output • LCD output • Hysteresis input • Analog input
T		• CMOS output • Hysteresis input • Analog input • Pull-up control
V		• CMOS output • CMOS input • LCD output • Analog input

8. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

8.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- **Absolute Maximum Ratings**

  Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- **Recommended Operating Conditions**

  Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

  Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

  No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- **Processing and Protection of Pins**

  These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

  (1) Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

  (2) Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

  Therefore, avoid this type of connection.

  (3) Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- **Latch-up**

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

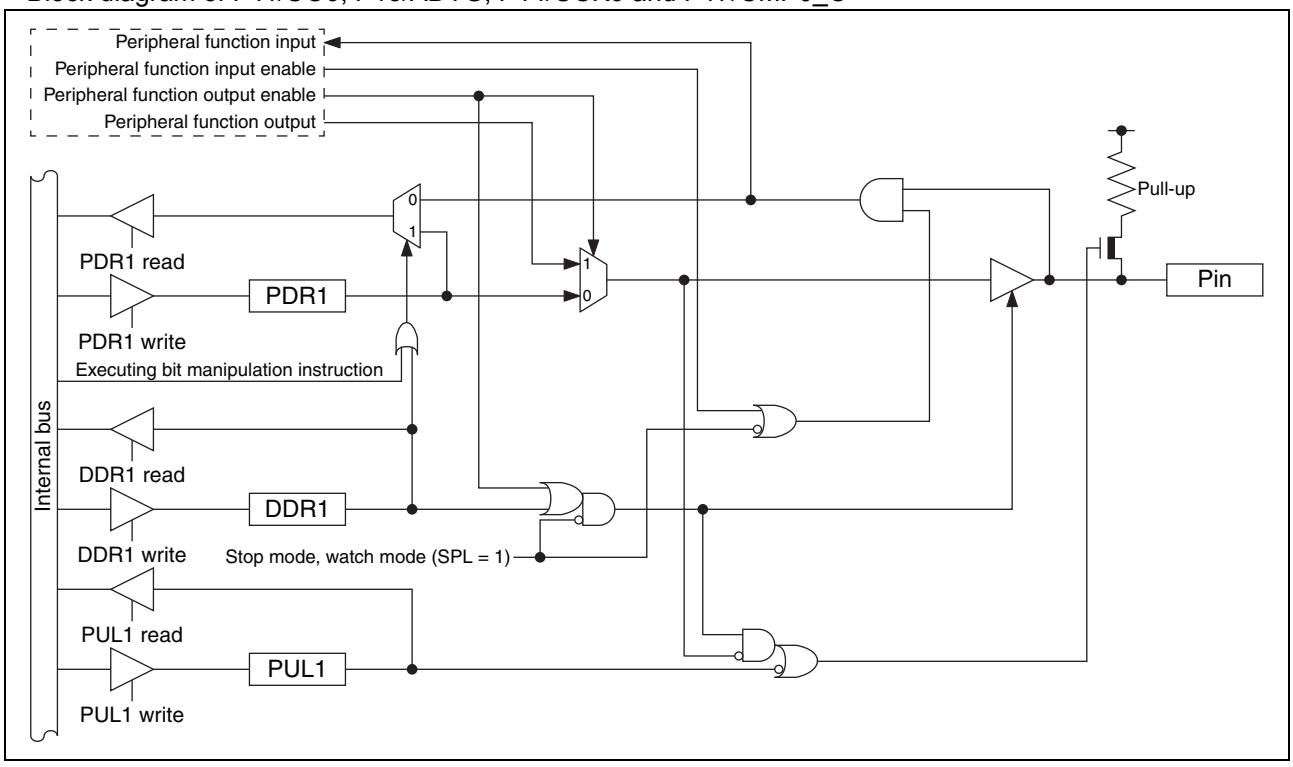
- P11/UO0 pin
  This pin has the following peripheral function:
  - UART/SIO ch. 0 data output pin (UO0)

- P13/ADTG pin
  This pin has the following peripheral function:
  - 8/12-bit A/D converter trigger input pin (ADTG)

- P14/UCK0 pin
  This pin has the following peripheral function:
  - UART/SIO ch. 0 clock I/O pin (UCK0)

- P17/CMP0_O pin
  This pin has the following peripheral function:
  - Comparator ch. 0 digital output pin (CMP0_O)

- Block diagram of P11/UO0, P13/ADTG, P14/UCK0 and P17/CMP0_O



18.8 Port A

Port A is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.8.1 Port A configuration

Port A is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port A data register (PDRA)
- Port A direction register (DDRA)

18.8.2 Block diagrams of port A

- PA0/COM0 pin
  This pin has the following peripheral function:
  - LCDC COM0 output pin (COM0)

- PA1/COM1 pin
  This pin has the following peripheral function:
  - LCDC COM1 output pin (COM1)

- PA2/COM2 pin
  This pin has the following peripheral function:
  - LCDC COM2 output pin (COM2)

- PA3/COM3 pin
  This pin has the following peripheral function:
  - LCDC COM3 output pin (COM3)

- PA4/COM4 pin
  This pin has the following peripheral function:
  - LCDC COM4 output pin (COM4)

- PA5/COM5 pin
  This pin has the following peripheral function:
  - LCDC COM5 output pin (COM5)

- PA6/COM6 pin
  This pin has the following peripheral function:
  - LCDC COM6 output pin (COM6)

- PA7/COM7 pin
  This pin has the following peripheral function:
  - LCDC COM7 output pin (COM7)

19.1.4 Port 0 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
  - If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR0 register returns the PDR0 register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When using an analog input shared pin as an input port, set the corresponding bit in the A/D input disable register (lower) (AIDRL) to “1”.
  - If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR0 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR0 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to “0”.
  - When using the analog input shared pin as another peripheral function input pin, configure it as an input port, which is the same as the operation as an input port.
  - Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

- Operation as an LCDC segment output pin
  - Set the bit in the DDR0 register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset

  If the CPU is reset, all bits in the DDR0 register are initialized to “0” and port input is enabled. As for a pin shared with analog input, its port input is disabled because the AIDRL register is initialized to “0”.

19.4.4 Port 6 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
  - If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR6 register returns the PDR6 register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC segment output pin
  - Set the bit in the DDR6 register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDR6 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.6 Port A

Port A is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.6.1 Port A configuration

Port A is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port A data register (PDRA)
- Port A direction register (DDRA)

19.6.2 Block diagrams of port A

- PA0/COM0 pin
  This pin has the following peripheral function:
  - LCDC COM0 output pin (COM0)

- PA1/COM1 pin
  This pin has the following peripheral function:
  - LCDC COM1 output pin (COM1)

- PA2/COM2 pin
  This pin has the following peripheral function:
  - LCDC COM2 output pin (COM2)

- PA3/COM3 pin
  This pin has the following peripheral function:
  - LCDC COM3 output pin (COM3)

- PA4/COM4 pin
  This pin has the following peripheral function:
  - LCDC COM4 output pin (COM4)

- PA5/COM5 pin
  This pin has the following peripheral function:
  - LCDC COM5 output pin (COM5)

- PA6/COM6 pin
  This pin has the following peripheral function:
  - LCDC COM6 output pin (COM6)

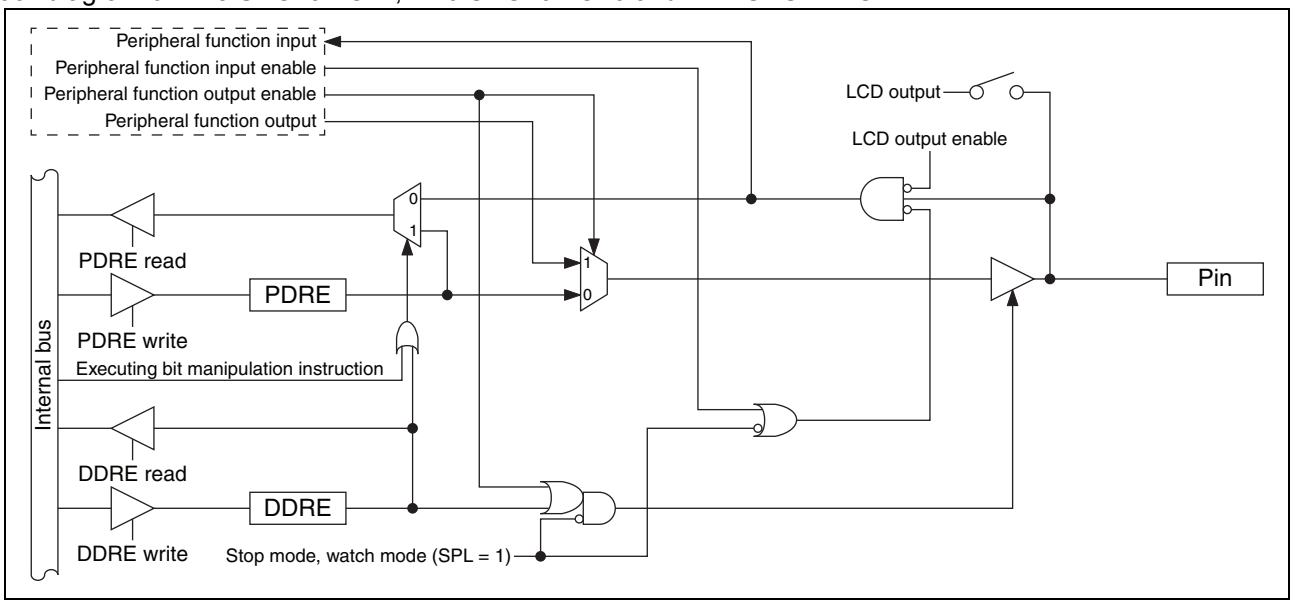
- PA7/COM7 pin
  This pin has the following peripheral function:
  - LCDC COM7 output pin (COM7)

- PE5/SEG19/TO11 pin
  This pin has the following peripheral functions:
  - LCDC SEG19 output pin (SEG19)
  - 8/16-bit composite timer ch. 1 output pin (TO11)

- PE6/SEG20/TO10 pin
  This pin has the following peripheral functions:
  - LCDC SEG20 output pin (SEG20)
  - 8/16-bit composite timer ch. 1 output pin (TO10)

- PE7/SEG21/EC1 pin
  This pin has the following peripheral functions:
  - LCDC SEG21 output pin (SEG21)
  - 8/16-bit composite timer ch. 1 clock input pin (EC1)

- Block diagram of PE5/SEG19/TO11, PE6/SEG20/TO10 and PE7/SEG21/EC1



19.9.3 Port E registers

- Port E register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRE	0	Pin state is “L” level.	PDRE value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRE value is “1”.	As output port, outputs “H” level.
DDRE	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port E

	Correspondence between related register bits and pins							
Pin name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
PDRE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDRE								

- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.10 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.10.1 Port F configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)

19.10.2 Block diagrams of port F

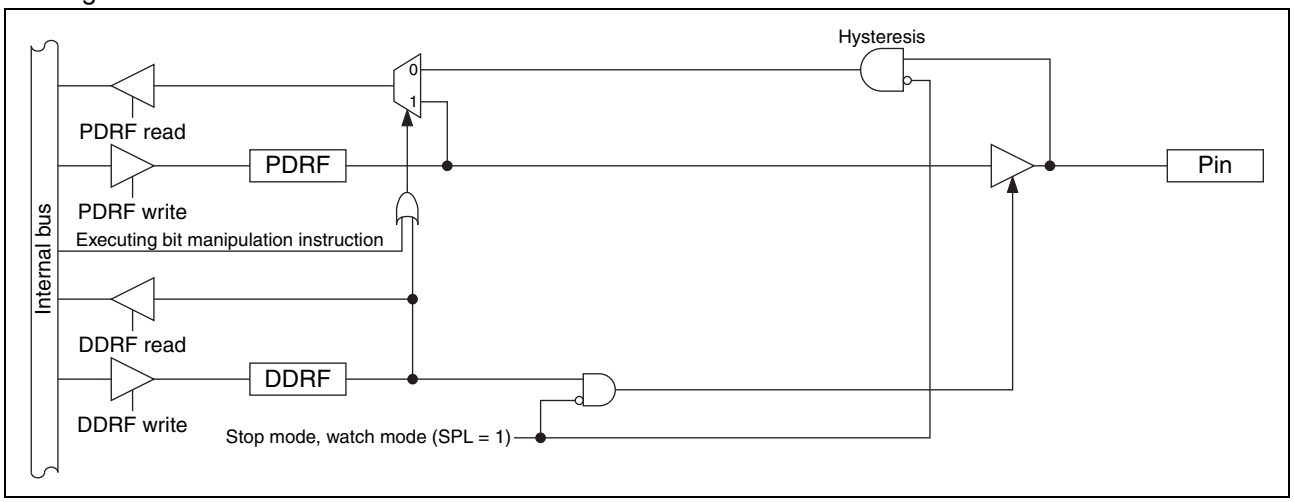
- PF0/X0 pin

  This pin has the following peripheral function:
  - Main clock input oscillation pin (X0)

- PF1/X1 pin

  This pin has the following peripheral function:
  - Main clock I/O oscillation pin (X1)

- Block diagram of PF0/X0 and PF1/X1



22.3 DC Characteristics

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P01, P04, P10, P22, P23	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{ILI}	P01, P04, P10, P22, P23	*1	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, P22, P23, PF2	—	V_{SS} – 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH}	Output pins other than P12, P22, P23, PF2	I_{OH} = –4 mA*3	V_{CC} – 0.5	—	—	V	

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

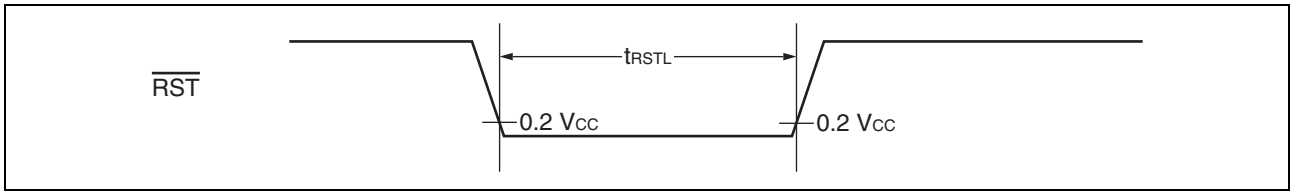
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{MCRPLL}	—	—	15.68	16	16.32	MHz	Operating conditions • PLL multiplication rate: 4 • 0 °C ≤ T_A ≤ +70 °C
				15.2	16	16.8	MHz	Operating conditions • PLL multiplication rate: 4 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
	F_{MPLL}	—	—	8	—	16	MHz	When the main PLL clock is used
	F_{CL}	X0A, X1A	——	—	32.768	—	kHz	When the sub-oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	150	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	—	30.8	—	1000	ns	When an external clock is used
		X0, X1	—	—	250	—	ns	When the main PLL clock is used
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1}, t_{WL1}	X0	—	12.4	—	—	ns	When an external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	—	—	125	—	ns	When the main PLL clock is used
	t_{WH2}, t_{WL2}	X0A	—	—	15.2	—	µs	When an external clock is used, the duty ratio should range between 40% and 60%.
Input clock rising time and falling time	t_{CR}, t_{CF}	X0, X0A	—	—	—	5	ns	When an external clock is used
CR oscillation start time	t_{CRHWK}	—	—	—	—	50	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	30	µs	When the sub-CR clock is used
PLL oscillation start time	$t_{MCRPLLWK}$	—	—	—	—	100	µs	When the main CR PLL clock is used

22.4.3 External Reset

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*	—	ns	

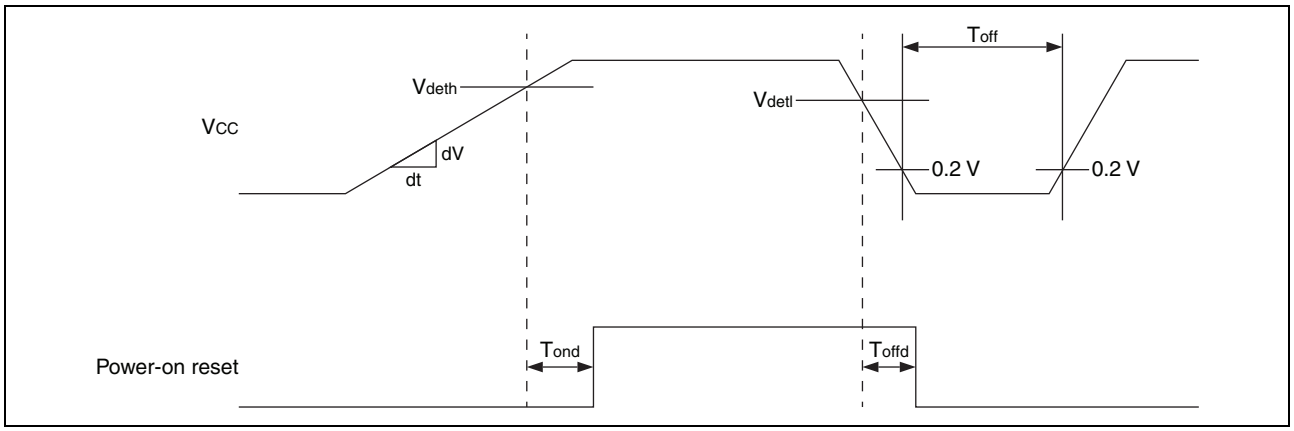
*: See "Source Clock/Machine Clock" for t_{MCLK}.



22.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply rising time	dV/dt	V_{CC}	0.1	—	—	V/ms	
Power supply cutoff time	T_{off}		1	—	—	ms	
Reset release voltage	V_{deth}		1.44	1.60	1.76	V	At voltage rise
Reset detection voltage	V_{detl}		1.39	1.55	1.71	V	At voltage fall
Reset release delay time	T_{ond}		—	—	10	ms	dV/dt ≥ 0.1 mV/µs
Reset detection delay time	T_{offd}		—	—	0.4	ms	dV/dt ≥ –0.04 mV/µs



- Low power consumption mode

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Interrupt release voltage 0	V_{IDLL0+}	2.06	2.3	2.54	V	At power supply rise
Interrupt detection voltage 0	V_{IDLL0-}	1.98	2.2	2.42	V	At power supply fall
Interrupt release voltage 1	V_{IDLL1+}	2.33	2.6	2.87	V	At power supply rise
Interrupt detection voltage 1	V_{IDLL1-}	2.25	2.5	2.75	V	At power supply fall
Interrupt release voltage 2	V_{IDLL2+}	2.6	2.9	3.2	V	At power supply rise
Interrupt detection voltage 2	V_{IDLL2-}	2.52	2.8	3.08	V	At power supply fall
Interrupt release voltage 3	V_{IDLL3+}	2.96	3.3	3.64	V	At power supply rise
Interrupt detection voltage 3	V_{IDLL3-}	2.88	3.2	3.52	V	At power supply fall
Interrupt release voltage 4	V_{IDLL4+}	3.32	3.7	4.08	V	At power supply rise
Interrupt detection voltage 4	V_{IDLL4-}	3.24	3.6	3.96	V	At power supply fall
Interrupt release voltage 5	V_{IDLL5+}	3.68	4.1	4.52	V	At power supply rise
Interrupt detection voltage 5	V_{IDLL5-}	3.6	4	4.4	V	At power supply fall
Power supply start voltage	V_{offL}	—	—	1.6	V	
Power supply end voltage	V_{onL}	4.52	—	—	V	
Power supply voltage change time (at power supply rise)	t_{rL}	7300	—	—	µs	Slope of power supply that the interrupt release signal generates within the rating (V_{IDLL+})
Power supply voltage change time (at power supply fall)	t_{fL}	7300	—	—	µs	Slope of power supply that the interrupt detection signal generates within the rating (V_{IDLL-})
Interrupt release delay time	t_{diL1}	—	—	400	µs	
Interrupt detection delay time	t_{diL2}	—	—	400	µs	
Interrupt threshold voltage transition stabilization time	t_{stbL}	—	—	400	µs	
Interrupt low-voltage detection mode switch time	t_{mdsw}	—	—	400	µs	Normal mode ⇔ Low power consumption mode

Note: When being used for interrupt, the low-voltage detection circuit can be switched between normal mode and low power consumption mode. Compared with normal mode, in low power consumption mode, while the detection voltage and release voltage are less accurate, and the detection delay time and the release delay time become longer, there is less power consumption. For the difference in power consumption between normal mode and low power consumption mode, see “22.3 DC Characteristics”. For the method of switching between normal mode and low power consumption mode, refer to “CHAPTER 16 LOW-VOLTAGE DETECTION CIRCUIT” in “New 8FX MB95710M/770M Series Hardware Manual”.

22.5 A/D Converter

22.5.1 A/D Converter Electrical Characteristics

(AV_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

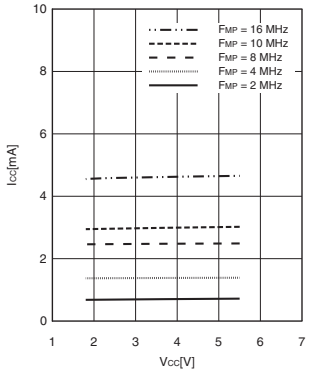
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	12	bit	
Total error		–6	—	+6	LSB	$V_{CC} \geq 2.7$ V
		–10	—	+10	LSB	$V_{CC} < 2.7$ V
Linearity error		–3	—	+3	LSB	$V_{CC} \geq 2.7$ V
		–5	—	+5	LSB	$V_{CC} < 2.7$ V
Differential linearity error		–1.9	—	+1.9	LSB	$V_{CC} \geq 2.7$ V
		–2.9	—	+2.9	LSB	$V_{CC} < 2.7$ V
Zero transition voltage	V_{0T}	V_{SS} – 6 LSB	—	V_{SS} + 8.2 LSB	V	
Full-scale transition voltage	V_{FST}	AV_{CC} – 6.2 LSB	—	AV_{CC} + 9.2 LSB	V	
Sampling time	T_S	*	—	10	µs	
Compare time	T_{cck}	0.861	—	14	µs	$V_{CC} \geq 2.7$ V
		2.8	—	14	µs	$V_{CC} < 2.7$ V
Time for transiting to operation enabled state	T_{stt}	1	—	—	µs	
Analog input current	I_{AIN}	–0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	AV_{CC}	V	

*: See “Notes on Using A/D Converter” for details of the minimum sampling time.

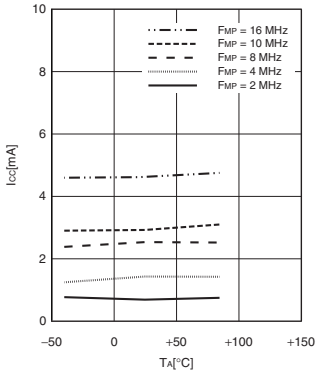
23. Sample Characteristics

- Power supply current temperature characteristics

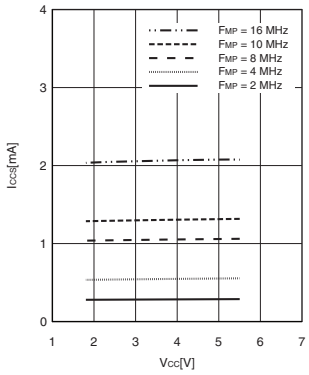
I_{CC} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



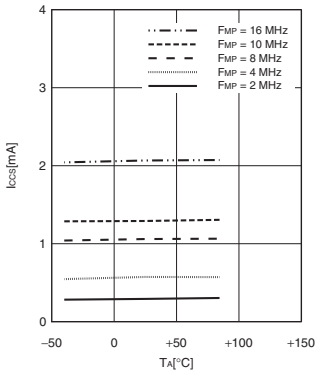
I_{CC} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



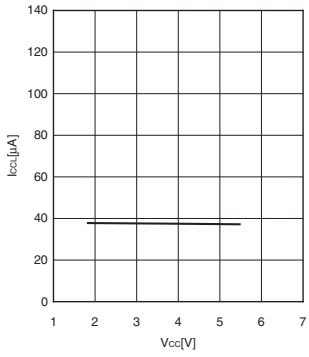
I_{CCS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



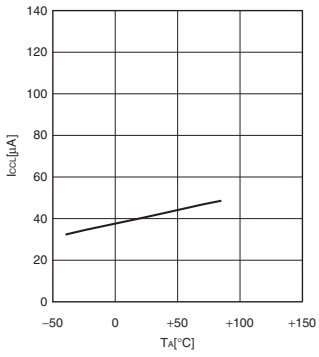
I_{CCS} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



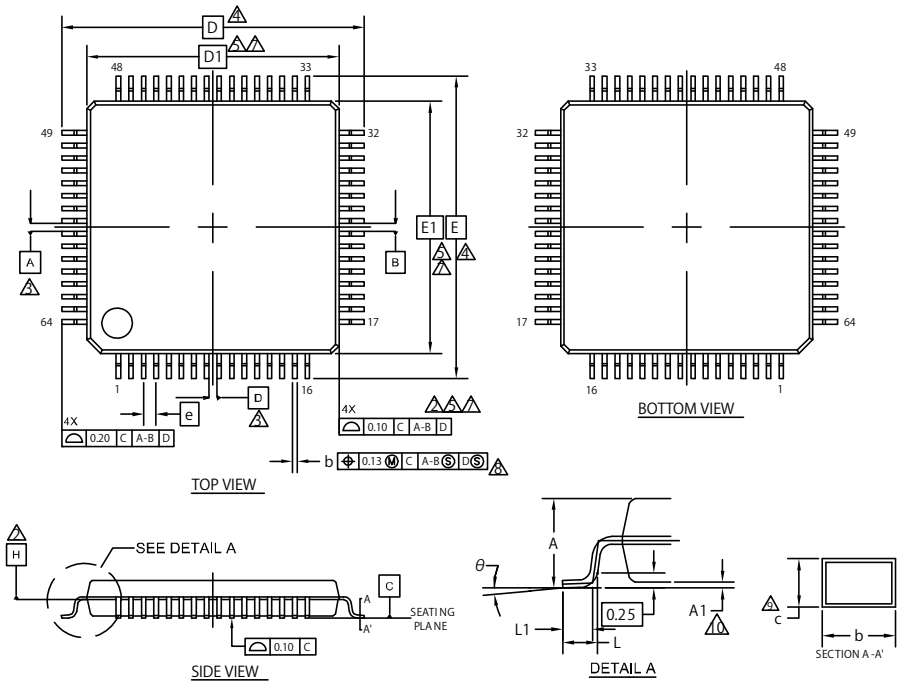
I_{CCL} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



I_{CCL} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



Package Type	Package Code
LQFP 64	LQG 064



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.00	——	0.20
b	0.27	0.32	0.37
c	0.09	——	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.65 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	——	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13881 **

PACKAGE OUTLINE, 64 LEAD LQFP
12.0X12.0X1.7 MM LQG064 REV**

Document History Page

Document Title: MB95710M Series, MB95770M Series, New 8FX 8-bit Microcontrollers Document Number: 002-09307				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	YSKA	07/31/2013	Migrated Spansion DS702-00019-1v0-E to Cypress and assigned document number 002-09307. No change to document contents or format.
*A	5511943	YSKA	11/08/2016	Updated to Cypress template
*B	5633448	HTER	03/07/2017	Changed the package codes as the following from “FPT-80P-M37” to “LQH080” from “FPT-64P-M38” to “LQD064” from “FPT-64P-M39” to “LQG064” in chapter: 1.Product Line-up (Page 6, 9) 2.Packages And Corresponding Products (Page 9) 4.Pin Assignment (Page 11 to 12) 25.Ordering Information (Page 167) 26.Package Dimensions (Page 168 to 170). Changed the Part numbers from “MB95F778JPMC2-G-SNE2” to “MB95F778JPMC2-G-UNE2” in chapter 25.Ordering Information (Page 167).
*C	5772061	YSAT	06/15/2017	Adapted new Cypress logo
*D	5900838	HUAL	09/29/2017	Modified from “MB95F718JPMC-G-SNE2” to “MB95F718JPMC-G-UNE2” in 25.Ordering Information (Page 167).