Infineon Technologies - MB95F778JPMC1-G-SNE2 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	59
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f778jpmc1-g-sne2

- Low-voltage detection (LVD) circuit (only available on MB95F714J/F716J/F718J/F774J/F776J/F778J)
  - Built-in low-voltage detection function
- Comparator × 1 channel
- Clock supervisor counter
  - Built-in clock supervisor counter
- Dual operation Flash memory
  - The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
  - Protects the content of the Flash memory.

3. Differences Among Products And Notes On Product Selection

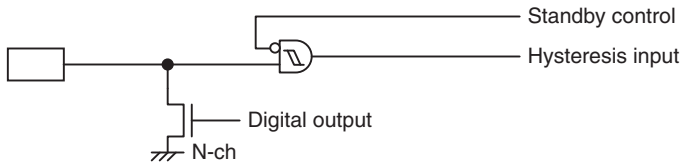
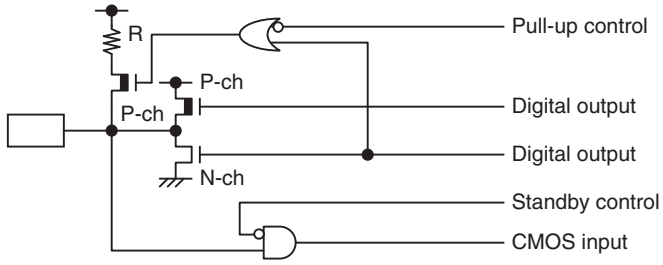
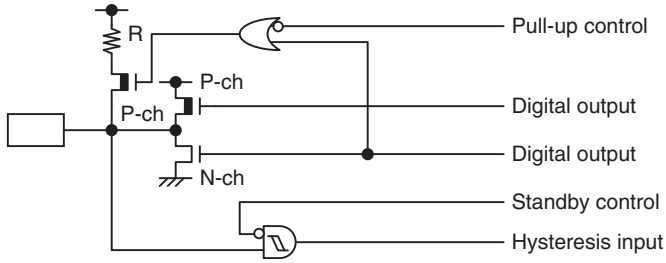
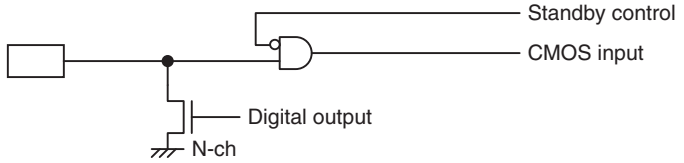
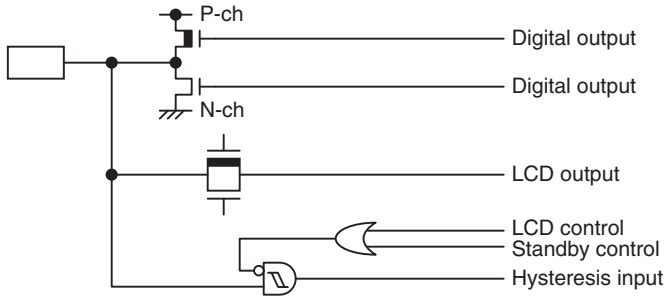
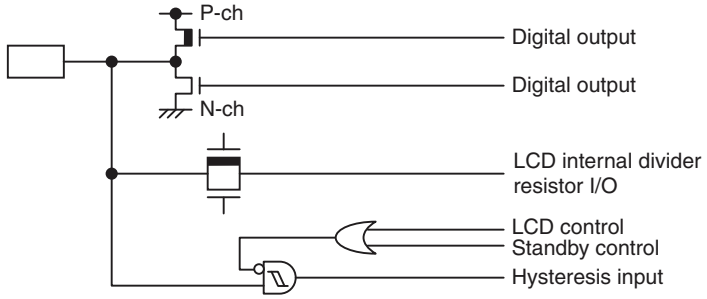
- Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.
  For details of current consumption, see “Electrical Characteristics”.

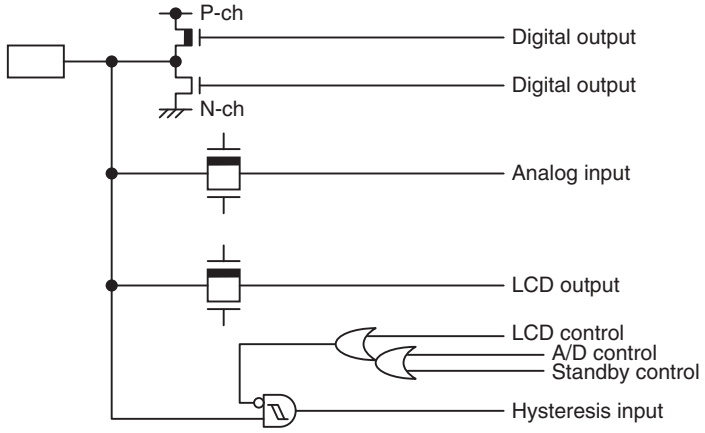
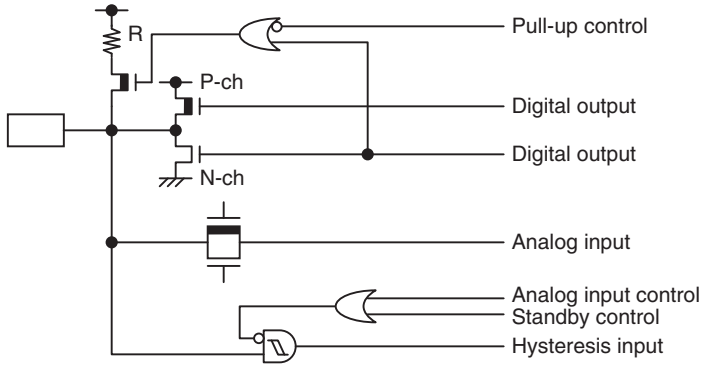
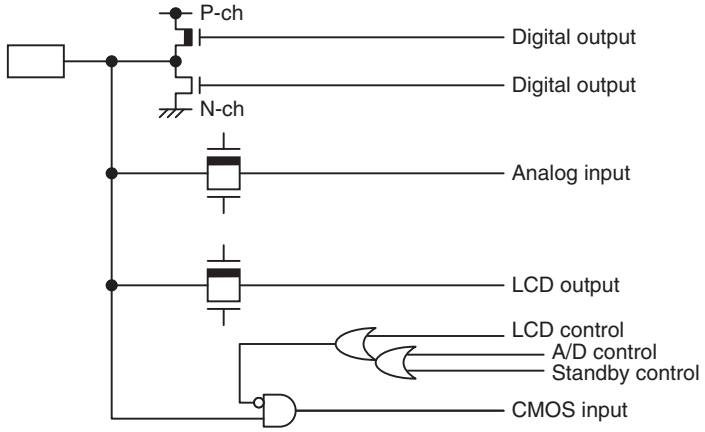
- Package
  For details of information on each package, see “Packages And Corresponding Products” and “Package Dimension”.

- Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of operating voltage, see “Electrical Characteristics”.

- On-chip debug function
  The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 26 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in “New 8FX MB95710M/770M Series Hardware Manual”.

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
38	PA5	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM5		LCDC COM5 output pin				
39	PA6	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM6		LCDC COM6 output pin				
40	PA7	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM7		LCDC COM7 output pin				
41	V_{SS}	—	Power supply pin (GND)	—	—	—	—
42	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
43	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
44	C	—	Decoupling capacitor connection pin	—	—	—	—
45	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				
46	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X0A		Subclock input oscillation pin				
47	V_{CC}	—	Power supply pin	—	—	—	—
48	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F714M/F716M/F718M				
49	P17	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	CMP0_O		Comparator ch. 0 digital output pin				
50	PB0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG00		LCDC SEG00 output pin				
51	PB1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG01		LCDC SEG01 output pin				
52	PC0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG02		LCDC SEG02 output pin				
53	PC1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG03		LCDC SEG03 output pin				
54	PC2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG04		LCDC SEG04 output pin				
55	PC3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG05		LCDC SEG05 output pin				
56	PC4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG06		LCDC SEG06 output pin				

Type	Circuit	Remarks
D		• N-ch open drain output • Hysteresis input
G		• CMOS output • CMOS input • Pull-up control
H		• CMOS output • Hysteresis input • Pull-up control
I		• N-ch open drain output • CMOS input
M		• CMOS output • LCD output • Hysteresis input
R		• CMOS output • LCD power supply • Hysteresis input

Type	Circuit	Remarks
S		• CMOS output • LCD output • Hysteresis input • Analog input
T		• CMOS output • Hysteresis input • Analog input • Pull-up control
V		• CMOS output • CMOS input • LCD output • Analog input

8. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

8.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- **Absolute Maximum Ratings**

  Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- **Recommended Operating Conditions**

  Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

  Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

  No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- **Processing and Protection of Pins**

  These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

  (1) Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

  (2) Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

  Therefore, avoid this type of connection.

  (3) Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- **Latch-up**

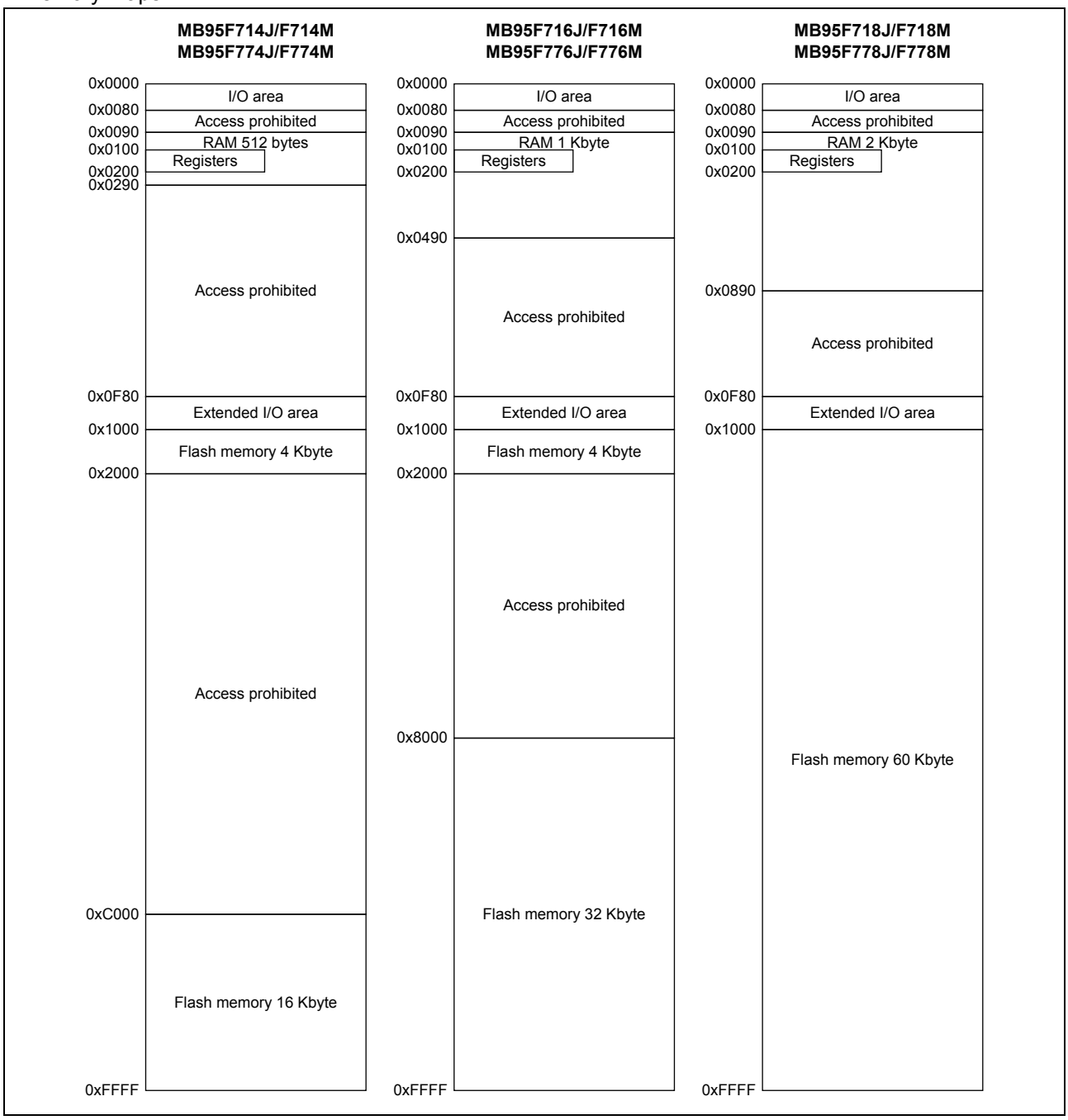
  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

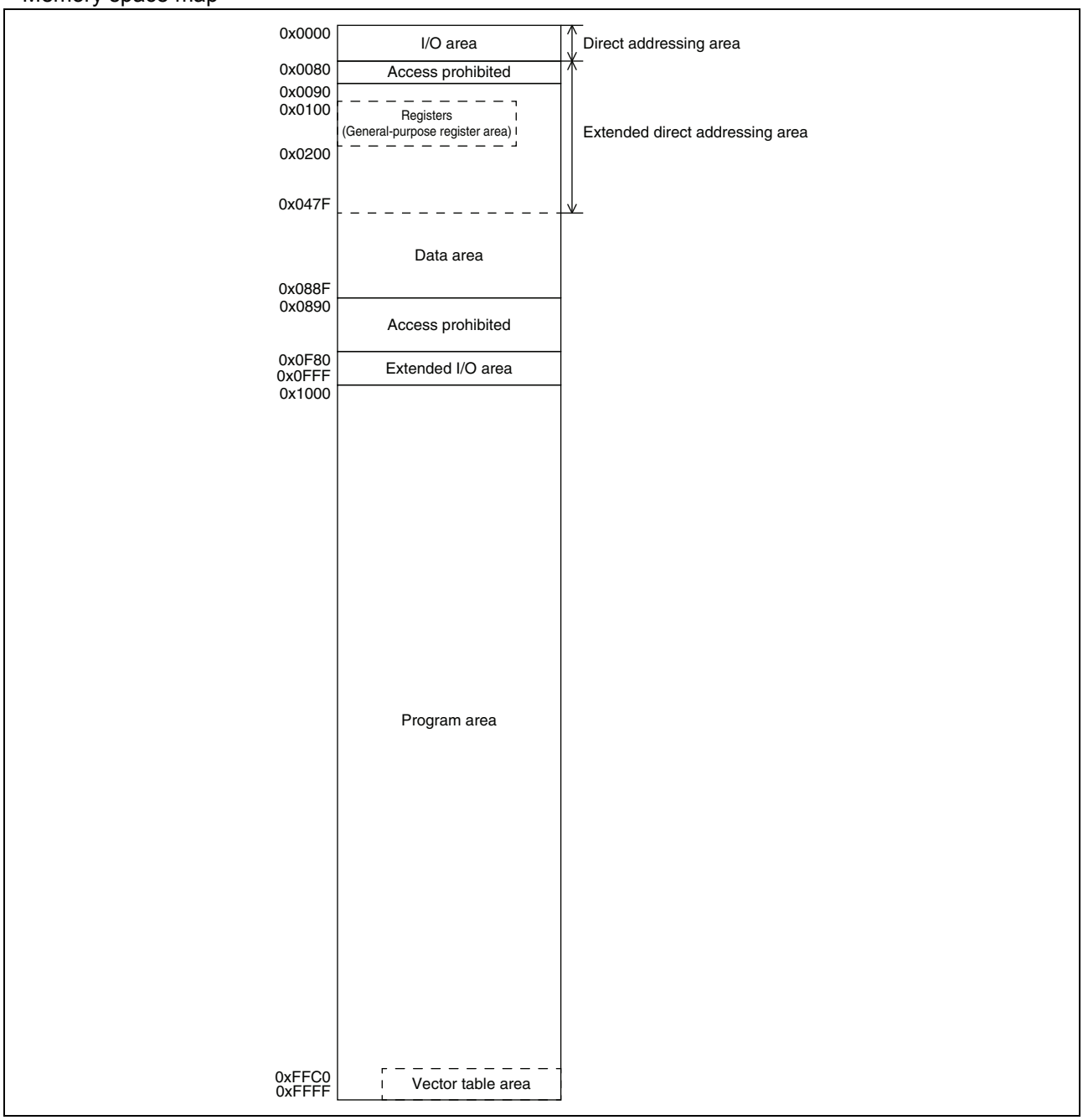
  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

13. CPU Core

- Memory space
  The memory space of the MB95710M/770M Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95710M/770M Series are shown below.
- Memory maps



- Memory space map



16. I/O Map (MB95710M Series)

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E	PDR2	Port 2 data register	R/W	0b00000000
0x000F	DDR2	Port 2 direction register	R/W	0b00000000
0x0010, 0x0011	—	(Disabled)	—	—
0x0012	PDR4	Port 4 data register	R/W	0b00000000
0x0013	DDR4	Port 4 direction register	R/W	0b00000000
0x0014	PDR5	Port 5 data register	R/W	0b00000000
0x0015	DDR5	Port 5 direction register	R/W	0b00000000
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018 to 0x001B	—	(Disabled)	—	—
0x001C	PDR9	Port 9 data register	R/W	0b00000000
0x001D	DDR9	Port 9 direction register	R/W	0b00000000
0x001E	PDRA	Port A data register	R/W	0b00000000
0x001F	DDRA	Port A direction register	R/W	0b00000000
0x0020	PDRB	Port B data register	R/W	0b00000000
0x0021	DDRB	Port B direction register	R/W	0b00000000
0x0022	PDRC	Port C data register	R/W	0b00000000
0x0023	DDRC	Port C direction register	R/W	0b00000000
0x0024, 0x0025	—	(Disabled)	—	—

Address	Register abbreviation	Register name	R/W	Initial value
0x0FA7	TMRL0	16-bit reload timer timer register (lower) ch. 0	R/W	0b00000000
	TMRLRL0	16-bit reload timer reload register (lower) ch. 0		
0x0FA8	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FA9	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FAA	PSSR1	UART/SIO dedicated baud rate generator prescaler select register ch. 1	R/W	0b00000000
0x0FAB	BRSR1	UART/SIO dedicated baud rate generator baud rate setting register ch. 1	R/W	0b00000000
0x0FAC	PSSR2	UART/SIO dedicated baud rate generator prescaler select register ch. 2	R/W	0b00000000
0x0FAD	BRSR2	UART/SIO dedicated baud rate generator baud rate setting register ch. 2	R/W	0b00000000
0x0FAE	—	(Disabled)	—	—
0x0FAF	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FB0	LCDCC1	LCDC control register 1	R/W	0b00000000
0x0FB1	—	(Disabled)	—	—
0x0FB2	LCDCE1	LCDC enable register 1	R/W	0b00111110
0x0FB3	LCDCE2	LCDC enable register 2	R/W	0b00000000
0x0FB4	LCDCE3	LCDC enable register 3	R/W	0b00000000
0x0FB5	LCDCE4	LCDC enable register 4	R/W	0b00000000
0x0FB6	LCDCE5	LCDC enable register 5	R/W	0b00000000
0x0FB7	LCDCE6	LCDC enable register 6	R/W	0b00000000
0x0FB8	—	(Disabled)	—	—
0x0FB9	LCDCB1	LCDC blinking setting register 1	R/W	0b00000000
0x0FBA	LCDCB2	LCDC blinking setting register 2	R/W	0b00000000
0x0FBB, 0x0FBC	—	(Disabled)	—	—
0x0FBD to 0x0FD8	LCDRAM	LCDC display RAM (28 bytes)	R/W	0b00000000
0x0FD9 to 0x0FE1	—	(Disabled)	—	—
0x0FE2	EVCR	Event counter control register	R/W	0b00000000
0x0FE3	WCDR	Watch counter data register	R/W	0b00111111
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	SYSC2	System configuration register 2	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b00111111
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	—	(Disabled)	—	—
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	—	(Disabled)	—	—

- R/W access symbols
  R/W : Readable/Writable
  R : Read only
- Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

18.8.4 Port A operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRA register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRA register to external pins.
  - If data is written to the PDRA register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRA register returns the PDRA register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRA register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRA register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRA register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRA register, the PDRA register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC common output pin
  - Set the bit in the DDRA register corresponding to an LCDC common output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC common output pin, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to “1” to select the LCDC common output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDRA register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRA register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.10.4 Port C operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRC register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRC register to external pins.
  - If data is written to the PDRC register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRC register returns the PDRC register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:02]) or in the LCDC enable register 4 (LCDCE4:SEG[09:08]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRC register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRC register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRC register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRC register, the PDRC register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:02]) or in the LCDC enable register 4 (LCDCE4:SEG[09:08]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC segment output pin
  - Set the bit in the DDRC register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:02]) or in the LCDC enable register 4 (LCDCE4:SEG[09:08]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDRC register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRC register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.11 Port E

Port E is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.11.1 Port E configuration

Port E is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port E data register (PDRE)
- Port E direction register (DDRE)

18.11.2 Block diagrams of port E

- PE0/SEG22 pin

  This pin has the following peripheral function:
  - LCDC SEG22 output pin (SEG22)

- PE1/SEG23 pin

  This pin has the following peripheral function:
  - LCDC SEG23 output pin (SEG23)

- PE2/SEG24 pin

  This pin has the following peripheral function:
  - LCDC SEG24 output pin (SEG24)

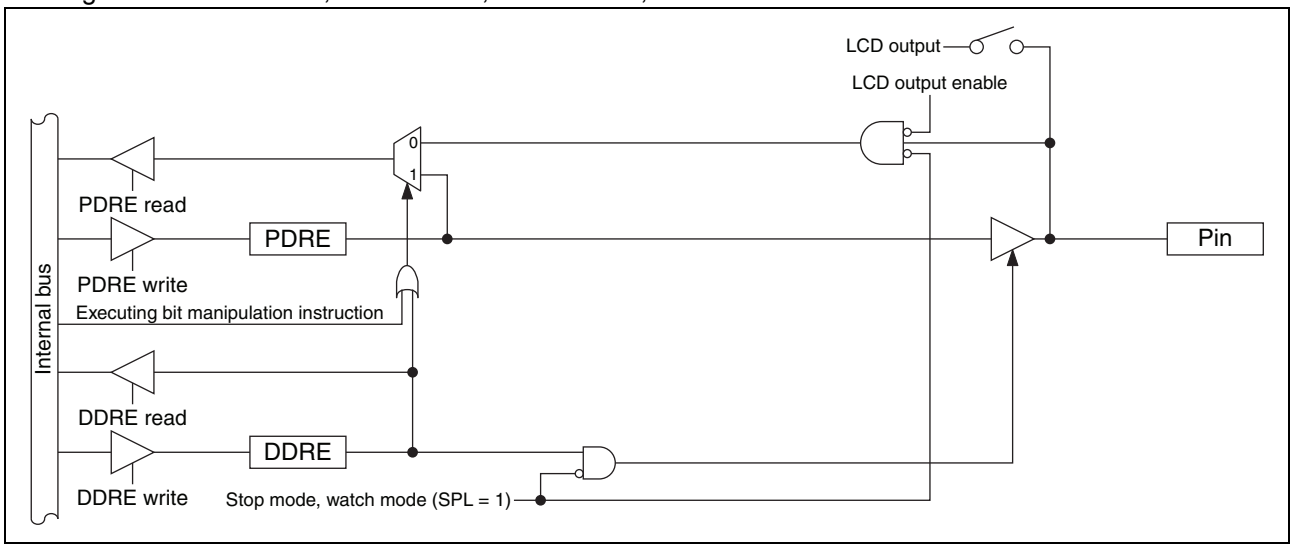
- PE3/SEG25 pin

  This pin has the following peripheral function:
  - LCDC SEG25 output pin (SEG25)

- PE4/SEG26 pin

  This pin has the following peripheral function:
  - LCDC SEG26 output pin (SEG26)

- Block diagram of PE0/SEG22, PE1/SEG23, PE2/SEG24, PE3/SEG25 and PE4/SEG26



19.5 Port 9

Port 9 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.5.1 Port 9 configuration

Port 9 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 9 data register (PDR9)
- Port 9 direction register (DDR9)

19.5.2 Block diagrams of port 9

- P90/V4 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V4)

- P91/V3 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V3)

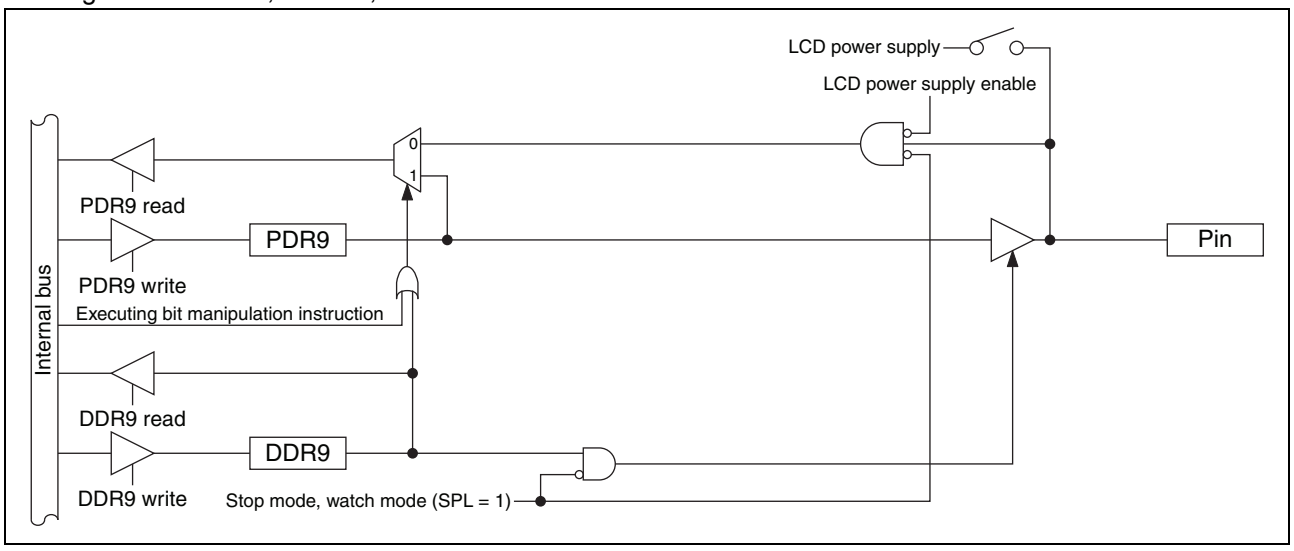
- P92/V2 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V2)

- P93/V1 pin

  This pin has the following peripheral function:
  - LCD drive power supply pin (V1)

- Block diagram of P90/V4, P91/V3, P92/V2 and P93/V1



19.10.4 Port F operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
  - If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRF register returns the PDRF register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.11 Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.11.1 Port G configuration

Port G is made up of the following elements.

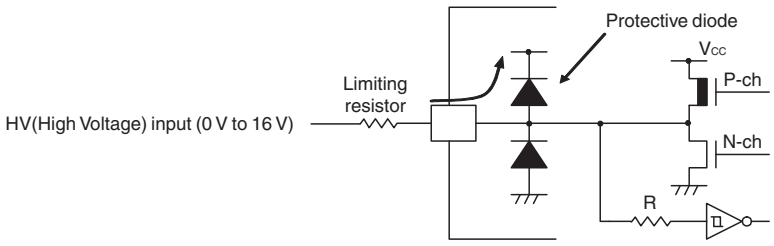
- General-purpose I/O pins/peripheral function I/O pins
- Port G data register (PDRG)
- Port G direction register (DDRG)
- Port G pull-up register (PULG)

19.11.2 Block diagram of port G

- PG1/X0A pin
  This pin has the following peripheral function:
  - Subclock input oscillation pin (X0A)

- PG2/X1A pin
  This pin has the following peripheral function:
  - Subclock I/O oscillation pin (X1A)

- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:
  - Input/Output equivalent circuit



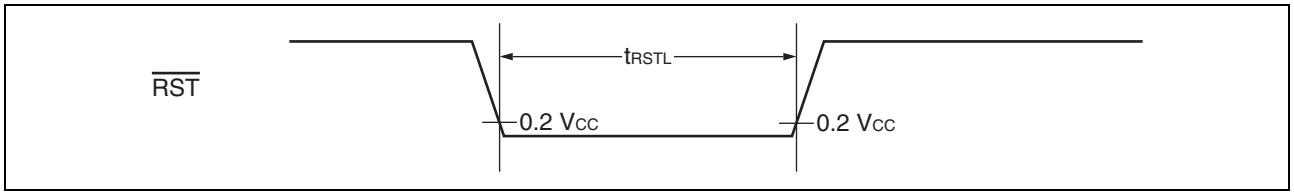
WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

22.4.3 External Reset

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*	—	ns	

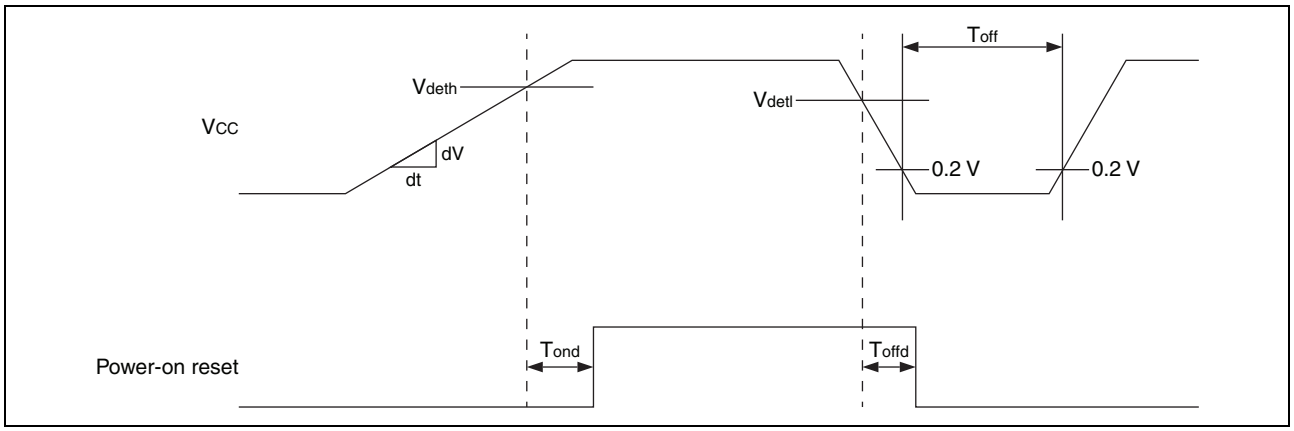
*: See "Source Clock/Machine Clock" for t_{MCLK}.



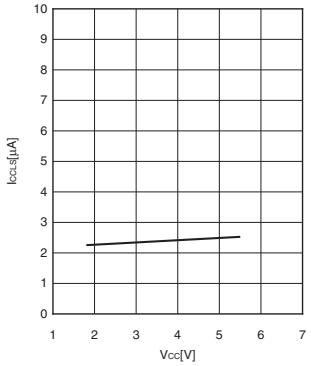
22.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

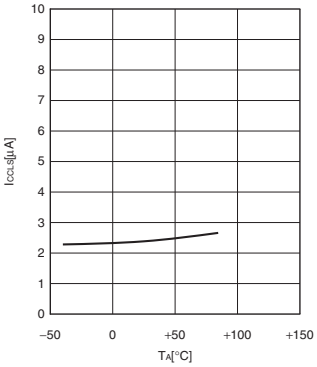
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply rising time	dV/dt	V_{CC}	0.1	—	—	V/ms	
Power supply cutoff time	T_{off}		1	—	—	ms	
Reset release voltage	V_{deth}		1.44	1.60	1.76	V	At voltage rise
Reset detection voltage	V_{detl}		1.39	1.55	1.71	V	At voltage fall
Reset release delay time	T_{ond}		—	—	10	ms	dV/dt ≥ 0.1 mV/µs
Reset detection delay time	T_{offd}		—	—	0.4	ms	dV/dt ≥ –0.04 mV/µs



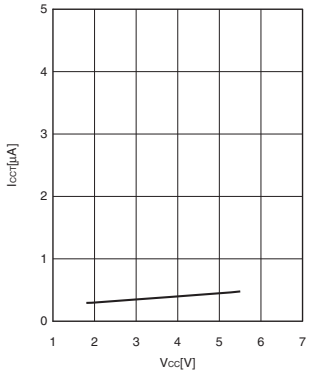
I_{CCLS} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



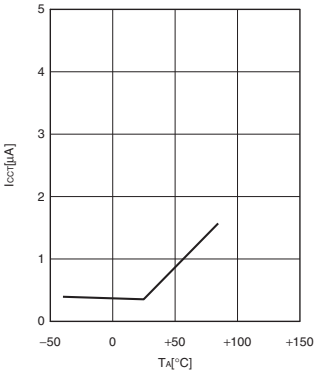
I_{CCLS} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



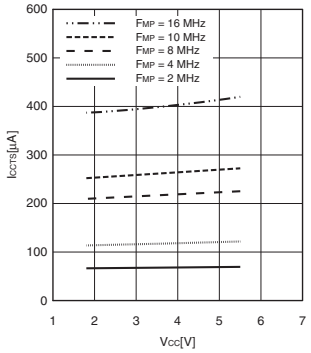
I_{CCT} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



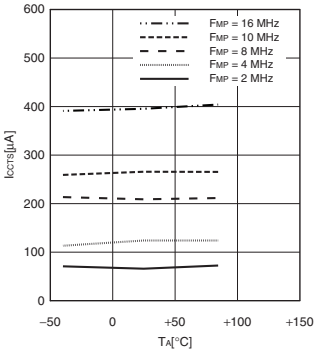
I_{CCT} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



I_{CCTS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating

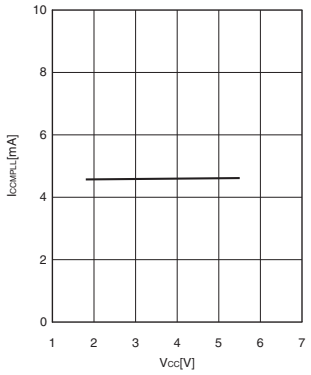


I_{CCTS} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating

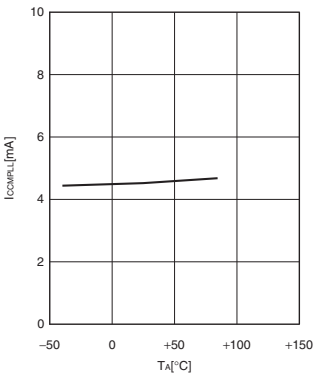


(Continued)

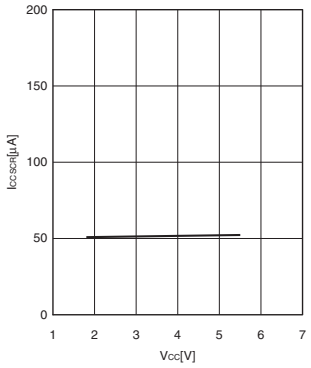
I_{CCMPLL} – V_{CC}
T_A = +25 °C, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main PLL clock mode



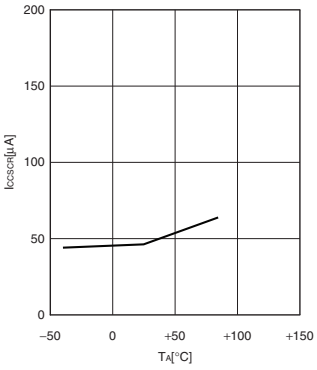
I_{CCMPLL} – T_A
V_{CC} = 3.3 V, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main PLL clock mode



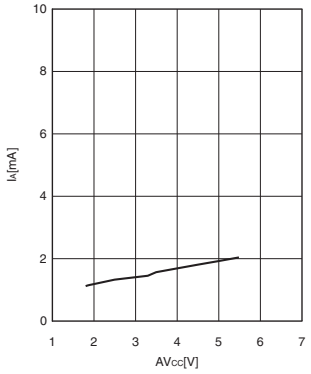
I_{CCSCR} – V_{CC}
T_A = +25 °C, F_{MPL} = 50 kHz (divided by 2)
Sub-CR clock mode



I_{CCSCR} – T_A
V_{CC} = 3.3 V, F_{MPL} = 50 kHz (divided by 2)
Sub-CR clock mode



I_A – AV_{CC}
T_A = +25 °C, F_{MP} = 16 MHz (divided by 2)
Main clock mode with the external clock operating



I_A – T_A
V_{CC} = 3.3 V, F_{MP} = 16 MHz (divided by 2)
Main clock mode with the external clock operating