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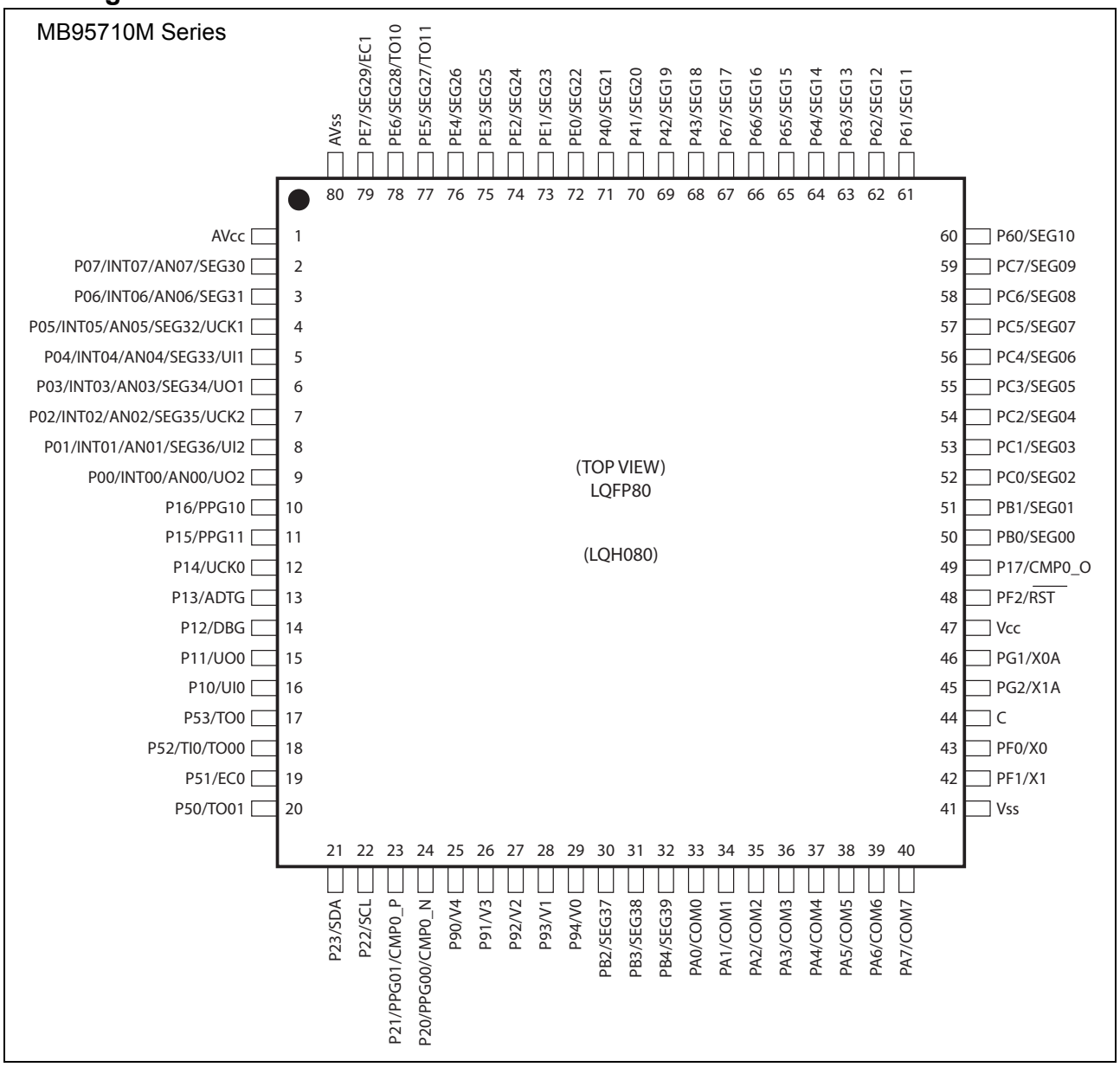
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f778mpmc1-g-sne2

4. Pin Assignment

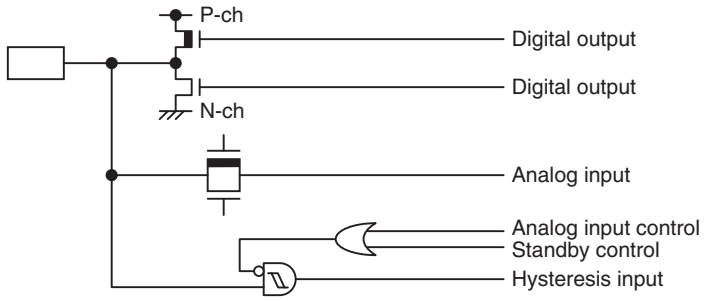
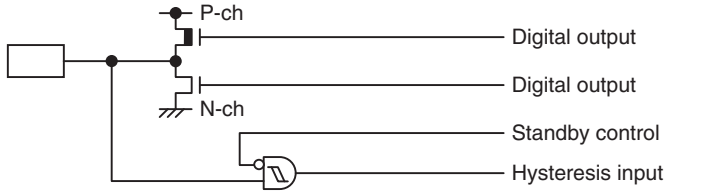


Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
24	P20	T	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	PPG00		8/16-bit PPG ch. 0 output pin				
	CMP0_N		Comparator ch. 0 inverting analog input (negative input) pin				
25	P90	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V4		LCD drive power supply pin				
26	P91	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V3		LCD drive power supply pin				
27	P92	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V2		LCD drive power supply pin				
28	P93	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V1		LCD drive power supply pin				
29	P94	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V0		LCD drive power supply pin				
30	PB2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG37		LCDC SEG37 output pin				
31	PB3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG38		LCDC SEG38 output pin				
32	PB4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG39		LCDC SEG39 output pin				
33	PA0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM0		LCDC COM0 output pin				
34	PA1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM1		LCDC COM1 output pin				
35	PA2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM2		LCDC COM2 output pin				
36	PA3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM3		LCDC COM3 output pin				
37	PA4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM4		LCDC COM4 output pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
75	PE3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG25		LCDC SEG25 output pin				
76	PE4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG26		LCDC SEG26 output pin				
77	PE5	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG27		LCDC SEG27 output pin				
	TO11		8/16-bit composite timer ch. 1 output pin				
78	PE6	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG28		LCDC SEG28 output pin				
	TO10		8/16-bit composite timer ch. 1 output pin				
79	PE7	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	SEG29		LCDC SEG27 output pin				
	EC1		8/16-bit composite timer ch. 1 clock input pin				
80	AV_{SS}	—	Power supply pin (GND) for 8/12-bit A/D converter and comparator	—	—	—	—

O: Available

*1: For the I/O circuit types, see “I/O Circuit Type”.
*2: N-ch open drain
*3: Pull-up

Type	Circuit	Remarks
W		• CMOS output • Hysteresis input • Analog input
Y		• CMOS output • Hysteresis input

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

- **Observance of Safety Regulations and Standards**

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- **Fail-Safe Design**

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- **Precautions Related to Usage of Devices**

  Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

8.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- **Lead Insertion Type**

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- **Surface Mount Type**

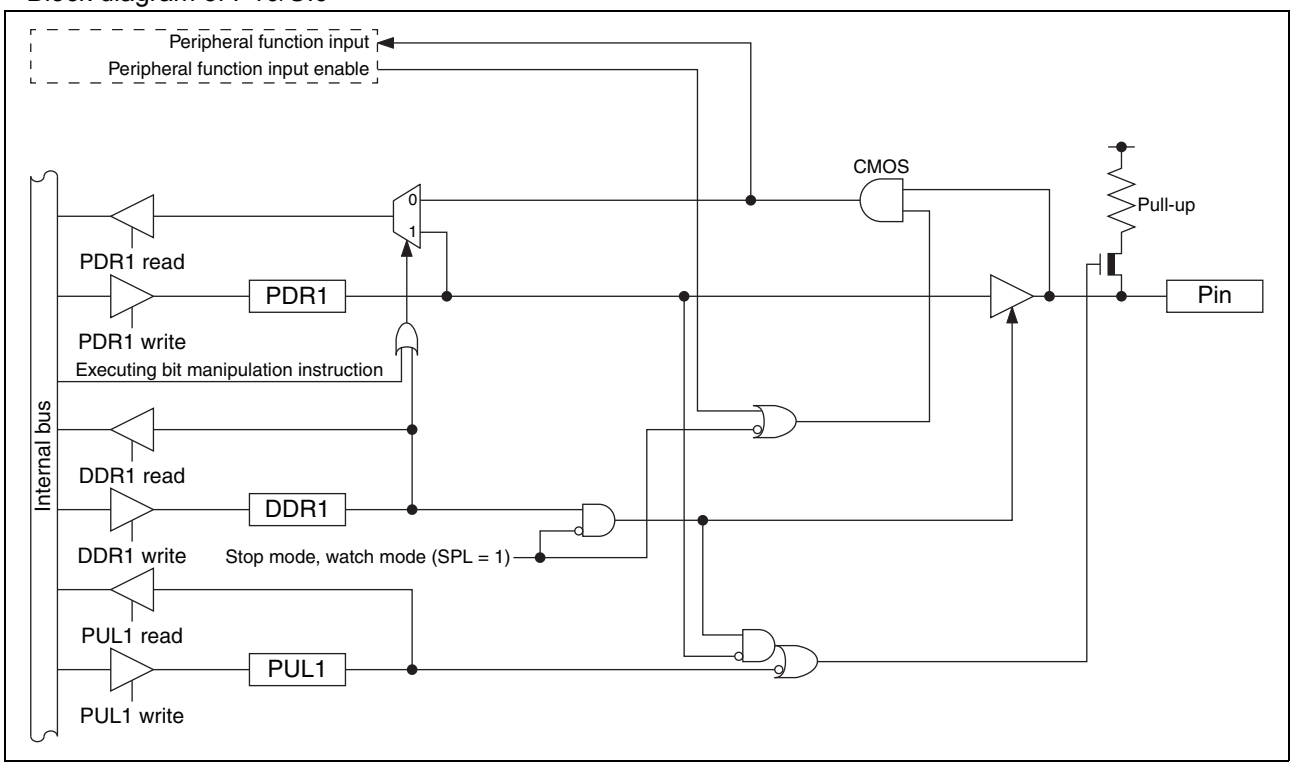
  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

- **Lead-Free Packaging**

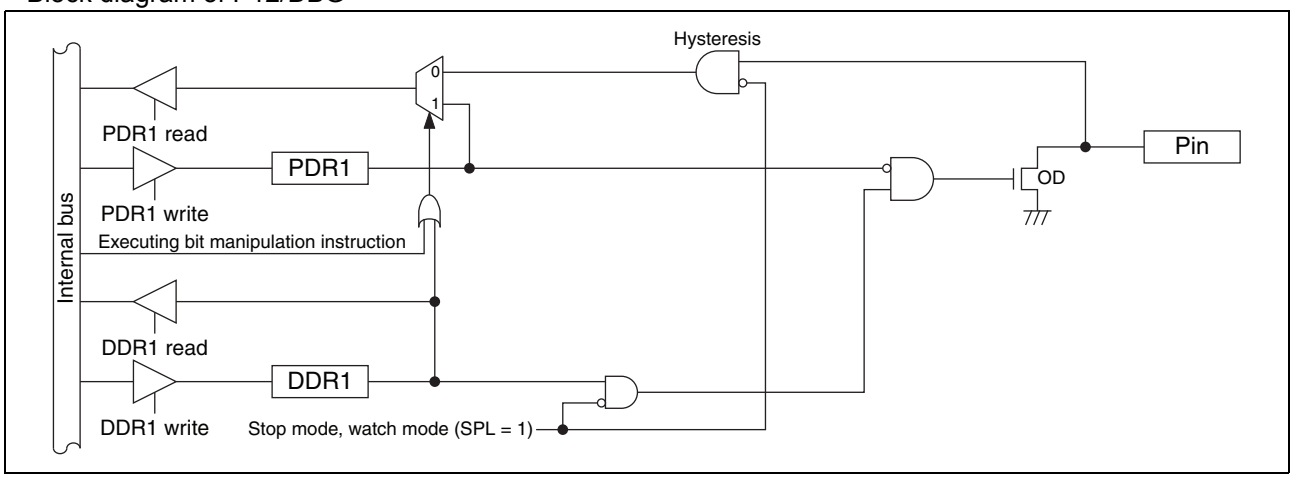
  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Block diagram of P10/UI0



- P12/DBG pin
  This pin has the following peripheral function:
  - DBG input pin (DBG)

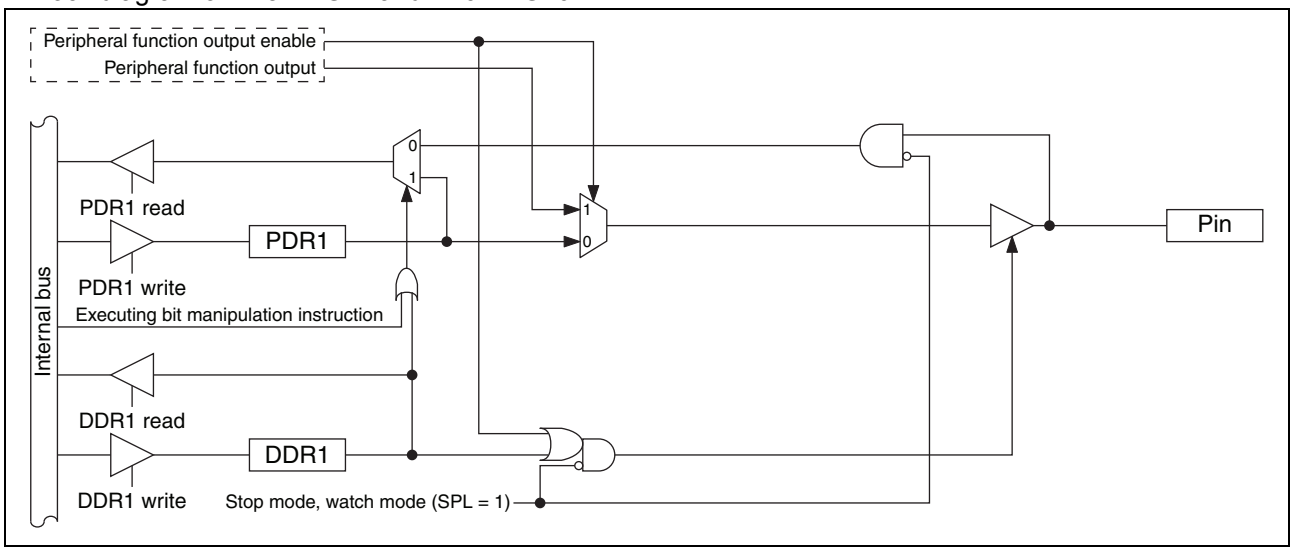
- Block diagram of P12/DBG



- P15/PPG11 pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 1 output pin (PPG11)

- P16/PPG10 pin
  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 1 output pin (PPG10)

- Block diagram of P15/PPG11 and P16/PPG10



18.2.3 Port 1 registers

- Port 1 register functions

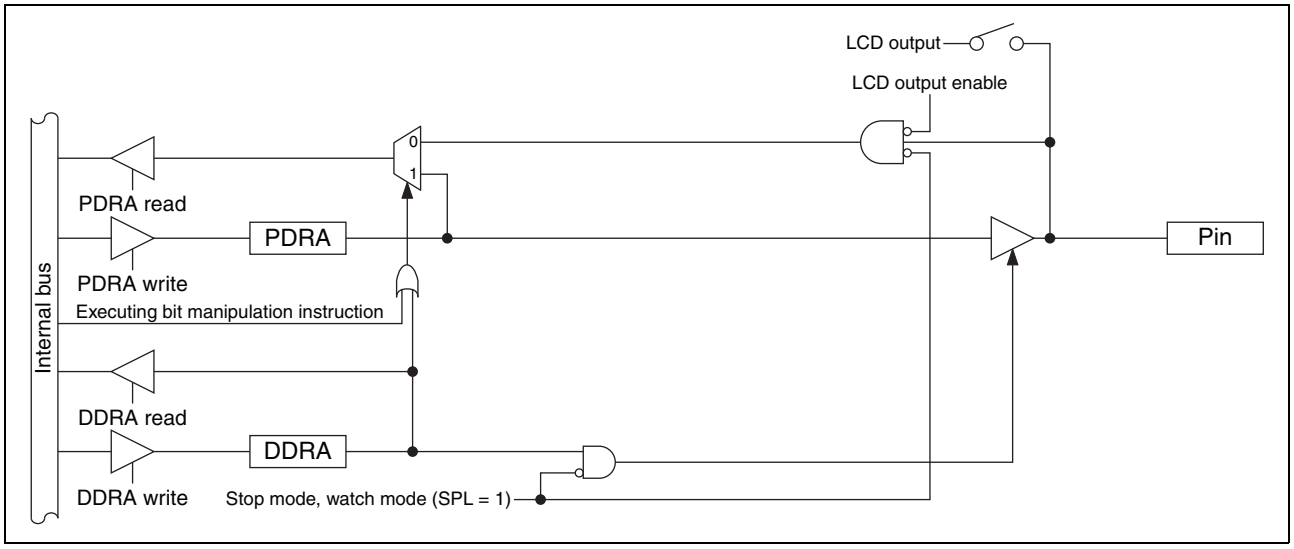
Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port 1

	Correspondence between related register bits and pins							
Pin name	P17	P16	P15	P14	P13	P12	P11	P10
PDR1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR1								
PUL1		-	-			-		

- Block diagram of PA0/COM0, PA1/COM1, PA2/COM2, PA3/COM3, PA4/COM4, PA5/COM5, PA6/COM6 and PA7/COM7



18.8.3 Port A registers

- Port A register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRA	0	Pin state is “L” level.	PDRA value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRA value is “1”.	As output port, outputs “H” level.
DDRA	0	Port input enabled		
	1	Port output enabled		

- Correspondence between registers and pins for port A

	Correspondence between related register bits and pins							
Pin name	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PDRA	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDRA								

18.9 Port B

Port B is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

18.9.1 Port B configuration

Port B is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port B data register (PDRB)
- Port B direction register (DDRB)

18.9.2 Block diagrams of port B

- PB0/SEG00 pin

  This pin has the following peripheral function:
  - LCDC SEG00 output pin (SEG00)

- PB1/SEG01 pin

  This pin has the following peripheral function:
  - LCDC SEG01 output pin (SEG01)

- PB2/SEG37 pin

  This pin has the following peripheral function:
  - LCDC SEG37 output pin (SEG37)

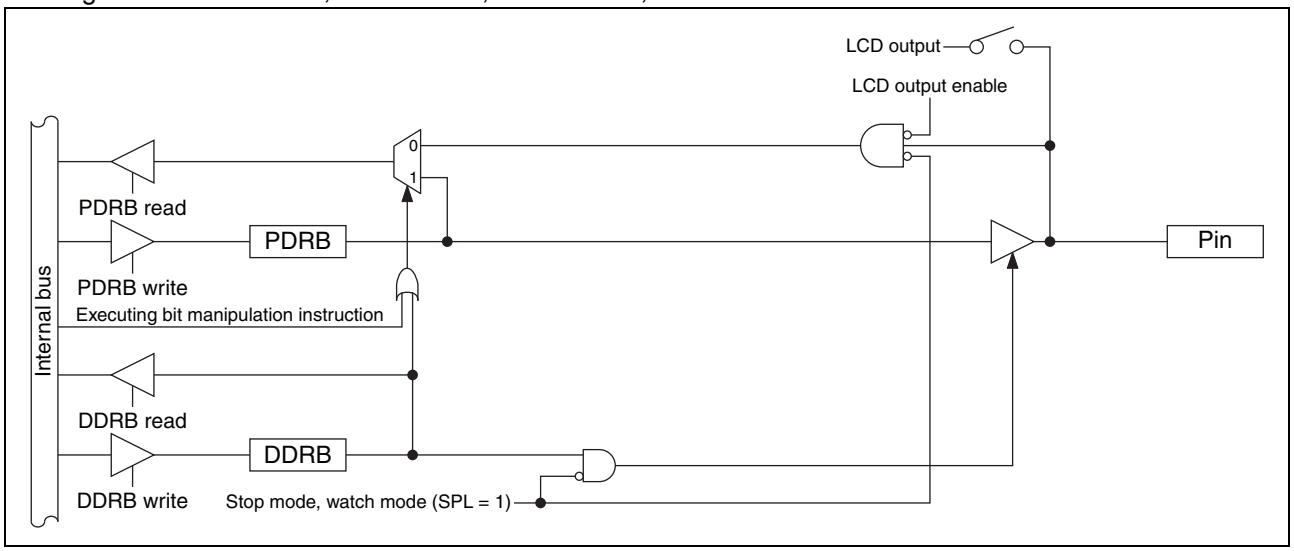
- PB3/SEG38 pin

  This pin has the following peripheral function:
  - LCDC SEG38 output pin (SEG38)

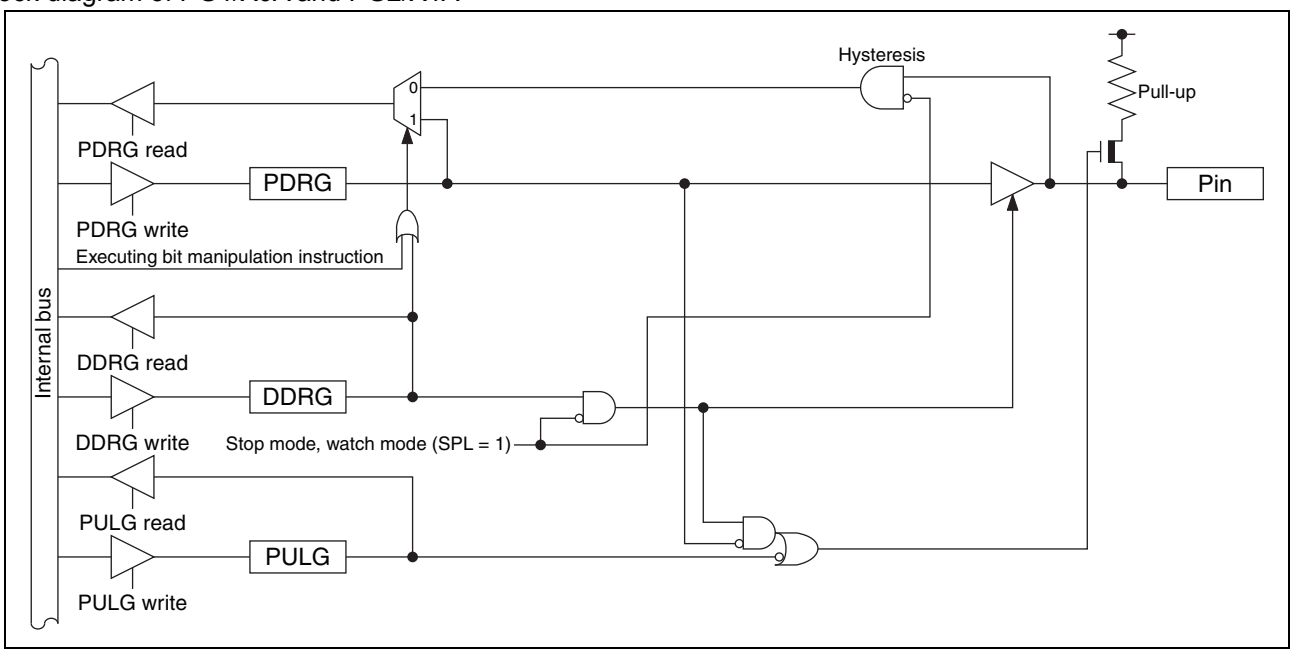
- PB4/SEG39 pin

  This pin has the following peripheral function:
  - LCDC SEG39 output pin (SEG39)

- Block diagram of PB0/SEG00, PB1/SEG01, PB2/SEG37, PB3/SEG38 and PB4/SEG39



- Block diagram of PG1/X0A and PG2/X1A



18.13.3 Port G registers

- Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

- Correspondence between registers and pins for port G

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PG2**	**PG1**	**-**
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

19. I/O Ports (MB95770M Series)

- List of port registers

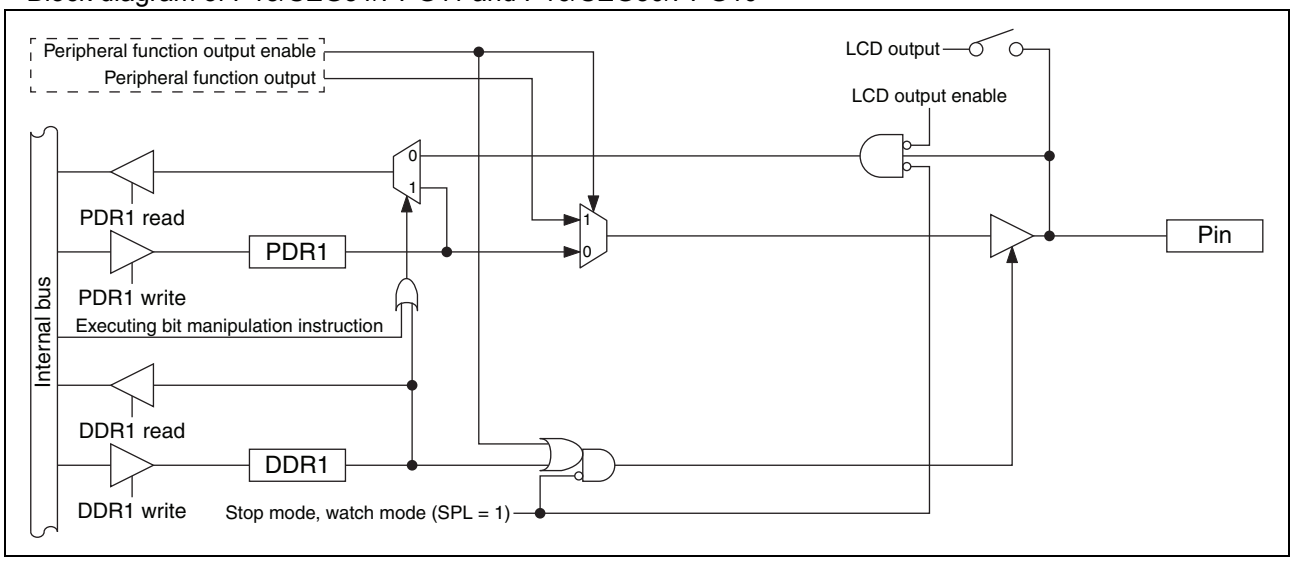
Register name		Read/Write	Initial value
Port 0 data register	PDR0	R, RM/W	0b00000000
Port 0 direction register	DDR0	R/W	0b00000000
Port 1 data register	PDR1	R, RM/W	0b00000000
Port 1 direction register	DDR1	R/W	0b00000000
Port 2 data register	PDR2	R, RM/W	0b00000000
Port 2 direction register	DDR2	R/W	0b00000000
Port 6 data register	PDR6	R, RM/W	0b00000000
Port 6 direction register	DDR6	R/W	0b00000000
Port 9 data register	PDR9	R, RM/W	0b00000000
Port 9 direction register	DDR9	R/W	0b00000000
Port A data register	PDRA	R, RM/W	0b00000000
Port A direction register	DDRA	R/W	0b00000000
Port B data register	PDRB	R, RM/W	0b00000000
Port B direction register	DDRB	R/W	0b00000000
Port C data register	PDRC	R, RM/W	0b00000000
Port C direction register	DDRC	R/W	0b00000000
Port E data register	PDRE	R, RM/W	0b00000000
Port E direction register	DDRE	R/W	0b00000000
Port F data register	PDRF	R, RM/W	0b00000000
Port F direction register	DDRF	R/W	0b00000000
Port G data register	PDRG	R, RM/W	0b00000000
Port G direction register	DDRG	R/W	0b00000000
Port 1 pull-up register	PUL1	R/W	0b00000000
Port 2 pull-up register	PUL2	R/W	0b00000000
Port G pull-up register	PULG	R/W	0b00000000
A/D input disable register (lower)	AIDRL	R/W	0b00000000

R/W : Readable/writable (The read value is the same as the write value.)
R, RM/W : Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)

- P15/SEG31/PPG11 pin
  This pin has the following peripheral functions:
  - LCDC SEG31 output pin (SEG31)
  - 8/16-bit PPG ch. 1 output pin (PPG11)

- P16/SEG30/PPG10 pin
  This pin has the following peripheral functions:
  - LCDC SEG30 output pin (SEG30)
  - 8/16-bit PPG ch. 1 output pin (PPG10)

- Block diagram of P15/SEG31/PPG11 and P16/SEG30/PPG10



19.2.3 Port 1 registers

- Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port 1

	Correspondence between related register bits and pins							
Pin name	P17	P16	P15	P14	P13	P12	P11	P10
PDR1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR1								
PUL1		-	-			-		

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P10/UI0/TO0 and P14/UCK0/EC0/TI0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL1 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

19.3 Port 2

Port 2 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.3.1 Port 2 configuration

Port 2 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 2 data register (PDR2)
- Port 2 direction register (DDR2)
- Port 2 pull-up register (PUL2)

19.3.2 Block diagrams of port 2

- P20/PPG00/CMP0_N pin
  This pin has the following peripheral functions:
  - 8/16-bit PPG ch. 0 output pin (PPG00)
  - Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)

- P21/PPG01/CMP0_P pin
  This pin has the following peripheral functions:
  - 8/16-bit PPG ch. 0 output pin (PPG01)
  - Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0_P)

19.4.4 Port 6 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
  - If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR6 register returns the PDR6 register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC segment output pin
  - Set the bit in the DDR6 register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDR6 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.6 Port A

Port A is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.6.1 Port A configuration

Port A is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port A data register (PDRA)
- Port A direction register (DDRA)

19.6.2 Block diagrams of port A

- PA0/COM0 pin
  This pin has the following peripheral function:
  - LCDC COM0 output pin (COM0)

- PA1/COM1 pin
  This pin has the following peripheral function:
  - LCDC COM1 output pin (COM1)

- PA2/COM2 pin
  This pin has the following peripheral function:
  - LCDC COM2 output pin (COM2)

- PA3/COM3 pin
  This pin has the following peripheral function:
  - LCDC COM3 output pin (COM3)

- PA4/COM4 pin
  This pin has the following peripheral function:
  - LCDC COM4 output pin (COM4)

- PA5/COM5 pin
  This pin has the following peripheral function:
  - LCDC COM5 output pin (COM5)

- PA6/COM6 pin
  This pin has the following peripheral function:
  - LCDC COM6 output pin (COM6)

- PA7/COM7 pin
  This pin has the following peripheral function:
  - LCDC COM7 output pin (COM7)

21. Pin States In Each Mode

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*1
	I/O port*2	I/O port*2	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Hi-Z - Input enabled*4 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*1
	I/O port*2	I/O port*2	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Hi-Z - Input enabled*4 (However, it does not function.)
PF2/$\overline{\text{RST}}$	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input*5
	I/O port*2	I/O port*2	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Previous state kept - Input blocked*2, *3	- Hi-Z - Input blocked*2, *3	- Hi-Z - Input enabled*4 (However, it does not function.)
PG1/X0A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*6
	I/O port*2	I/O port*2	- Previous state kept - Input blocked*2, *3	- Hi-Z*7 - Input blocked*2, *3	- Previous state kept - Input blocked*2, *3	- Hi-Z*7 - Input blocked*2, *3	- Hi-Z - Input enabled*4 (However, it does not function.)
PG2/X1A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*6
	I/O port*2	I/O port*2	- Previous state kept - Input blocked*2, *3	- Hi-Z*7 - Input blocked*2, *3	- Previous state kept - Input blocked*2, *3	- Hi-Z*7 - Input blocked*2, *3	- Hi-Z - Input enabled*4 (However, it does not function.)
P00/INT00/ AN00/ SEG29*8/ UO2 P01/INT01/ AN01/ SEG28*8/ SEG36*8/ TO00*9/UI2 P02/INT02/ AN02/ SEG27*8/ SEG35*8/ UCK2 P03/INT03/ AN03/ SEG26*8/ SEG34*8/ UO1	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*3, *10	- Hi-Z - Input blocked*3, *10	- Previous state kept - Input blocked*3, *10	- Hi-Z - Input blocked*3, *10	- Hi-Z - Input blocked*3

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P04/INT04/ AN04/ SEG25*8/ SEG33*8/ UI1 P05/INT05/ AN05/ SEG24*8/ SEG32*8/ UCK1 P06/INT06/ AN06/ SEG23*8/ SEG31*8 P07/INT07/ AN07/ SEG22*8/ SEG30*8	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*3, *10	- Hi-Z - Input blocked*3, *10	- Previous state kept - Input blocked*3, *10	- Hi-Z - Input blocked*3, *10	- Hi-Z - Input blocked*3
P10/UI0/ TO0*9 P11/UO0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Hi-Z - Input enabled*4 (However, it does not function.)
P12/DBG	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	“H”	- Previous state kept - Input blocked*3	“H”	“H”
P13/ADTG/ TO01*9 P14/UCK0/ EC0*9/TI0*9	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Hi-Z - Input enabled*4 (However, it does not function.)
P15/ SEG31*8/ PPG11 P16/ SEG30*8/ PPG10	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Hi-Z - Input blocked*3
P17/ CMP0_O	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept*11 - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Previous state kept*11 - Input blocked*3	- Hi-Z*7 - Input blocked*3	- Hi-Z - Input enabled*4 (However, it does not function.)
P20/ PPG00/ CMP0_N P21/ PPG01/ CMP0_P	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*3, *12	- Hi-Z*7 - Input blocked*3, *12	- Previous state kept - Input blocked*3, *12	- Hi-Z*7 - Input blocked*3, *12	- Hi-Z - Input enabled*4
P22/SCL P23/SDA	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3, *13	- Hi-Z - Input blocked*3, *13	- Previous state kept - Input blocked*3, *13	- Hi-Z - Input blocked*3, *13	- Hi-Z - Input enabled*4

22. Electrical Characteristics

22.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	–2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average current	I_{OLAV}	—	4	mA	Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average current	I_{OHAV}	—	–4	mA	Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{stg}	–55	+150	°C	

*1: These parameters are based on the condition that V_{SS} is 0.0 V.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Specific pins: P00 to P07, P10, P11, P13 to P16, P20 to P22, P40 to P43, P50 to P53, P60 to P67, P90 to P94, PA0 to PA7, PB0 to PB4, PC0 to PC7, PE0 to PE7, PF0, PF1, PG1, PG2 (P40 to P43, P50 to P53, P94, PB2 to PB4 and PC4 to PC7 are only available on the MB95710M Series.)

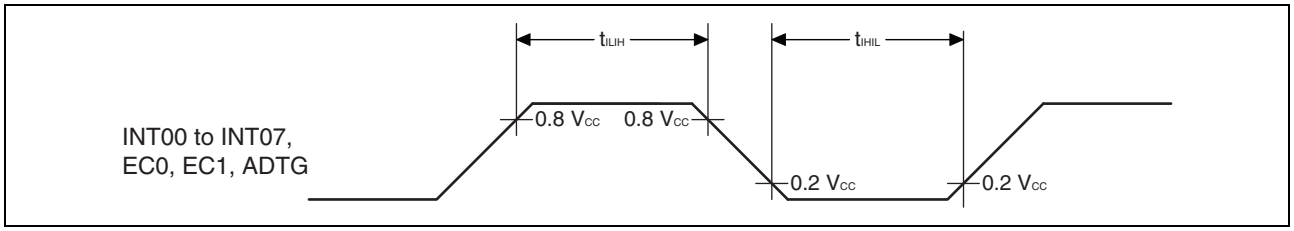
- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.

22.4.5 Peripheral Input Timing

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, ADTG	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.



22.4.6 Low-voltage Detection

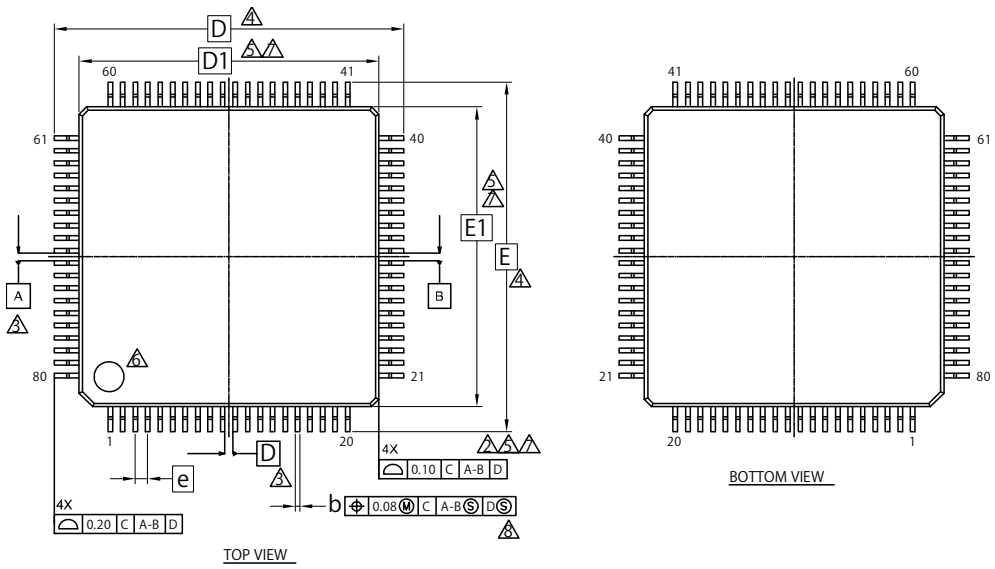
• Normal mode

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Reset release voltage	V_{PDL+}	1.88	2.03	2.18	V	At power supply rise
Reset detection voltage	$V_{PDL–}$	1.8	1.93	2.06	V	At power supply fall
Interrupt release voltage 0	V_{IDL0+}	2.13	2.3	2.47	V	At power supply rise
Interrupt detection voltage 0	$V_{IDL0–}$	2.05	2.2	2.35	V	At power supply fall
Interrupt release voltage 1	V_{IDL1+}	2.41	2.6	2.79	V	At power supply rise
Interrupt detection voltage 1	$V_{IDL1–}$	2.33	2.5	2.67	V	At power supply fall
Interrupt release voltage 2	V_{IDL2+}	2.69	2.9	3.11	V	At power supply rise
Interrupt detection voltage 2	$V_{IDL2–}$	2.61	2.8	2.99	V	At power supply fall
Interrupt release voltage 3	V_{IDL3+}	3.06	3.3	3.54	V	At power supply rise
Interrupt detection voltage 3	$V_{IDL3–}$	2.98	3.2	3.42	V	At power supply fall
Interrupt release voltage 4	V_{IDL4+}	3.43	3.7	3.97	V	At power supply rise
Interrupt detection voltage 4	$V_{IDL4–}$	3.35	3.6	3.85	V	At power supply fall
Interrupt release voltage 5	V_{IDL5+}	3.81	4.1	4.39	V	At power supply rise
Interrupt detection voltage 5	$V_{IDL5–}$	3.73	4	4.27	V	At power supply fall
Power supply start voltage	V_{off}	—	—	1.6	V	
Power supply end voltage	V_{on}	4.39	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	697.5	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{PDL+}/V_{IDL+})
Power supply voltage change time (at power supply fall)	t_f	697.5	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{PDL-}/V_{IDL-})
Reset release delay time	t_{dp1}	—	—	30	µs	
Reset detection delay time	t_{dp2}	—	—	30	µs	
Interrupt release delay time	t_{di1}	—	—	30	µs	
Interrupt detection delay time	t_{di2}	—	—	30	µs	
Interrupt threshold voltage transition stabilization time	t_{stb}	—	—	30	µs	

26. Package Dimension

Package Type	Package Code
LQFP 80	LQH 080



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	14.00 BSC.		
D1	12.00 BSC.		
e	0.50 BSC		
E	14.00 BSC.		
E1	12.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11501 **

PACKAGE OUTLINE, 80 LEAD LQFP
12.0X12.0X1.7 MM LQH080 Rev **