Infineon Technologies - MB95F778MPMC2-G-SNE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f778mpmc2-g-sne2

- Low-voltage detection (LVD) circuit (only available on MB95F714J/F716J/F718J/F774J/F776J/F778J)
  - Built-in low-voltage detection function
- Comparator × 1 channel
- Clock supervisor counter
  - Built-in clock supervisor counter
- Dual operation Flash memory
  - The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
  - Protects the content of the Flash memory.

1. Product Line-up

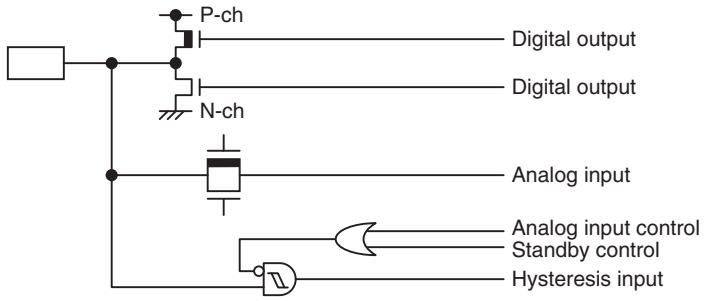
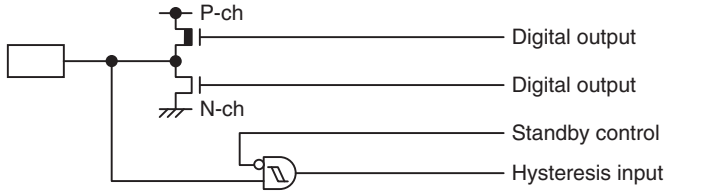
1.1 MB95710M Series

Part number / Parameter	MB95F714J	MB95F716J	MB95F718J	MB95F714M	MB95F716M	MB95F718M
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation and the subclock oscillation.					
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	512 bytes	1 Kbyte	2 Kbyte	512 bytes	1 Kbyte	2 Kbyte
Power-on reset	Yes					
Low-voltage detection reset	Yes			No		
Reset input	Selected through software			With dedicated reset input		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O port : 75 • CMOS I/O : 71 • N-ch open drain : 4			• I/O port : 74 • CMOS I/O : 71 • N-ch open drain : 3		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (min) • The sub-CR clock can be used as the source clock of the software watchdog timer.					
Wild register	It can be used to replace 3 bytes of data.					
8/12-bit A/D converter	8 channels					
	8-bit or 12-bit resolution can be selected.					
8/16-bit composite timer	2 channels					
	• The timer can be configured as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
External interrupt	8 channels					
	• Interrupt by edge detection (The rising edge, falling edge, and both edges can be selected.) • It can be used to wake up the device from different standby modes.					
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).					

Part number / Parameter	MB95F774J	MB95F776J	MB95F778J	MB95F774M	MB95F776M	MB95F778M
UART/SIO	3 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.					
I^2C bus interface	1 channel					
	• Master/slave transmission and reception • It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.					
8/16-bit PPG	2 channels					
	• Each channel can be used as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • The counter operating clock can be selected from eight clock sources.					
16-bit reload timer	1 channel					
	• Two clock modes and two counter operating modes are available to use. • It can output square wave. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Two counter operating modes: reload mode and one-shot mode					
Event counter	• The event counter function is implemented by configuring the 16-bit reload timer and 8/16-bit composite timer ch. 1. • When the event counter function is used, the 16-bit reload timer and 8/16-bit composite timer ch. 1 become unavailable.					
LCD controller (LCDC)	• COM output: 4 or 8 (max) (selectable) • SEG output: 28 or 32 (max) (selectable) - If the number of COM outputs is 4, the maximum number of SEG outputs is 32, and the maximum number of pixels that can be displayed 128 (4 × 32). - If the number of COM outputs is 8, the maximum number of SEG outputs is 28, and the maximum number of pixels that can be displayed 224 (8 × 28). • LCD drive power supply (bias) pins: 4 (max)					
	• Duty LCD mode • LCD standby mode • Blinking function • Internal divider resistor whose resistance value can be selected from 10 kΩ or 100 kΩ through software • Interrupt in sync with the LCD module frame frequency • Inverted display function					
Watch counter	• Count clock: four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • The counter value can be selected from 0 to 63. (The watch counter can count for one minute when the clock source is one second and the counter value is set to 60.)					
Watch prescaler	Eight different time intervals can be selected.					
Comparator	1 channel					

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
9	P00	W	General-purpose I/O port	Hysteresis/ analog	CMOS/ LCD	—	—
	INT00		External interrupt input pin				
	AN00		8/12-bit A/D converter analog input pin				
	UO2		UART/SIO ch. 2 data output pin				
10	P16	Y	General-purpose I/O port	Hysteresis	CMOS	—	—
	PPG10		8/16-bit PPG ch. 1 output pin				
11	P15	Y	General-purpose I/O port	Hysteresis	CMOS	—	—
	PPG11		8/16-bit PPG ch. 1 output pin				
12	P14	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	UCK0		UART/SIO ch. 0 clock I/O pin				
13	P13	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	ADTG		8/12-bit A/D converter trigger input pin				
14	P12	D	General-purpose I/O port	Hysteresis	CMOS	O	—
	DBG		DBG input pin				
15	P11	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	UO0		UART/SIO ch. 0 data output pin				
16	P10	G	General-purpose I/O port	CMOS	CMOS	—	O
	UI0		UART/SIO ch. 0 data input pin				
17	P53	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO0		16-bit reload timer ch. 0 output pin				
18	P52	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	TI0		16-bit reload timer ch. 0 input pin				
	TO00		8/16-bit composite timer ch. 0 output pin				
19	P51	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	EC0		8/16-bit composite timer ch. 0 clock input pin				
20	P50	H	General-purpose I/O port	Hysteresis	CMOS	—	O
	TO01		8/16-bit composite timer ch. 0 output pin				
21	P23	I	General-purpose I/O port	CMOS	CMOS	O	—
	SDA		I^2C bus interface ch. 0 data I/O pin				
22	P22	I	General-purpose I/O port	CMOS	CMOS	O	—
	SCL		I^2C bus interface ch. 0 clock I/O pin				
23	P21	T	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	PPG01		8/16-bit PPG ch. 0 output pin				
	CMP0_P		Comparator ch. 0 non-inverting analog input (positive input) pin				

Pin no.	Pin name	I/O circuit type*1	Function	I/O type			
				Input	Output	OD*2	PU*3
21	P90	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V4		LCD drive power supply pin				
22	P91	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V3		LCD drive power supply pin				
23	P92	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V2		LCD drive power supply pin				
24	P93	R	General-purpose I/O port	Hysteresis/ LCD power supply	CMOS/ LCD power supply	—	—
	V1		LCD drive power supply pin				
25	PA0	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM0		LCDC COM0 output pin				
26	PA1	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM1		LCDC COM1 output pin				
27	PA2	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM2		LCDC COM2 output pin				
28	PA3	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM3		LCDC COM3 output pin				
29	PA4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM4		LCDC COM4 output pin				
30	PA5	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM5		LCDC COM5 output pin				
31	PA6	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM6		LCDC COM6 output pin				
32	PA7	M	General-purpose I/O port	Hysteresis	CMOS/ LCD	—	—
	COM7		LCDC COM7 output pin				
33	V_{SS}	—	Power supply pin (GND)	—	—	—	—
34	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
35	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
36	C	—	Decoupling capacitor connection pin	—	—	—	—
37	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				

Type	Circuit	Remarks
W		• CMOS output • Hysteresis input • Analog input
Y		• CMOS output • Hysteresis input

- **Storage of Semiconductor Devices**

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

  Condition: 125°C/24 h

- **Static Electricity**

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%.
  Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

8.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

Address	Register abbreviation	Register name	R/W	Initial value
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	—	(Disabled)	—	—
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000
0x0F9C	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	0b11111111
0x0F9D	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	0b11111111
0x0F9E	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	0b11111111
0x0F9F	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	0b11111111
0x0FA0	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	0b11111111
0x0FA1	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	0b11111111
0x0FA2	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	0b11111111
0x0FA3	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	0b11111111
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000
0x0FA6	TMRH0	16-bit reload timer timer register (upper) ch. 0	R/W	0b00000000
	TMRLRH0	16-bit reload timer reload register (upper) ch. 0		

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P10/UI0/TO0 and P14/UCK0/EC0/TI0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL1 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

19.3 Port 2

Port 2 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.3.1 Port 2 configuration

Port 2 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 2 data register (PDR2)
- Port 2 direction register (DDR2)
- Port 2 pull-up register (PUL2)

19.3.2 Block diagrams of port 2

- P20/PPG00/CMP0_N pin
  This pin has the following peripheral functions:
  - 8/16-bit PPG ch. 0 output pin (PPG00)
  - Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)

- P21/PPG01/CMP0_P pin
  This pin has the following peripheral functions:
  - 8/16-bit PPG ch. 0 output pin (PPG01)
  - Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0_P)

19.8.4 Port C operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRC register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRC register to external pins.
  - If data is written to the PDRC register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRC register returns the PDRC register value.
  - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[05:02]) to “0” to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to “1”.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRC register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRC register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRC register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRC register, the PDRC register value is returned.
  - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[05:02]) to “0” to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation as an LCDC segment output pin
  - Set the bit in the DDRC register corresponding to an LCDC segment output pin to “0”.
  - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[05:02]) to “1” to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to “1”.

- Operation at reset
  If the CPU is reset, all bits in the DDRC register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRC register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.10 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95710M/770M Series Hardware Manual”.

19.10.1 Port F configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)

19.10.2 Block diagrams of port F

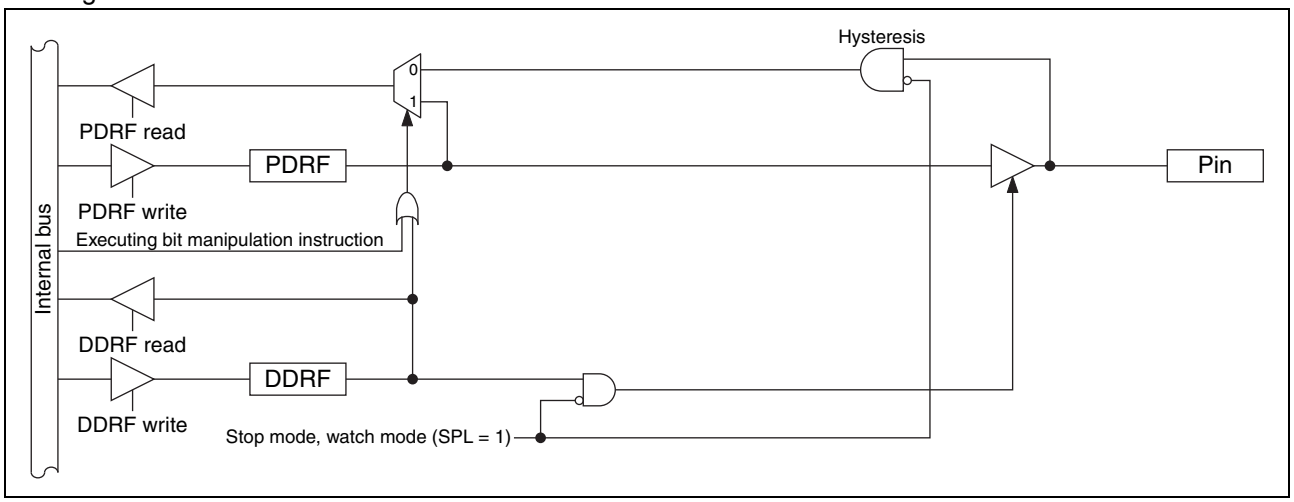
- PF0/X0 pin

  This pin has the following peripheral function:
  - Main clock input oscillation pin (X0)

- PF1/X1 pin

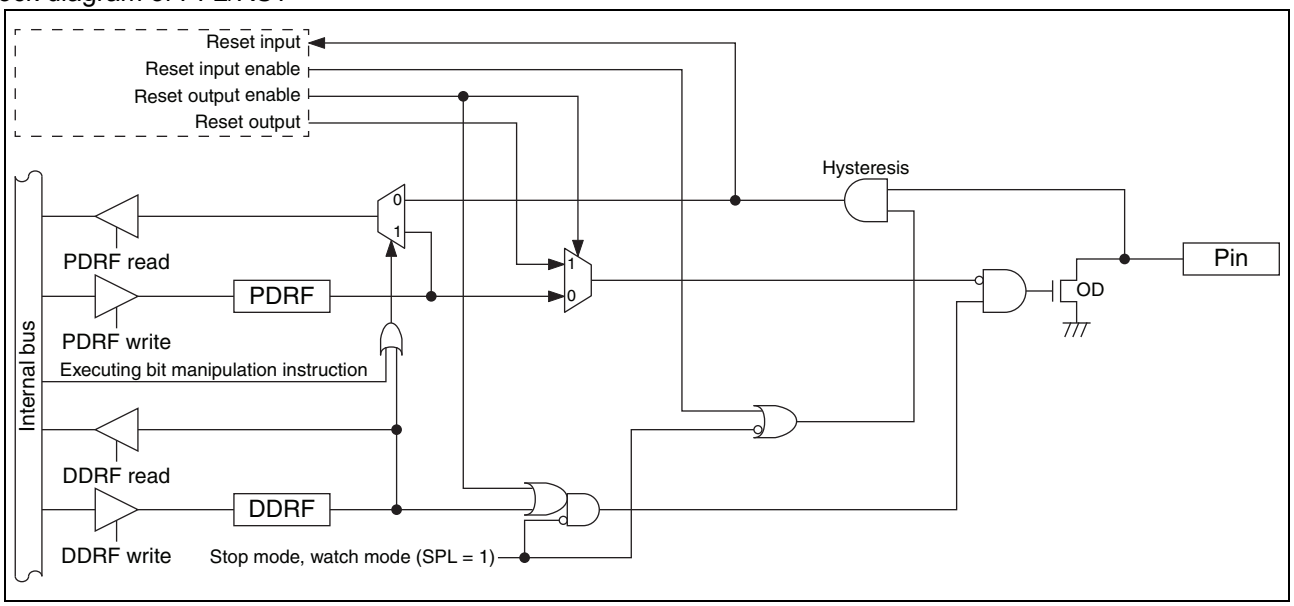
  This pin has the following peripheral function:
  - Main clock I/O oscillation pin (X1)

- Block diagram of PF0/X0 and PF1/X1



- PF2/$\overline{\text{RST}}$ pin
  This pin has the following peripheral function:
  - Reset pin ($\overline{\text{RST}}$)

- Block diagram of PF2/$\overline{\text{RST}}$



19.10.3 Port F registers

- Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRF	0	Pin state is “L” level.	PDRF value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRF value is “1”.	As output port, outputs “H” level.*
DDRF	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port F

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PF2***	**PF1**	**PF0**
PDRF	-	-	-	-	-	bit2	bit1	bit0
DDRF								

*: PF2/$\overline{\text{RST}}$ is the dedicated reset pin on MB95F774M/F776M/F778M.

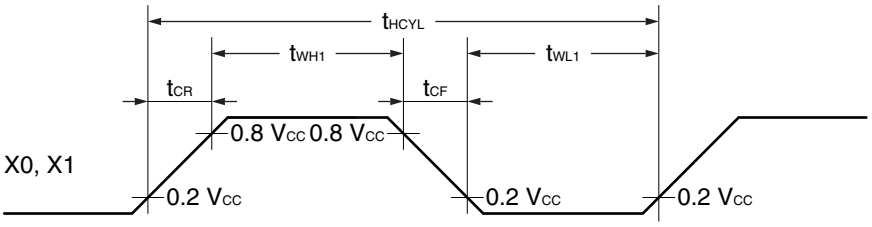
22.4 AC Characteristics

22.4.1 Clock Timing

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

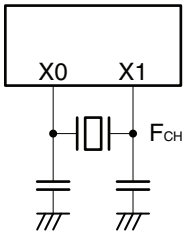
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency		X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	—	1	—	32.5	MHz	When the main external clock is used
	F_{CH}	X0, X1	—	4	—	8.13	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 2
				4	—	6.5	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 2.5
				4	—	5.41	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 3
				4	—	4.06	MHz	Operating conditions • The main clock is used. • PLL multiplication rate: 4
	F_{CRH}	—	—	3.92	4	4.08	MHz	Operating conditions • The main CR clock is used. • 0 °C ≤ T_A ≤ +70 °C
				3.8	4	4.2	MHz	Operating conditions • The main CR clock is used. • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
	F_{MCRPLL}	—	—	7.84	8	8.16	MHz	Operating conditions • PLL multiplication rate: 2 • 0 °C ≤ T_A ≤ +70 °C
				7.6	8	8.4	MHz	Operating conditions • PLL multiplication rate: 2 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				9.8	10	10.2	MHz	Operating conditions • PLL multiplication rate: 2.5 • 0 °C ≤ T_A ≤ +70 °C
				9.5	10	10.5	MHz	Operating conditions • PLL multiplication rate: 2.5 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				11.76	12	12.24	MHz	Operating conditions • PLL multiplication rate: 3 • 0 °C ≤ T_A ≤ +70 °C
				11.4	12	12.6	MHz	Operating conditions • PLL multiplication rate: 3 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C

- Input waveform generated when an external clock (main clock) is used

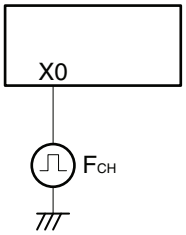


- Figure of main clock input port external connection

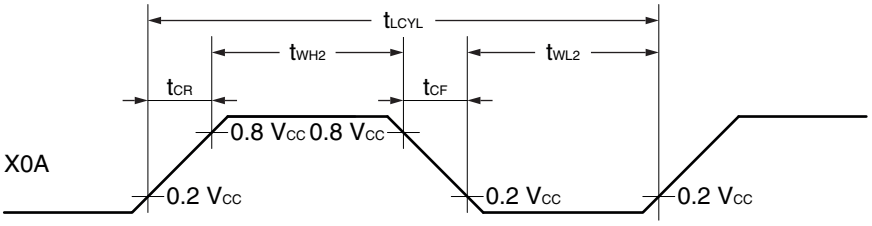
When a crystal oscillator or a ceramic oscillator is used



When an external clock is used

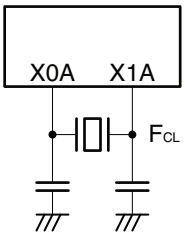


- Input waveform generated when an external clock (subclock) is used

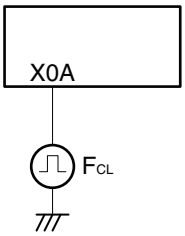


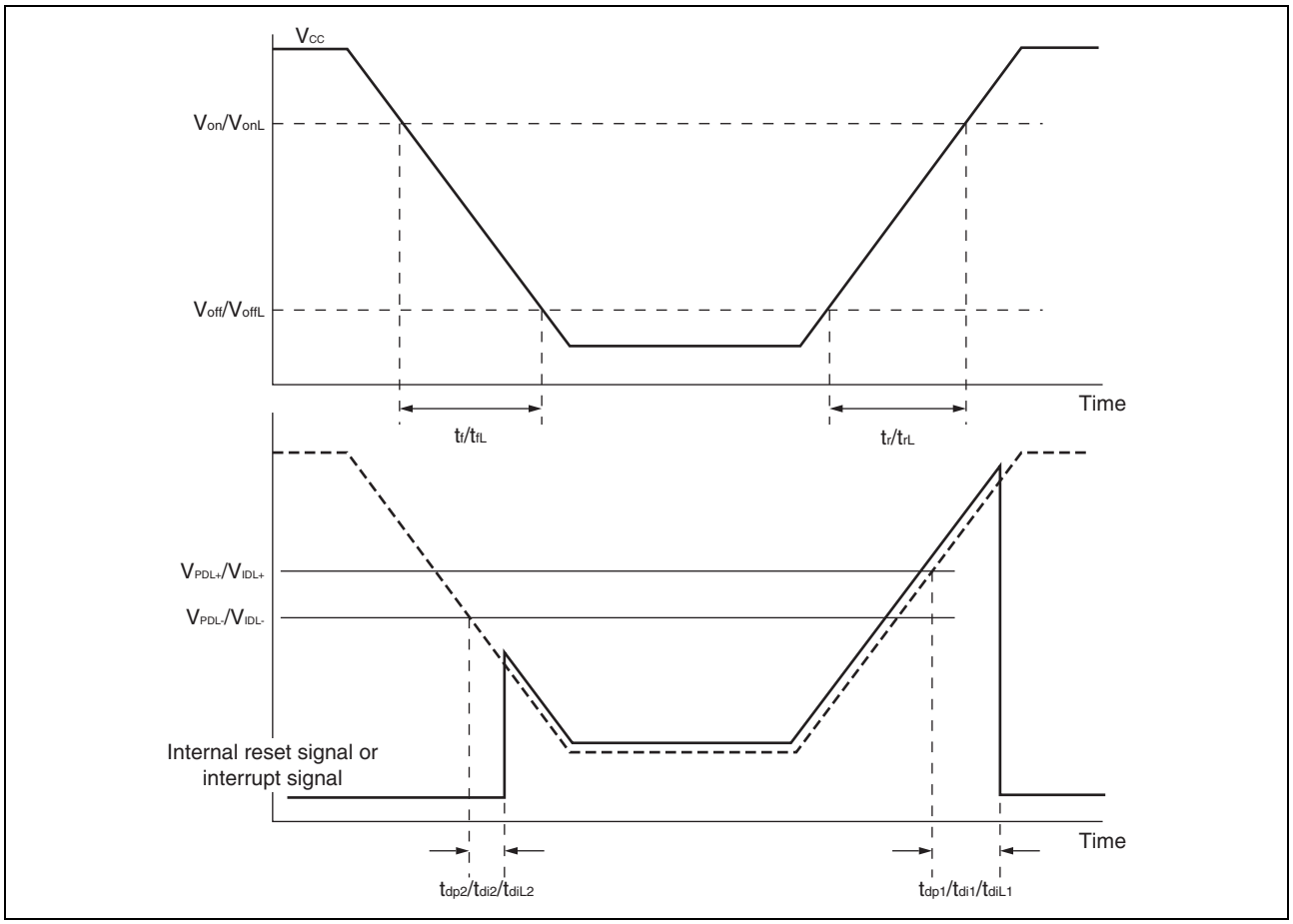
- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used

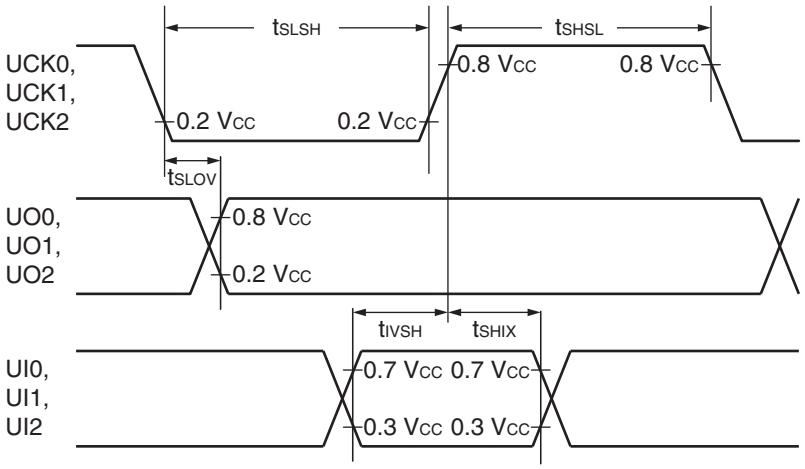


When an external clock is used




Vcc
Von/VonL
Voff/VoffL
Time
tf/tfL
tr/trL
VPDL+/VIDL+
VPDL-/VIDL-
Internal reset signal or
interrupt signal
Time
tdp2/tdi2/tdiL2
tdp1/tdi1/tdiL1

- External shift clock mode

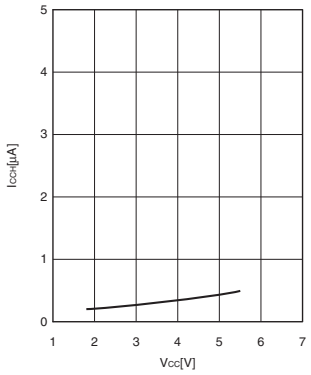


22.4.9 Comparator Timing

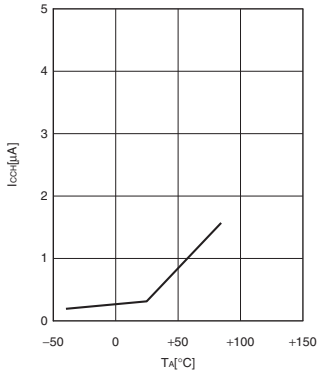
(AV_{CC} = 1.8 V to 5.5 V, AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Voltage range	CMP0_P, CMP0_N	0	—	AV_{CC}	V	
Offset voltage	CMP0_P, CMP0_N	–20	—	+20	mV	
Delay time	CMP0_O	—	600	1200	ns	Overdrive 5 mV
		—	120	420	ns	Overdrive 50 mV
Power down delay	CMP0_O	—	—	1200	ns	Power down recovery PD: 1 → 0
		0	—	150	ns	Power down PD: 0 → 1
Power up stabilization time	CMP0_O	—	—	1200	ns	Output stabilization time at power up
Bandgap reference voltage	—	1.15	1.21	1.27	V	

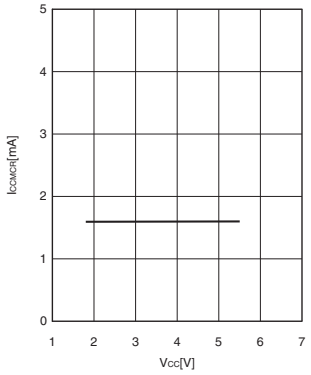
I_{CCH} – V_{CC}
T_A = +25 °C, F_{MPL} = (stop)
Substop mode with the external clock stopping



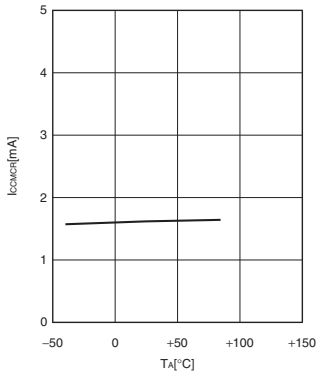
I_{CCH} – T_A
V_{CC} = 3.3 V, F_{MPL} = (stop)
Substop mode with the external clock stopping



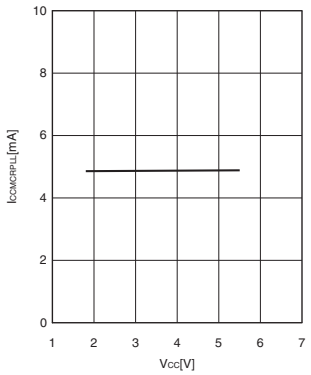
I_{CCMCR} – V_{CC}
T_A = +25 °C, F_{MP} = 4 MHz (no division)
Main CR clock mode



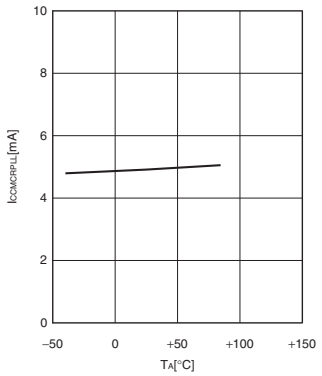
I_{CCMCR} – T_A
V_{CC} = 3.3 V, F_{MP} = 4 MHz (no division)
Main CR clock mode



$I_{CCMCRPLL}$ – V_{CC}
T_A = +25 °C, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode

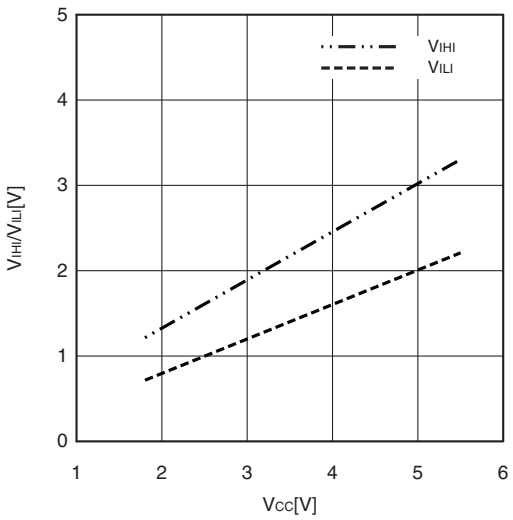


$I_{CCMCRPLL}$ – T_A
V_{CC} = 3.3 V, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode

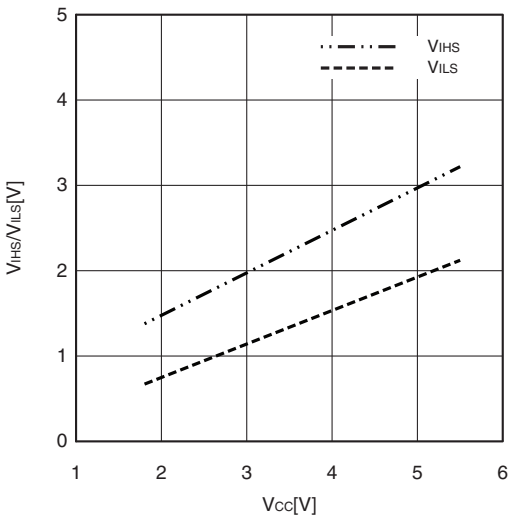


- Input voltage characteristics

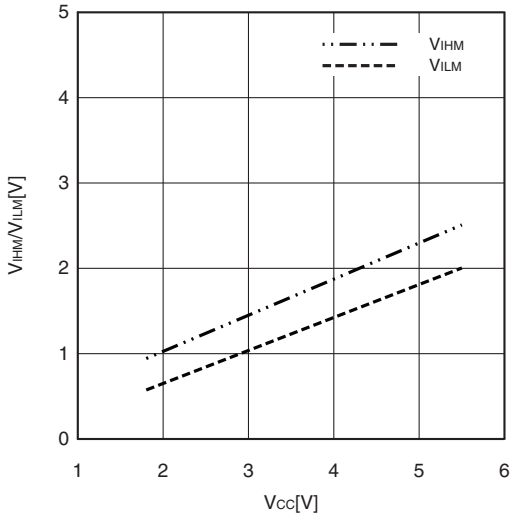
V_{IHI} – V_{CC} and V_{ILI} – V_{CC}
T_A = +25 °C



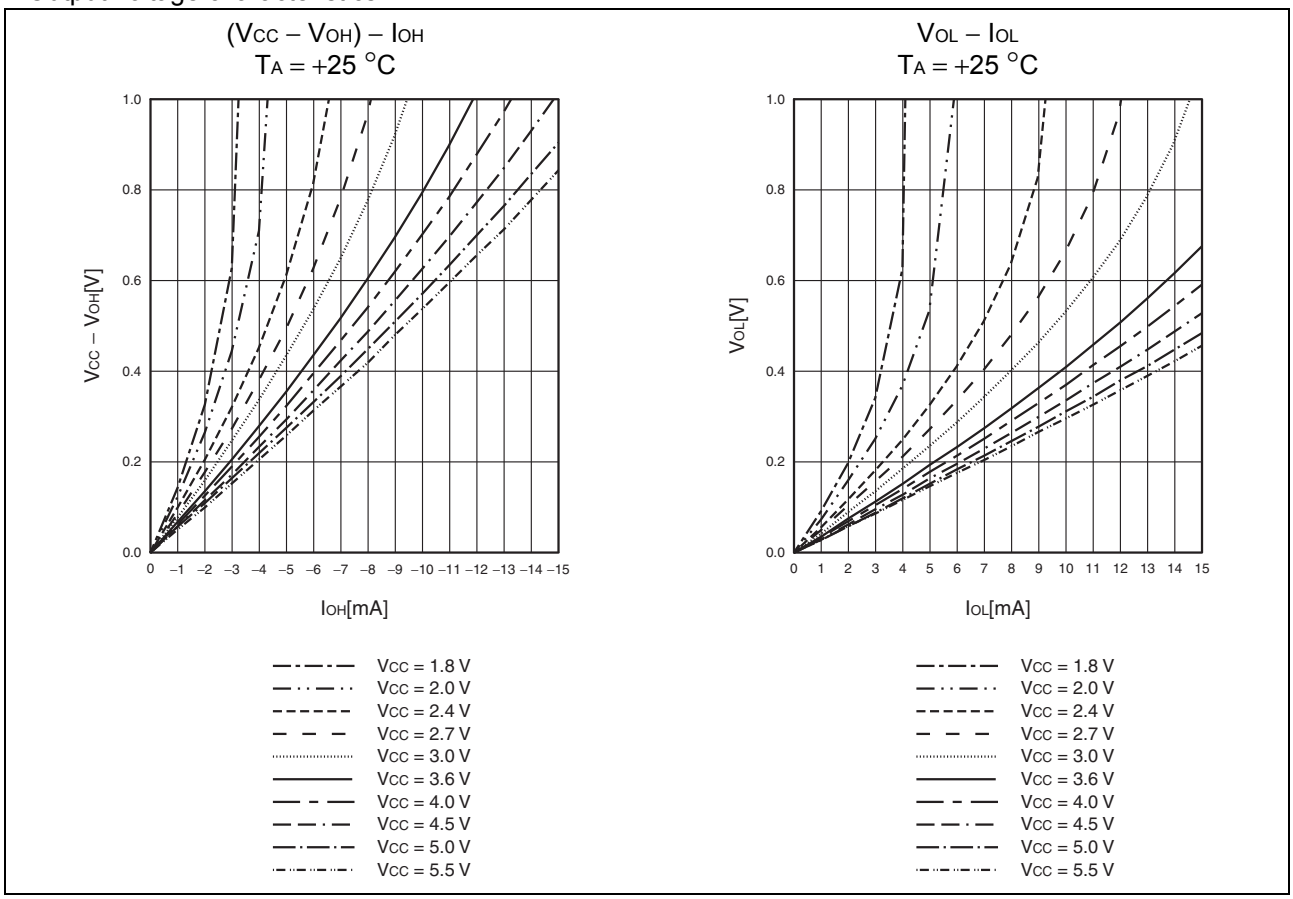
V_{IHS} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25 °C



V_{IHM} – V_{CC} and V_{ILM} – V_{CC}
T_A = +25 °C

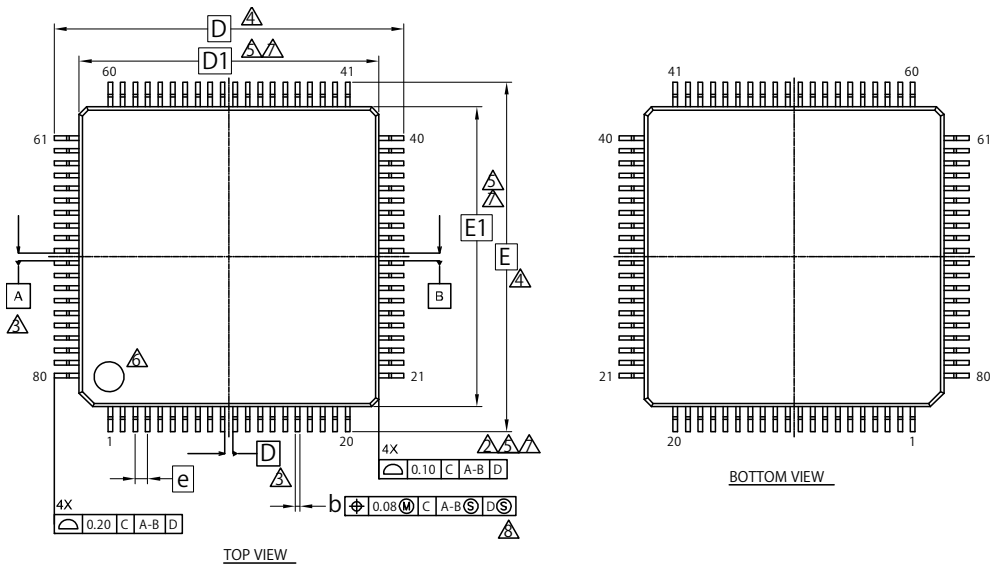


- Output voltage characteristics



26. Package Dimension

Package Type	Package Code
LQFP 80	LQH 080



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	14.00 BSC.		
D1	12.00 BSC.		
e	0.50 BSC		
E	14.00 BSC.		
E1	12.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11501 **

PACKAGE OUTLINE, 80 LEAD LQFP
12.0X12.0X1.7 MM LQH080 Rev **