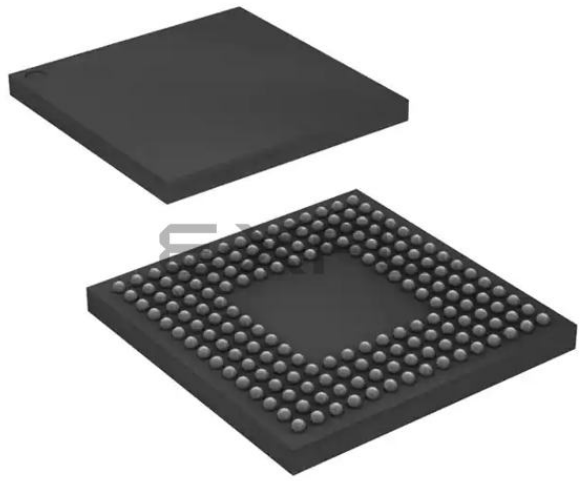

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	33MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, WDT
Number of I/O	58
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91m55800a-33ci-t

3. Pin Description

Table 3-1. Pin Description

Module	Name	Function	Type	Active Level	Comments
EBI	A0 - A23	Address bus	Output	–	
	D0 - D15	Data bus	I/O	–	
	NCS0 - NCS7	Chip select	Output	Low	
	NWR0	Lower byte 0 write signal	Output	Low	Used in Byte-write option
	NWR1	Lower byte 1 write signal	Output	Low	Used in Byte-write option
	NRD	Read signal	Output	Low	Used in Byte-write option
	NWE	Write enable	Output	Low	Used in Byte-select option
	NOE	Output enable	Output	Low	Used in Byte-select option
	NUB	Upper byte-select	Output	Low	Used in Byte-select option
	NLB	Lower byte-select	Output	Low	Used in Byte-select option
	NWAIT	Wait input	Input	Low	
	BMS	Boot mode select	Input	–	Sampled during reset
AIC	IRQ0 - IRQ5	External interrupt request	Input	–	PIO-controlled after reset
	FIQ	Fast external interrupt request	Input	–	PIO-controlled after reset
Timer	TCLK0 - TCLK5	Timer external clock	Input	–	PIO-controlled after reset
	TIOA0 - TIOA5	Multipurpose timer I/O pin A	I/O	–	PIO-controlled after reset
	TIOB0 - TIOB5	Multipurpose timer I/O pin B	I/O	–	PIO-controlled after reset
USART	SCK0 - SCK2	External serial clock	I/O	–	PIO-controlled after reset
	TXD0 - TXD2	Transmit data output	Output	–	PIO-controlled after reset
	RXD0 - RXD2	Receive data input	Input	–	PIO-controlled after reset
SPI	SPCK	SPI clock	I/O	–	PIO-controlled after reset
	MISO	Master in slave out	I/O	–	PIO-controlled after reset
	MOSI	Master out slave in	I/O	–	PIO-controlled after reset
	NSS	Slave select	Input	Low	PIO-controlled after reset
	NPCS0 - NPCS3	Peripheral chip select	Output	Low	PIO-controlled after reset
PIO	PA0 - PA29	Parallel I/O port A	I/O	–	Input after reset
	PB0 - PB27	Parallel I/O port B	I/O	–	Input after reset
WD	NWDOVF	Watchdog timer overflow	Output	Low	Open drain
ADC	AD0-AD7	Analog input channels 0 - 7	Analog in	–	
	AD0TRIG	ADC0 external trigger	Input	–	PIO-controlled after reset
	AD1TRIG	ADC1 external trigger	Input	–	PIO-controlled after reset
	ADVREF	Analog reference	Analog ref	–	

PIO Controllers called PIOA and PIOB. The PIO controller enables the generation of an interrupt on input change and insertion of a simple input glitch filter on any of the PIO pins.

8.4.5 WD: Watchdog

The Watchdog is built around a 16-bit counter, and is used to prevent system lock-up if the software becomes trapped in a deadlock. It can generate an internal reset or interrupt, or assert an active level on the dedicated pin NWDOVF. All programming registers are password-protected to prevent unintentional programming.

8.4.6 SF: Special Function

The AT91M55800A provides registers which implement the following special functions.

- Chip identification
- RESET status

8.5 User Peripherals

8.5.1 USART: Universal Synchronous Asynchronous Receiver Transmitter

The AT91M55800A provides three identical, full-duplex, universal synchronous/asynchronous receiver/transmitters.

Each USART has its own baud rate generator, and two dedicated Peripheral Data Controller channels. The data format includes a start bit, up to 8 data bits, an optional programmable parity bit and up to 2 stop bits.

The USART also features a Receiver Timeout register, facilitating variable-length frame support when it is working with the PDC, and a Time-guard register, used when interfacing with slow remote equipment.

8.5.2 TC: Timer Counter

The AT91M55800A features two Timer Counter blocks that include three identical 16-bit timer counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse-width modulation.

The Timer Counters can be used in Capture or Waveform mode, and all three counter channels can be started simultaneously and chained together.

8.5.3 SPI: Serial Peripheral Interface

The SPI provides communication with external devices in master or slave mode. It has four external chip selects that can be connected to up to 15 devices. The data length is programmable, from 8- to 16-bit.

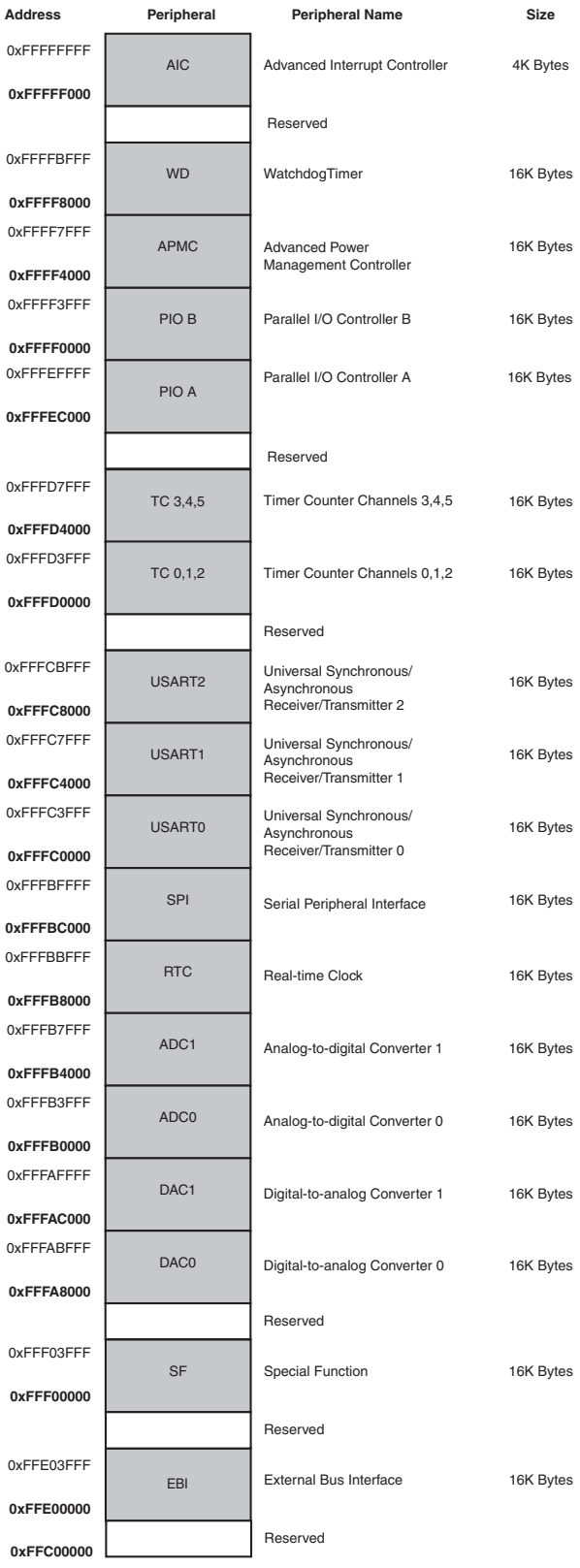
8.5.4 ADC: Analog-to-digital Converter

The two identical 4-channel 10-bit analog-to-digital converters (ADC) are based on a Successive Approximation Register (SAR) approach.

Each ADC has 4 analog input pins, AD0 to AD3 and AD4 to AD7, digital trigger input pins AD0TRIG and AD1TRIG, and provides an interrupt signal to the AIC. Both ADCs share the analog power supply pins VDDA and GNDA, and the input reference voltage pin ADVREF.

10. Peripheral Memory Map

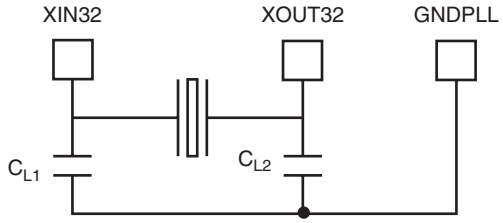
Figure 1. AT91M55800A Peripheral Memory Map



12.2 Slow Clock Generator

The AT91M55800A has a very low power 32 kHz oscillator powered by the backup battery voltage supplied on the VDDBU pins. The XIN32 and XOUT32 pins must be connected to a 32768 Hz crystal. The oscillator has been especially designed to connect to a 6 pF typical load capacitance crystal and does not require any external capacitor, as it integrates the XIN32 and XOUT32 capacitors to ground. For a higher typical load capacitance, two external capacitances must be wired as shown in Figure 12-3:

Figure 12-3. Higher Typical Load Capacitance



12.2.1 Backup Reset Controller

The backup reset controller initializes the logic supplied by the backup battery power. A simple RC circuit connected to the NRSTBU pin provides a power-on reset signal to the RTC and the shutdown logic. When the reset signal increases and as the startup time of the 32 kHz oscillator is around 300 ms, the AT91M55800A maintains the internal backup reset signal for 32768 oscillator clock cycles in order to guarantee the backup power supplied logic does not operate before the oscillator output is stabilized.

Alternatively, a reset supervisor can be connected to the NRSTBU pin in place of the RC.

12.2.2 Slow Clock

The Slow Clock is the only clock considered permanent in an AT91M55800A-based system and is essential in the operations of the APMC (Advanced Power Management Controller). In any use-case, a 32768 Hz crystal must be connected to the XIN32 and XOUT32 pins in order to ensure that the Slow Clock is present.

13.3.3 RTC Time Register

Register Name: RTC_TIMR

Access Type: Read/Write

Reset State: 0x0

Offset: 0x08

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	AMPM	HOUR					
15	14	13	12	11	10	9	8
–	MIN						
7	6	5	4	3	2	1	0
–	SEC						

- **SEC: Current Second (Code Label `RTC_SEC`)**

The range that can be set is 0 - 59 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

- **MIN: Current Minute (Code Label `RTC_MIN`)**

The range that can be set is 0-59 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

- **HOUR: Current Hour (Code Label `RTC_HOUR`)**

The range that can be set is 1 - 12 (BCD) in 12-hour mode or 0 - 23 (BCD) in 24-hour mode.

- **AMPM: Ante Meridiem Post Meridiem Indicator (Code Label `RTC_AMPM`)**

This bit is the AM/PM indicator in 12-hour mode. It must be written at 0 if HRMOD in RTC_HMR defines 24-Hour mode.

0 = AM.

1 = PM.

13.3.8 RTC Status Clear Register

Register Name: RTC_SCR

Access Type: Write-only

Offset: 0x1C

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	CALEV	TIMEV	SEC	ALARM	ACKUPD

- **ACKUPD: Acknowledge for Update Interrupt Clear (Code Label `RTC_ACKUPD`)**

0 = No effect.

1 = Clears Acknowledge for Update status bit.

- **ALARM: Alarm Flag Interrupt Clear (Code Label `RTC_ALARM`)**

0 = No effect.

1 = Clears Alarm Flag bit.

- **SEC: Second Event Interrupt Clear (Code Label `RTC_SEC`)**

0 = No effect.

1 = Clears Second Event bit.

- **TIMEV: Time Event Interrupt Clear (Code Label `RTC_TIMEV`)**

0 = No effect.

1 = Clears Time Event bit.

- **CALEV: Calendar Event Interrupt Clear (Code Label `RTC_CALEV`)**

0 = No effect.

1 = Clears Calendar Event bit.

Table 15-1. AIC Interrupt Sources

Interrupt Source	Interrupt Name	Interrupt Description
0	FIQ	Fast interrupt
1	SWIRQ	Software interrupt
2	US0IRQ	USART Channel 0 interrupt
3	US1IRQ	USART Channel 1 interrupt
4	US2IRQ	USART Channel 2 interrupt
5	SPIRQ	SPI interrupt
6	TC0IRQ	Timer Channel 0 interrupt
7	TC1IRQ	Timer Channel 1 interrupt
8	TC2IRQ	Timer Channel 2 interrupt
9	TC3IRQ	Timer Channel 3 interrupt
10	TC4IRQ	Timer Channel 4 interrupt
11	TC5IRQ	Timer Channel 5 interrupt
12	WDIRQ	Watchdog interrupt
13	PIOAIRQ	Parallel I/O Controller A interrupt
14	PIOBIRQ	Parallel I/O Controller B interrupt
15	AD0IRQ	Analog-to-digital Converter Channel 0 interrupt
16	AD1IRQ	Analog-to-digital Converter Channel 1 interrupt
17	DA0IRQ	Digital-to-analog Converter Channel 0 interrupt
18	DA1IRQ	Digital-to-analog Converter Channel 1 interrupt
19	RTCIRQ	Real-time Clock interrupt
20	APMCIRQ	Advanced Power Management Controller interrupt
21	–	Reserved
22	–	Reserved
23	SLCKIRQ	Slow Clock Interrupt
24	IRQ5	External interrupt 5
25	IRQ4	External interrupt 4
26	IRQ3	External interrupt 3
27	IRQ2	External interrupt 2
28	IRQ1	External interrupt 1
29	IRQ0	External interrupt 0
30	COMMRX	RX Debug Communication Channel interrupt
31	COMMTX	TX Debug Communication Channel interrupt

15.10.8 AIC Core Interrupt Status Register

Register Name: AIC_CISR

Access Type: Read-only

Reset Value: 0

Offset: 0x114

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	NIRQ	NFIQ

- **NFIQ: NFIQ Status (Code Label `AIC_NFIQ`)**

0 = NFIQ line inactive.

1 = NFIQ line active.

- **NIRQ: NIRQ Status (Code Label `AIC_NIRQ`)**

0 = NIRQ line inactive.

1 = NIRQ line active.

15.10.9 AIC Interrupt Enable Command Register

Register Name: AIC_IECR

Access Type: Write-only

Offset: 0x120

31	30	29	28	27	26	25	24
COMMRX	COMMTX	IRQ0	IRQ1	IRQ2	IRQ3	IRQ4	IRQ5
23	22	21	20	19	18	17	16
SLCKIRQ	–	–	APMCIRQ	RTCIRQ	DAC1IRQ	DAC0IRQ	ADC1IRQ
15	14	13	12	11	10	9	8
ADC0IRQ	PIOBIRQ	PIOAIRQ	WDIRQ	TC5IRQ	TC4IRQ	TC3IRQ	TC2IRQ
7	6	5	4	3	2	1	0
TC1IRQ	TC0IRQ	SPIRQ	US2IRQ	US1IRQ	US0IRQ	SWIRQ	FIQ

- **Interrupt Enable**

0 = No effect.

1 = Enables corresponding interrupt.

- **NBSTOP: Number of Stop Bits**

The interpretation of the number of stop bits depends on SYNC.

NBSTOP		Asynchronous (SYNC = 0)	Synchronous (SYNC = 1)	Code Label: US_NBSTOP
0	0	1 stop bit	1 stop bit	US_NBSTOP_1
0	1	1.5 stop bits	Reserved	US_NBSTOP_1_5
1	0	2 stop bits	2 stop bits	US_NBSTOP_2
1	1	Reserved	Reserved	–

- **CHMODE: Channel Mode**

CHMODE		Mode Description	Code Label: US_CHMODE
0	0	Normal Mode The USART Channel operates as an Rx/Tx USART.	US_CHMODE_NORMAL
0	1	Automatic Echo Receiver Data Input is connected to TXD pin.	US_CHMODE_AUTOMATIC_ECHO
1	0	Local Loopback Transmitter Output Signal is connected to Receiver Input Signal.	US_CHMODE_LOCAL_LOOPBACK
1	1	Remote Loopback RXD pin is internally connected to TXD pin.	US_CHMODE_REMODE_LOOPBACK

- **MODE9: 9-Bit Character Length (Code Label US_MODE9)**

0 = CHRL defines character length.

1 = 9-Bit character length.

- **CKLO: Clock Output Select (Code Label US_CLKO)**

0 = The USART does not drive the SCK pin.

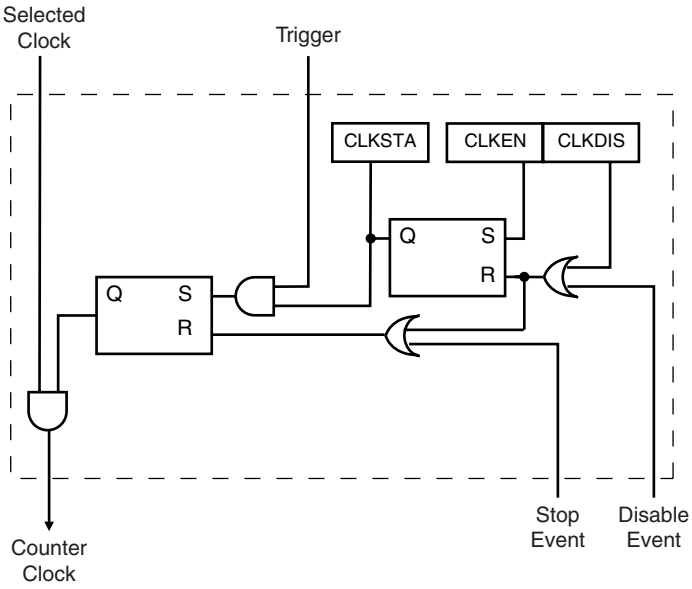
1 = The USART drives the SCK pin if USCLKS[1] is 0.

19.2.3 Clock Control

The clock of each counter can be controlled in two different ways: it can be enabled/disabled and started/stopped.

- The clock can be **enabled** or **disabled** by the user with the CLKEN and the CLKDIS commands in the Control Register. In Capture Mode it can be disabled by an RB load event if LDBDIS is set to 1 in TC_CMR. In Waveform Mode, it can be disabled by an RC Compare event if CPCDIS is set to 1 in TC_CMR. When disabled, the start or the stop actions have no effect: only a CLKEN command in the Control Register can re-enable the clock. When the clock is enabled, the CLKSTA bit is set in the Status Register.
- The clock can also be **started** or **stopped**: a trigger (software, synchro, external or compare) always starts the clock. The clock can be stopped by an RB load event in Capture Mode (LDBSTOP = 1 in TC_CMR) or a RC compare event in Waveform Mode (CPCSTOP = 1 in TC_CMR). The start and the stop commands have effect only if the clock is enabled.

Figure 19-3. Clock Control



19.2.4 Timer Counter Operating Modes

Each Timer Counter channel can independently operate in two different modes:

- Capture Mode allows measurement on signals
- Waveform Mode allows wave generation

The Timer Counter Mode is programmed with the WAVE bit in the TC Mode Register. In Capture Mode, TIOA and TIOB are configured as inputs. In Waveform Mode, TIOA is always configured to be an output and TIOB is an output if it is not selected to be the external trigger.

19.2.5 Trigger

A trigger resets the counter and starts the counter clock. Three types of triggers are common to both modes, and a fourth external trigger is available to each mode.

The following triggers are common to both modes:

- Software Trigger: Each channel has a software trigger, available by setting SWTRG in TC_CCR.
- SYNC: Each channel has a synchronization signal SYNC. When asserted, this signal has the same effect as a software trigger. The SYNC signals of all channels are asserted simultaneously by writing TC_BCR (Block Control) with SYNC set.
- Compare RC Trigger: RC is implemented in each channel and can provide a trigger when the counter value matches the RC value if CPCTRG is set in TC_CMR.

The Timer Counter channel can also be configured to have an external trigger. In Capture Mode, the external trigger signal can be selected between TIOA and TIOB. In Waveform Mode, an external event can be programmed on one of the following signals: TIOB, XC0, XC1 or XC2. This external event can then be programmed to perform a trigger by setting ENETRG in TC_CMR.

If an external trigger is used, the duration of the pulses must be longer than the system clock (MCK) period in order to be detected.

- **LDBDIS: Counter Clock Disable with RB Loading (Code Label `TC_LDBDIS`)**

0 = Counter clock is not disabled when RB loading occurs.

1 = Counter clock is disabled when RB loading occurs.

- **ETRGEDG: External Trigger Edge Selection**

ETRGEDG		Edge	Code Label: `TC_ETRGEDG`
0	0	None	`TC_ETRGEDG_EDGE_NONE`
0	1	Rising edge	`TC_ETRGEDG_RISING_EDGE`
1	0	Falling edge	`TC_ETRGEDG_FALLING_EDGE`
1	1	Each edge	`TC_ETRGEDG_BOTH_EDGE`

- **ABETRG: TIOA or TIOB External Trigger Selection**

ABETRG	Selected ABETRG	Code Label: `TC_ABETRG`
0	TIOB is used as an external trigger.	TC_ABETRG_TIOB
1	TIOA is used as an external trigger.	TC_ABETRG_TIOA

- **CPCTRG: RC Compare Trigger Enable (Code Label `TC_CPCTRG`)**

0 = RC Compare has no effect on the counter and its clock.

1 = RC Compare resets the counter and starts the counter clock.

- **WAVE = 0 (Code Label `TC_WAVE`)**

0 = Capture Mode is enabled.

1 = Capture Mode is disabled (Waveform Mode is enabled).

- **LDRA: RA Loading Selection**

LDRA		Edge	Code Label: `TC_LDRA`
0	0	None	`TC_LDRA_EDGE_NONE`
0	1	Rising edge of TIOA	`TC_LDRA_RISING_EDGE`
1	0	Falling edge of TIOA	`TC_LDRA_FALLING_EDGE`
1	1	Each edge of TIOA	`TC_LDRA_BOTH_EDGE`

- **LDRB: RB Loading Selection**

LDRB		Edge	Code Label: `TC_LDRB`
0	0	None	`TC_LDRB_EDGE_NONE`
0	1	Rising edge of TIOA	`TC_LDRB_RISING_EDGE`
1	0	Falling edge of TIOA	`TC_LDRB_FALLING_EDGE`
1	1	Each edge of TIOA	`TC_LDRB_BOTH_EDGE`

19.5.12 TC Interrupt Disable Register

Register Name: TC_IDR
Access Type: Write-only
Offset: 0x28

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

- **COVFS: Counter Overflow (Code Label `TC_COVFS`)**

0 = No effect.

1 = Disables the Counter Overflow Interrupt.

- **LOVRS: Load Overrun (Code Label `TC_LOVRS`)**

0 = No effect.

1 = Disables the Load Overrun Interrupt (if WAVE = 0).

- **CPAS: RA Compare (Code Label `TC_CPAS`)**

0 = No effect.

1 = Disables the RA Compare Interrupt (if WAVE = 1).

- **CPBS: RB Compare (Code Label `TC_CPBS`)**

0 = No effect.

1 = Disables the RB Compare Interrupt (if WAVE = 1).

- **CPCS: RC Compare (Code Label `TC_CPCS`)**

0 = No effect.

1 = Disables the RC Compare Interrupt.

- **LDRAS: RA Loading (Code Label `TC_LDRAS`)**

0 = No effect.

1 = Disables the RA Load Interrupt (if WAVE = 0).

- **LDRBS: RB Loading (Code Label `TC_LDRBS`)**

0 = No effect.

1 = Disables the RB Load Interrupt (if WAVE = 0).

- **ETRGS: External Trigger (Code Label `TC_ETRGS`)**

0 = No effect.

1 = Disables the External Trigger Interrupt.

20. SPI: Serial Peripheral Interface

The AT91M55800A includes an SPI which provides communication with external devices in master or slave mode.

The SPI has four external chip selects which can be connected to up to 15 devices. The data length is programmable, from 8- to 16-bit.

As for the USART, a 2-channel PDC can be used to move data between memory and the SPI without CPU intervention.

20.1 Pin Description

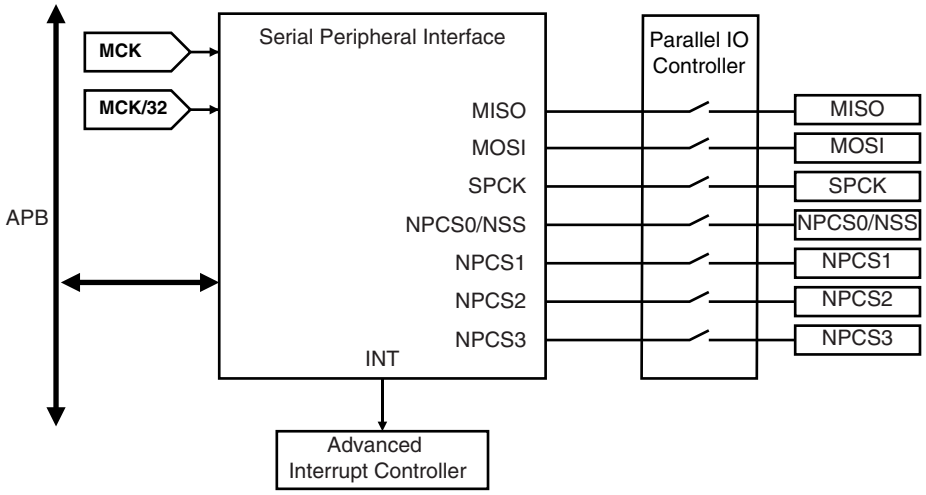
Seven pins are associated with the SPI Interface. When not needed for the SPI function, each of these pins can be configured as a PIO.

Support for an external master is provided by the PIO Controller Multi-driver option. To configure an SPI pin as open-drain to support external drivers, set the corresponding bits in the PIO_MDSR register.

An input filter can be enabled on the SPI input pins by setting the corresponding bits in the PIO_IFSR.

The NPCS0/NSS pin can function as a peripheral chip select output or slave select input. Refer to Table 20-1 for a description of the SPI pins.

Figure 20-1. SPI Block Diagram



20.7.3 SPI Receive Data Register

Register Name: SP_RDR
Access Type: Read-only
Reset State: 0
Offset: 0x08

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	PCS			

15	14	13	12	11	10	9	8
RD							

7	6	5	4	3	2	1	0
RD							

- **RD: Receive Data (Code Label `SP_RD`)**

Data received by the SPI Interface is stored in this register right-justified. Unused bits read zero.

- **PCS: Peripheral Chip Select Status**

In Master Mode only, these bits indicate the value on the NPCS pins at the end of a transfer. Otherwise, these bits read zero.

- **SCBR: Serial Clock Baud Rate (Code Label `SP_SCBR`)**

In Master Mode, the SPI Interface uses a modulus counter to derive the SPCK baud rate from the SPI Master Clock (selected between MCK and MCK/32). The Baud rate is selected by writing a value from 2 to 255 in the field SCBR. The following equation determines the SPCK baud rate:

$$\text{SPCK\_Baud\_Rate} = \frac{\text{SPI\_Master\_Clock\_frequency}}{2 \times \text{SCBR}}$$

Giving SCBR a value of zero or one disables the baud rate generator. SPCK is disabled and assumes its inactive state value. No serial transfers may occur. At reset, baud rate is disabled.

- **DLYBS: Delay Before SPCK (Code Label `SP_DLYBS`)**

This field defines the delay from NPCS valid to the first valid SPCK transition.

When DLYBS equals zero, the NPCS valid to SPCK transition is 1/2 the SPCK clock period.

Otherwise, the following equation determines the delay:

NPCS_to_SPCK_Delay = DLYBS * SPI_Master_Clock_period

- **DLYBCT: Delay Between Consecutive Transfers (Code Label `SP_DLYBCT`)**

This field defines the delay between two consecutive transfers with the same peripheral without removing the chip select. The delay is always inserted after each transfer and before removing the chip select if needed.

When DLYBCT equals zero, a delay of four SPI Master Clock periods are inserted.

Otherwise, the following equation determines the delay:

Delay_After_Transfer = 32 * DLYBCT * SPI_Master_Clock_period

21.0.5 ADC User Interface

Base Address ADC 0:0xFFFB0000 (Code Label `ADC0_BASE`)
Base Address ADC 1:0xFFFB4000 (Code Label `ADC1_BASE`)

Table 21-2. Register Mapping

Offset	Register	Name	Access	Reset
0x00	Control Register	ADC_CR	Write-only	–
0x04	Mode Register	ADC_MR	Read/Write	0
0x08	Reserved	–	–	–
0x0C	Reserved	–	–	–
0x10	Channel Enable Register	ADC_CHER	Write-only	–
0x14	Channel Disable Register	ADC_CHDR	Write-only	–
0x18	Channel Status Register	ADC_CHSR	Read-only	0
0x1C	Reserved	–	–	–
0x20	Status Register	ADC_SR	Read-only	0
0x24	Interrupt Enable Register	ADC_IER	Write-only	–
0x28	Interrupt Disable Register	ADC_IDR	Write-only	–
0x2C	Interrupt Mask Register	ADC_IMR	Read-only	0
0x30	Convert Data Register 0	ADC_CDR0	Read-only	0
0x34	Convert Data Register 1	ADC_CDR1	Read-only	0
0x38	Convert Data Register 2	ADC_CDR2	Read-only	0
0x3C	Convert Data Register 3	ADC_CDR3	Read-only	0

21.0.8 ADC Channel Enable Register

Register Name: ADC_CHER
Access Type: Write-only
Offset: 0x10

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CH3	CH2	CH1	CH0

- **CH: Channel Enable (Code Label `ADC_CHx`)**

0 = No effect.

1 = Enables the corresponding channel.

21.0.9 ADC Channel Disable Register

Register Name: ADC_CHDR
Access Type: Write-only
Offset: 0x14

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CH3	CH2	CH1	CH0

- **CH: Channel Disable (Code Label `ADC_CHx`)**

0 = No effect.

1 = Disables the corresponding channel.

21.0.15 ADC Convert Data Register

Register Name: ADC_CDR0 to ADC_CDR3
Access Type: Read-only
Reset State: 0
Offset: 0x30 to 0x3C

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	DATA	

7	6	5	4	3	2	1	0
DATA							

- **DATA: Converted Data**

The analog-to-digital conversion data is placed into this register at the end of a conversion and remains until a new conversion is completed. The Convert Data Register (CDR) is only loaded if the corresponding analog channel is enabled.

DATA	Selected DATA	Code Label: `ADC_CDRx`
0 or 1	10-bits Data	ADC_DATA_10BITS
0 or 1	8-bits Data	ADC_DATA_8BITS

27. Errata

The following known errata are applicable to:

- The following datasheets:

  AT91M55800A Summary, 1745S

  AT91M55800A, (This document)

  AT91M55800A, Electrical Characteristics Rev.1727

- 176-lead LQFP and 176-ball BGA devices with the following markings:

27.1 ADC: ADC Characteristics and Behavior

The tracking time has a theoretical minimum duration. It equals one ADC Clock period and is normally ensured by the ADC Controller.

It might randomly happen that this minimum duration cannot be guaranteed on the first enabled channel. When this happens, the sampling and hold process is too short and the conversion result is wrong.

Problem Fix/Work Around

To use only one channel, the user has to enable two channels and then must use the second channel only.

In the event that all of the ADC channels need to be used, only three channels will be available.

A software work around allows all the channels to be used. It consists of performing several conversions and averaging the samples on the first enabled channel. This method does not support fast conversion. However, signals from temperature sensors, which are slow signals, can be handled by averaging a number of samples.

27.2 Warning: Additional NWAIT Constraints

When the NWAIT signal is asserted during an external memory access, the following EBI behavior is correct:

- NWAIT is asserted before the first rising edge of the master clock and respects the NWAIT to MCKI rising setup timing as defined in the Electrical Characteristics datasheet.
- NWAIT is sampled inactive and at least one standard wait state remains to be executed, even if NWAIT does not meet the NWAIT to first MCKI rising setup timing (i.e., NWAIT is asserted only on the second rising edge of MCKI).

In these cases, the access is delayed as required by NWAIT and the access operations are correctly performed.