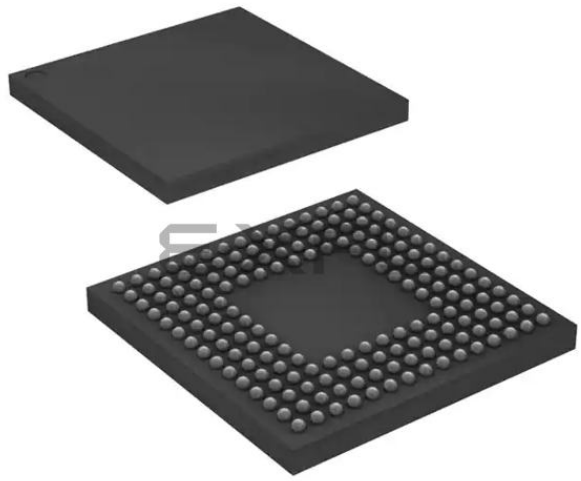

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	33MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, WDT
Number of I/O	58
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91m55800a-33ci

7.7 External Bus Interface

The External Bus Interface handles the accesses between addresses 0x0040 0000 and 0xFFC0 0000. It generates the signals that control access to the external devices, and can configure up to eight 16-Mbyte banks. In all cases it supports byte, half-word and word aligned accesses.

For each of these banks, the user can program:

- Number of wait states
- Number of data float times (wait time after the access is finished to prevent any bus contention in case the device is too long in releasing the bus)
- Data bus width (8-bit or 16-bit)
- With a 16-bit wide data bus, the user can program the EBI to control one 16-bit device (Byte Access Select Mode) or two 8-bit devices in parallel that emulate a 16-bit memory (Byte-write Access mode).

The External Bus Interface features also the Early Read Protocol, configurable for all the devices, that significantly reduces access time requirements on an external device.

11.6 Read Protocols

The EBI provides two alternative protocols for external memory read access: standard and early read. The difference between the two protocols lies in the timing of the NRD (read cycle) waveform.

The protocol is selected by the DRP field in EBI_MCR (Memory Control Register) and is valid for all memory devices. Standard read protocol is the default protocol after reset.

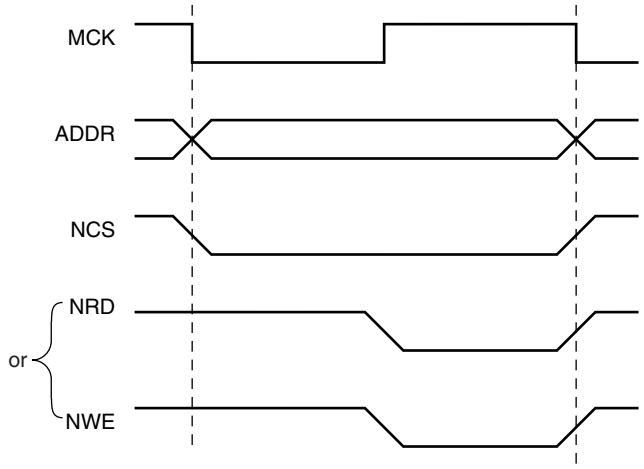
Note: In the following waveforms and descriptions, **NRD** represents NRD and NOE since the two signals have the same waveform. Likewise, **NWE** represents NWE, NWR0 and NWR1 unless NWR0 and NWR1 are otherwise represented. **ADDR** represents A0 - A23 and/or A1 - A23.

11.6.1 Standard Read Protocol

Standard read protocol implements a read cycle in which NRD and NWE are similar. Both are active during the second half of the clock cycle. The first half of the clock cycle allows time to ensure completion of the previous access as well as the output of address and NCS before the read cycle begins.

During a standard read protocol, external memory access, NCS is set low and ADDR is valid at the beginning of the access while NRD goes low only in the second half of the master clock cycle to avoid bus conflict (see Figure 11-7). NWE is the same in both protocols. NWE always goes low in the second half of the master clock cycle (see Figure 11-8).

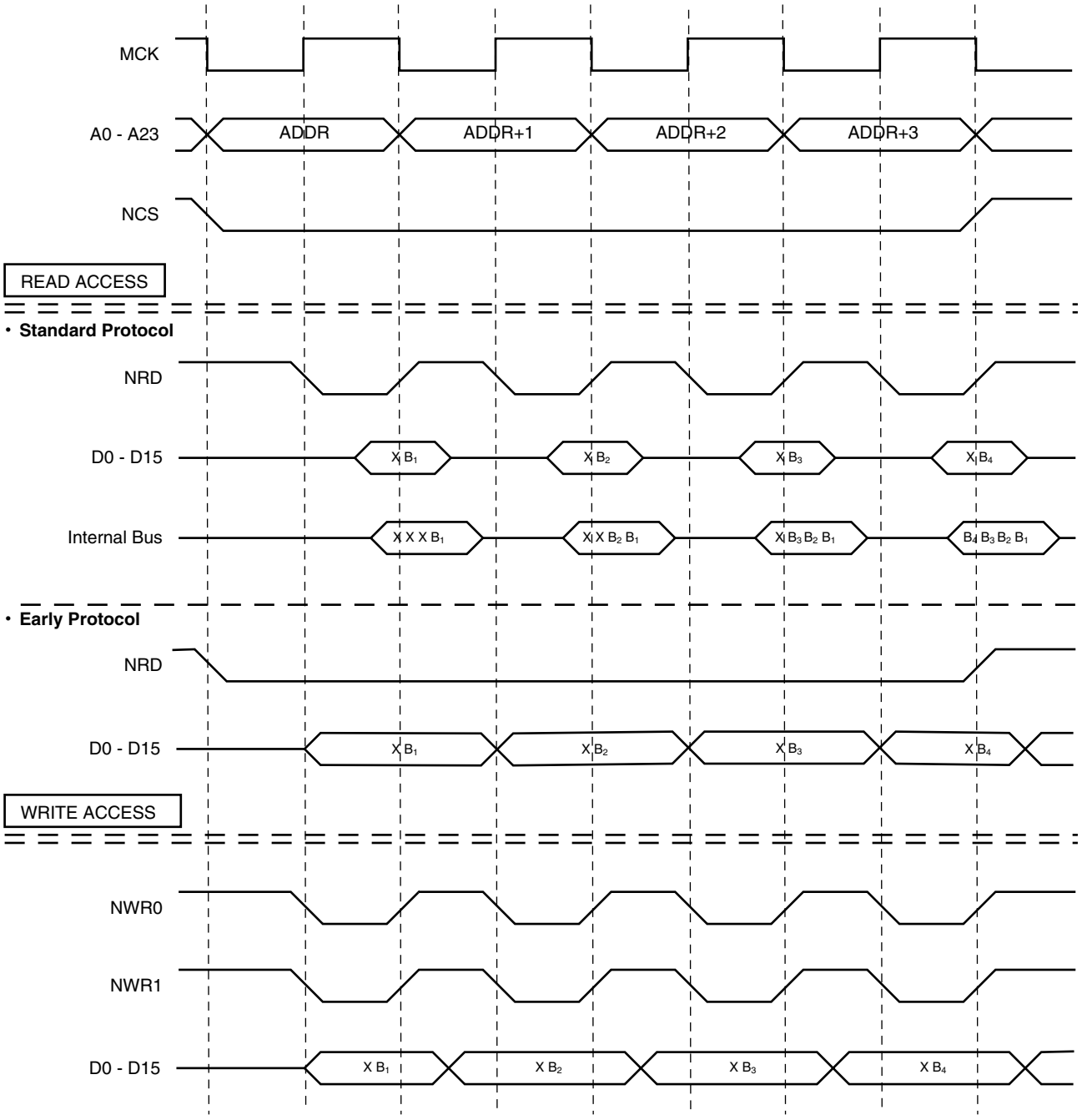
Figure 11-7. Standard Read Protocol



11.6.2 Early Read Protocol

Early read protocol provides more time for a read access from the memory by asserting NRD at the beginning of the clock cycle. In the case of successive read cycles in the same memory, NRD remains active continuously. Since a read cycle normally limits the speed of operation of the external memory system, early read protocol can allow a faster clock frequency to be used. However, an extra wait state is required in some cases to avoid contentions on the external bus.

Figure 11-22. 0 Wait States, 8-bit Bus Width, Word Transfer



15.10.10 AIC Interrupt Disable Command Register

Register Name: AIC_IDCR

Access Type: Write-only

Offset: 0x124

31	30	29	28	27	26	25	24
COMMRX	COMMTX	IRQ0	IRQ1	IRQ2	IRQ3	IRQ4	IRQ5
23	22	21	20	19	18	17	16
SLCKIRQ	–	–	APMCIRQ	RTCIRQ	DAC1IRQ	DAC0IRQ	ADC1IRQ
15	14	13	12	11	10	9	8
ADC0IRQ	PIOBIRQ	PIOAIRQ	WDIRQ	TC5IRQ	TC4IRQ	TC3IRQ	TC2IRQ
7	6	5	4	3	2	1	0
TC1IRQ	TC0IRQ	SPIRQ	US2IRQ	US1IRQ	US0IRQ	SWIRQ	FIQ

- Interrupt Disable

0 = No effect.

1 = Disables corresponding interrupt.

15.10.11 AIC Interrupt Clear Command Register

Register Name: AIC_ICCR

Access Type: Write-only

Offset: 0x128

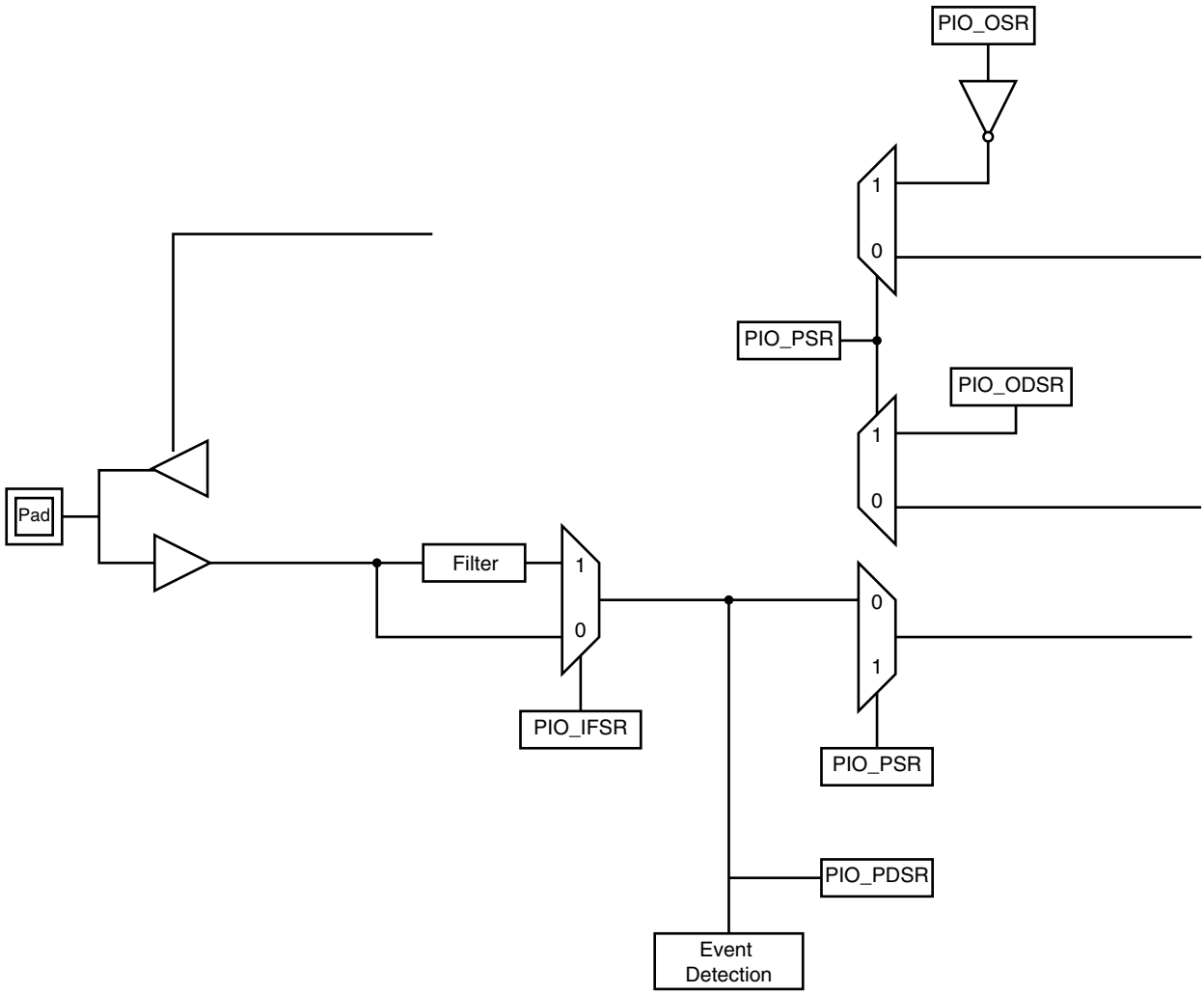
31	30	29	28	27	26	25	24
COMMRX	COMMTX	IRQ0	IRQ1	IRQ2	IRQ3	IRQ4	IRQ5
23	22	21	20	19	18	17	16
SLCKIRQ	–	–	APMCIRQ	RTCIRQ	DAC1IRQ	DAC0IRQ	ADC1IRQ
15	14	13	12	11	10	9	8
ADC0IRQ	PIOBIRQ	PIOAIRQ	WDIRQ	TC5IRQ	TC4IRQ	TC3IRQ	TC2IRQ
7	6	5	4	3	2	1	0
TC1IRQ	TC0IRQ	SPIRQ	US2IRQ	US1IRQ	US0IRQ	SWIRQ	FIQ

- Interrupt Clear

0 = No effect.

1 = Clears corresponding interrupt.

Figure 16-1. Parallel I/O Multiplexed with a Bi-directional Signal



Note: 1. See “Section 16.8 ”PIO Connection Tables” .”

Table 16-2. PIO Controller B Connection Table

PIO Controller		Peripheral					
Bit Number	Port Name	Port Name	Signal Description	Signal Direction	OFF Value[1]	Reset State	Pin Number
0	PB0	–	–	–	–	PIO Input	139
1	PB1	–	–	–	–	PIO Input	140
2	PB2	–	–	–	–	PIO Input	141
3	PB3	IRQ4	External Interrupt 4	Input	0	PIO Input	142
4	PB4	IRQ5	External Interrupt 5	Input	0	PIO Input	143
5	PB5	–	–	–	0	PIO Input	144
6	PB6	AD0TRIG	ADC0 External Trigger	Input	0	PIO Input	145
7	PB7	AD1TRIG	ADC1 External Trigger	Input	0	PIO Input	146
8	PB8	–	–	–	–	PIO Input	149
9	PB9	–	–	–	–	PIO Input	150
10	PB10	–	–	–	–	PIO Input	151
11	PB11	–	–	–	–	PIO Input	152
12	PB12	–	–	–	–	PIO Input	153
13	PB13	–	–	–	–	PIO Input	154
14	PB14	–	–	–	–	PIO Input	155
15	PB15	–	–	–	–	PIO Input	156
16	PB16	–	–	–	–	PIO Input	157
17	PB17	–	–	–	–	PIO Input	158
18	PB18	BMS	Boot Mode Select	Input	0	PIO Input	163
19	PB19	TCLK0	Timer 0 Clock signal	Input	0	PIO Input	55
20	PB20	TIOA0	Timer 0 Signal A	Bi-directional	0	PIO Input	56
21	PB21	TIOB0	Timer 0 Signal B	Bi-directional	0	PIO Input	57
22	PB22	TCLK1	Timer 1 Clock signal	Input	0	PIO Input	58
23	PB23	TIOA1	Timer 1 Signal A	Bi-directional	0	PIO Input	61
24	PB24	TIOB1	Timer 1 Signal B	Bi-directional	0	PIO Input	62
25	PB25	TCLK2	Timer 2 Clock signal	Input	0	PIO Input	63
26	PB26	TIOA2	Timer 2 Signal A	Bi-directional	0	PIO Input	64
27	PB27	TIOB2	Timer 2 Signal B	Bi-directional	0	PIO Input	65
28	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–

Note: 1. The OFF value is the default level seen on the peripheral input when the PIO line is enabled.

Table 24-1. Common Dimensions (mm)

Symbol	Min	Nom	Max
c	0.09		0.20
c1	0.09		0.16
L	0.45	0.6	0.75
L1		1.00 REF	
R2	0.08		0.2
R1	0.08		
S	0.2		
q	0!	3.5!	7!
’ 1	0!		
’ 2	11!	12!	13!
’ 3	11!	12!	13!
A			1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
Tolerances of form and position			
aaa		0.2	
bbb		0.2	

Table 24-2. Lead Count Dimensions (mm)

Pin Count	D/E BSC	D1/E1 BSC	b			b1			e BSC	ccc	ddd
			Min	Nom	Max	Min	Nom	Max			
176	26.0	24.0	0.17	0.20	0.27	0.17	0.20	0.23	0.50	0.10	0.08

Table 24-3. Device and 176-lead LQFP Package Maximum Weight

2023	mg