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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	50MHz
Non-Volatile Memory	-
On-Chip RAM	12kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1401awbstz-rl

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REVISION HISTORY

11/10—Rev. 0 to Rev. A

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4/10—Revision 0: Initial Version

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Signal-to-Noise Ratio					
A-Weighted		100		dB	
Dynamic Range					−60 dB with respect to full-scale analog input
A-Weighted	92	100		dB	
Total Harmonic Distortion + Noise		−83		dB	−3 dB with respect to full-scale analog input
Interchannel Gain Mismatch		25	250	mdB	
Crosstalk		−82		dB	Analog channel-to-channel crosstalk
DC Bias	1.4	1.5	1.6	V	
Gain Error	−11		+11	%	
DAC OUTPUTS					
Number of Channels		4			Two stereo output channels
Resolution		24		Bits	
Full-Scale Analog Output		0.85 (2.4)		V rms (V p-p)	Sine wave
Signal-to-Noise Ratio					
A-Weighted		104		dB	
Dynamic Range					−60 dB with respect to full-scale analog output
A-Weighted	98	104		dB	
Total Harmonic Distortion + Noise		−90		dB	−1 dB with respect to full-scale analog output
Crosstalk		−100		dB	Analog channel-to-channel crosstalk
Interchannel Gain Mismatch		25	250	mdB	
Gain Error	−10		+10	%	
DC Bias	1.4	1.5	1.6	V	
VOLTAGE REFERENCE					
Absolute Voltage, CM Pin	1.4	1.5	1.6	V	
AUXILIARY ADC					
Full-Scale Analog Input	2.8	2.95	3.1	V	
INL		0.5		LSB	
DNL		0.5		LSB	
Offset		15		mV	
Input Impedance	17.8	30	42	kΩ	

DIGITAL INPUT/OUTPUT

Table 3.

Parameter	Min	Typ	Max[1]	Unit	Test Conditions/Comments
Input Voltage, High (V_{IH})	2.0		IOVDD	V	
Input Voltage, Low (V_{IL})			0.8	V	
Input Leakage, High (I_{IH})			1	µA	Excluding MCLKI
Input Leakage, Low (I_{IL})			1	µA	Excluding MCLKI and bidirectional pins
Bidirectional Pin Pull-Up Current, Low			150	µA	
MCLKI Input Leakage, High (I_{IH})			3	µA	
MCLKI Input Leakage, Low (I_{IL})			3	µA	
Output Voltage, High (V_{OH})	2.0			V	I_{OH} = 2 mA
Output Voltage, Low (V_{OL})			0.8	V	I_{OL} = 2 mA
Input Capacitance			5	pF	
GPIO Output Drive		2		mA	

[1] Maximum specifications are measured across a temperature range of −40°C to +130°C (case), a DVDD range of 1.62 V to 1.98 V, and an AVDD range of 2.97 V to 3.63 V.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

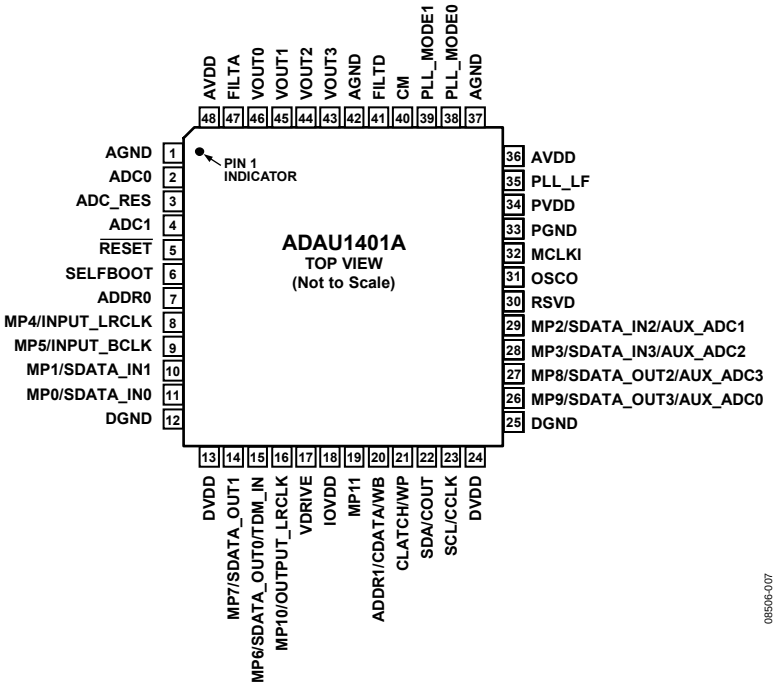

Figure 7. 48-Lead LQFP Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 37, 42	AGND	PWR	Analog Ground Pin. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. AGND should be decoupled to an AVDD pin with a 100 nF capacitor.
2	ADC0	A_IN	Analog Audio Input 0. Full-scale 100 µA rms input. The current input allows the input voltage level to be scaled with an external resistor. An 18 kΩ resistor results in a 2 V rms full-scale input. See the Audio ADCS section for details.
3	ADC_RES	A_IN	ADC Reference Current. The full-scale current of the ADCs can be set with an external 18 kΩ resistor connected between this pin and ground. See the Audio ADCS section for details.
4	ADC1	A_IN	Analog Audio Input 1. Full-scale 100 µA rms input. The current input allows the input voltage level to be scaled with an external resistor. An 18 kΩ resistor results in a 2 V rms full-scale input.
5	$\overline{\text{RESET}}$	D_IN	Active Low Reset Input. Reset is triggered on a high-to-low edge, and the ADAU1401A exits reset on a low-to-high edge. For more information about initialization, see the Power-Up Sequence section for details.
6	SELFBOOT	D_IN	Enable/Disable Self-Boot. SELFBOOT selects control port (low) or self-boot (high). Setting this pin high initiates a self-boot operation when the ADAU1401A is brought out of a reset. This pin can be tied directly to the control voltage or pulled up/down with a resistor. See the Self-Boot section.
7	ADDR0	D_IN	I^2C and SPI Address 0. In combination with ADDR1, this pin allows up to four ADAU1401A devices to be used on the same I^2C bus or up to two ICs to be used with a common SPI CLATCH signal. See the I^2C Port section for details.
8	MP4/INPUT_LRCLK	D_IO	Multipurpose GPIO/Serial Input Port LRCLK. See the Multipurpose Pins section for more details.
9	MP5/INPUT_BCLK	D_IO	Multipurpose GPIO/Serial Input Port BCLK. See the Multipurpose Pins section for more details.
10	MP1/SDATA_IN1	D_IO	Multipurpose GPIO/Serial Input Port Data 1. See the Multipurpose Pins section for more details.
11	MP0/SDATA_IN0	D_IO	Multipurpose GPIO/Serial Input Port Data 0. See the Multipurpose Pins section for more details.
12, 25	DGND	PWR	Digital Ground Pin. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. DGND should be decoupled to a DVDD pin with a 100 nF capacitor.
13, 24	DVDD	PWR	1.8 V Digital Supply. The input for this pin can be supplied either externally or generated

Pin No.	Mnemonic	Type[1]	Description
			from a 3.3 V supply with the on-board 1.8 V regulator. DVDD should be decoupled to DGND with a 100 nF capacitor.
14	MP7/SDATA_OUT1	D_IO	Multipurpose GPIO/Serial Output Port Data 1. See the Multipurpose Pins section for more details.
15	MP6/SDATA_OUT0/ TDM_IN	D_IO	Multipurpose GPIO/Serial Output Port Data 0/TDM Data Input. See the Multipurpose Pins section for more details.
16	MP10/OUTPUT_LRCLK	D_IO	Multipurpose GPIO/Serial Output Port LRCLK. See the Multipurpose Pins section for more details.
17	VDRIVE	A_OUT	Drive for 1.8 V Regulator. The base of the voltage regulator external PNP transistor is driven from VDRIVE. See the Voltage Regulator section for details.
18	IOVDD	PWR	Supply for Input and Output Pins. The voltage on this pin sets the highest input voltage that should be seen on the digital input pins. This pin is also the supply for the digital output signals on the control port and MPx pins. IOVDD should always be set to 3.3 V. The current draw of this pin is variable because it is dependent on the loads of the digital outputs.
19	MP11	D_IO	Multipurpose GPIO or Serial Output Port BCLK (OUTPUT_BCLK). See the Multipurpose Pins section for more details.
20	ADDR1/CDATA/WB	D_IN	I^2C Address 1/SPI Data Input/EEPROM Writeback Trigger. ADDR1 in combination with ADDR0 sets the I^2C address of the IC so that four ADAU1401A devices can be used on the same I^2C bus (see the I^2C Port section for details). For more information about the CDATA function of this pin, see the SPI Port section. A rising (default) or falling (if set by EEPROM messages) edge on the WB pin triggers a writeback of the interface registers to the external EEPROM. This function can be used to save parameter data on power-down (see the Self-Boot section for details).
21	CLATCH/WP	D_IO	SPI Latch Signal/Self-Boot EEPROM Write Protect. CLATCH must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction can take a different number of cycles on the CCLK pin to complete, depending on the address and read/write bit that are sent at the beginning of the SPI transaction (see the SPI Port section for details). The WP pin is an open-collector output when the device is in self-boot mode. The ADAU1401A pulls WP low to enable writes to an external EEPROM. This pin should be pulled high to 3.3 V (see the Self-Boot section for details).
22	SDA/COUT	D_IO	I^2C Data/SPI Data Output. SDA is a bidirectional open collector. The line connected to SDA should have a 2.2 kΩ pull-up resistor (see the I^2C Port section for details). COUT is used for reading back registers and memory locations. It is three-stated when an SPI read is not active (see the SPI Port section for details).
23	SCL/CCLK	D_IO	I^2C Clock/SPI Clock. SCL is always an open-collector input when in I^2C control mode. In self-boot mode, SCL is an open-collector output (I^2C master). The line connected to SCL should have a 2.2 kΩ pull-up resistor (see the I^2C Port section for details). CCLK can either run continuously or be gated off between SPI transactions (see the SPI Port section for details).
26	MP9/SDATA_OUT3/ AUX_ADC0	D_IO/A_IO	Multipurpose GPIO/Serial Output Port Data 3/Auxiliary ADC Input 0. See the Multipurpose Pins section for more details.
27	MP8/SDATA_OUT2/ AUX_ADC3	D_IO/A_IO	Multipurpose GPIO/Serial Output Port Data 2/Auxiliary ADC Input 3. See the Multipurpose Pins section for more details.
28	MP3/SDATA_IN3/ AUX_ADC2	D_IO/A_IO	Multipurpose GPIO/Serial Input Port Data 3/Auxiliary ADC Input 2. See the Multipurpose Pins section for more details.
29	MP2/SDATA_IN2/ AUX_ADC1	D_IO/A_IO	Multipurpose GPIO/Serial Input Port Data 2/Auxiliary ADC Input 1. See the Multipurpose Pins section for more details.
30	RSVD		Reserved. Tie this pin to ground, either directly or through a pull-down resistor.
31	OSCO	D_OUT	Crystal Oscillator Circuit Output. A 100 Ω damping resistor should be connected between this pin and the crystal. This output should not be used to directly drive a clock to another IC. If the crystal oscillator is not used, this pin can be left unconnected. See the Using the Oscillator section for details.
32	MCLKI	D_IN	Master Clock Input. This pin can either be connected to a 3.3 V clock signal or be the input from the crystal oscillator circuit. See the Setting Master Clock/PLL Mode section for details.
33	PGND	PWR	PLL Ground Pin. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. PGND should be decoupled to PVDD with a 100 nF capacitor.
34	PVDD	PWR	3.3 V Power Supply for the PLL and the Auxiliary ADC Analog Section. This pin should be decoupled to PGND with a 100 nF capacitor.
35	PLL_LF	A_OUT	PLL Loop Filter Connection. Two capacitors and a resistor must be connected to this pin, as shown in Figure 15. See the Setting Master Clock/PLL Mode section for more details.
36, 48	AVDD	PWR	3.3 V Analog Supply. This pin should be decoupled to AGND with a 100 nF capacitor.

Pin No.	Mnemonic	Type[1]	Description
38, 39	PLL_MODE0, PLL_MODE1	D_IN	PLL Mode Setting. These pins set the output frequency of the master clock PLL. See the Setting Master Clock/PLL Mode section for more details.
40	CM	A_OUT	1.5 V Common-Mode Reference. A 47 µF decoupling capacitor should be connected between this pin and ground to reduce crosstalk between the ADCs and DACs. The material of the capacitors is not critical. This pin can be used to bias external analog circuits, as long as those circuits are not drawing current from the pin (such as when the CM pin is connected to the noninverting input of an op amp).
41	FILTD	A_OUT	DAC Filter Decoupling Pin. A 10 µF capacitor should be connected between this pin and ground. The capacitor material is not critical. The voltage on this pin is 1.5 V.
43	VOUT3	A_OUT	VOUT3 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with an active or passive output reconstruction filter. See the Audio DACS section for details.
44	VOUT2	A_OUT	VOUT2 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with an active or passive output reconstruction filter. See the Audio DACS section for details.
45	VOUT1	A_OUT	VOUT1 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with an active or passive output reconstruction filter. See the Audio DACS section for details.
46	VOUT0	A_OUT	VOUT0 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with an active or passive output reconstruction filter. See the Audio DACS section for details.
47	FILTA	A_OUT	ADC Filter Decoupling Pin. A 10 µF capacitor should be connected between this pin and ground. The capacitor material is not critical. The voltage on this pin is 1.5 V.

[1] PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_IO = digital input/output, D_IO/A_IO = digital input/output or analog input/output.

INITIALIZATION

This section describes the procedure for properly setting up the ADAU1401A. The following five-step sequence provides an overview of how to initialize the IC:

1. Apply power to the ADAU1401A.
2. Wait for the PLL to lock.
3. Load the SigmaDSP program and parameters.
4. Set up registers (including multipurpose pins and digital interfaces).
5. Turn off the default muting of the converters, clear the data registers, and initialize the DAC setup register (see the Control Registers Setup section for specific settings).

To only test analog audio pass-through (ADCs to DACs), skip Step 3 and Step 4 and use the default internal program.

POWER-UP SEQUENCE

The ADAU1401A has a built-in power-up sequence that initializes the contents of all internal RAMs on power-up or when the device is brought out of a reset. On the rising edge of RESET, the contents of the internal program boot ROM are copied to the internal program RAM memory, the parameter RAM is filled with values (all 0s) from its associated boot ROM, and all registers are initialized to 0s. The default boot ROM program copies audio from the inputs to the outputs without processing it (see Figure 13). In this program, SDATA_IN0 and SDATA_IN1 are output on DAC0 and DAC1 and on SDATA_OUT0 and SDATA_OUT1. ADC0 and ADC1 are output on DAC2 and DAC3. The data memories are also zeroed at power-up. New values should not be written to the control port until the initialization is complete.

Table 12. Power-Up Time

MCLKI Input Frequency	Init. Time	Maximum Program/ Parameter/Register Boot Time (I^2C)	Total Time
3.072 MHz (64 × f_S)	85 ms	175 ms	260 ms
11.2896 MHz (256 × f_S)	23 ms	175 ms	198 ms
12.288 MHz (256 × f_S)	21 ms	175 ms	196 ms
18.432 MHz (384 × f_S)	16 ms	175 ms	191 ms
24.576 MHz (512 × f_S)	11 ms	175 ms	186 ms

The PLL start-up time lasts for 2^{18} cycles of the clock on the MCLKI pin. This time ranges from 10.7 ms for a 24.576 MHz (512 × f_S) input clock to 85.3 ms for a 3.072 MHz (64 × f_S) input clock and is measured from the rising edge of RESET. Following the PLL startup, the duration of the ADAU1401A boot cycle is about 42 µs for a f_S of 48 kHz. The user should avoid writing to or reading from the ADAU1401A during this start-up time. For an MCLKI input signal of 12.288 MHz, the full initialization sequence (PLL startup plus boot cycle) is approximately 21 ms. As the device comes out of a reset, the clock mode is immediately set by the PLL_MODE0 and PLL_MODE1 pins. The reset is synchronized to the falling edge of the internal clock.

Table 12 lists typical times to boot the ADAU1401A into an operational state for an application, assuming a 400 kHz I^2C clock loading a full program, parameter set, and all registers (about 8.5 kB). In reality, most applications do not fill the RAMs and, therefore, boot time is less than the value listed in Column 3 of Table 12.

CONTROL REGISTERS SETUP

The following registers must be set as described in this section to initialize the ADAU1401A. These settings are the basic minimum settings needed to operate the IC with an analog input/output of 48 kHz. More registers may need to be set, depending on the application. See the RAMs and Registers section for additional settings.

DSP Core Control Register (Address 2076)

Set Bits[4:2] (ADM, DAM, and CR) each to 111.

DAC Setup Register (Address 2087)

Set Bits[1:0] (DS[1:0]) to 01.

RECOMMENDED PROGRAM/PARAMETER LOADING PROCEDURE

When writing large amounts of data to the program or parameter RAM in direct write mode, the processor core should be disabled to prevent unpleasant noises from appearing in the audio output. To disable the processor core,

1. Set Bits[4:3] (active low) of the DSP core control register (Address 2076) to 1 to mute the ADCs and DACs. This begins a volume ramp-down.
2. Set Bit 2 (active low) of the DSP core control register to 1. This zeroes the SigmaDSP accumulators, the data output registers, and the data input registers.
3. Fill the program RAM using burst mode writes.
4. Fill the parameter RAM using burst mode writes.
5. Set Bits[4:2] of the DSP core control register to 111.

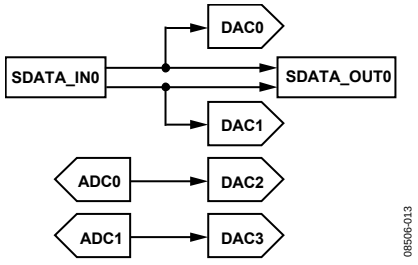

Figure 13. Default Program Signal Flow

POWER REDUCTION MODES

Sections of the ADAU1401A chip can be turned on and off as needed to reduce power consumption. These include the ADCs, DACs, and voltage reference.

The individual analog sections can be turned off by writing to the auxiliary ADC and power control register (Address 2082). By default, the ADCs, DACs, and reference are enabled (all bits

VOLTAGE REGULATOR

The digital voltage of the ADAU1401A must be set to 1.8 V. The chip includes an on-board voltage regulator that allows the device to be used in systems without an available 1.8 V supply but with an available 3.3 V supply. The only external components needed in such instances are a PNP transistor, a resistor, and a few bypass capacitors. Only one pin, VDRIVE, is necessary to support the regulator.

The recommended design for the voltage regulator is shown in Figure 16. The 10 µF and 100 nF capacitors shown in this configuration are recommended for bypassing, but are not necessary for operation. Each DVDD pin should have its own 100 nF bypass capacitor, but only one bulk capacitor (10 µF to 47 µF) is needed for both DVDD pins. With this configuration, 3.3 V is the main system voltage; 1.8 V is generated at the transistor's collector, which is connected to the DVDD pins. VDRIVE is connected to the base of the PNP transistor. If the regulator is not used in the design, VDRIVE can be tied to ground.

Two specifications must be considered when choosing a regulator transistor: the transistor's current amplification factor (h_{FE} or beta) should be at least 100, and the transistor's collector must be able to dissipate the heat generated when regulating from 3.3 V to 1.8 V. The maximum digital current drawn from the ADAU1401A is 40 mA. The equation to determine the minimum power dissipation of the transistor is as follows:

$$(3.3\ V - 1.8\ V) \times 60\ mA = 90\ mW$$

There are many transistors with these specifications available in small SOT-23 or SOT-223 packages.

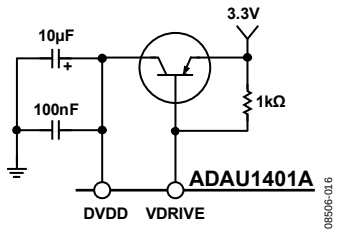

Figure 16. Voltage Regulator Configuration

I²C Read and Write Operations

Figure 22 shows the timing of a single-word write operation. On every ninth clock, the ADAU1401A issues an acknowledge by pulling SDA low.

Figure 23 shows the timing of a burst mode write sequence. This figure shows an example where the target destination registers are two bytes. The ADAU1401A knows to increment its subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with a word length of two bytes.

The timing of a single-word read operation is shown in Figure 24. Note that the first R/$\overline{W}$ bit is 0, indicating a write operation. This is because the subaddress still needs to be written to set up the internal address. After the ADAU1401A acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ bit set to 1 (read). This causes the ADAU1401A SDA to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the ADAU1401A.

Figure 25 shows the timing of a burst mode read sequence. This figure shows an example where the target read registers are two bytes. The ADAU1401A increments its subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with word lengths of two bytes. Other addresses may have word lengths ranging from one to five bytes. The ADAU1401A always decodes the subaddress and sets the auto-increment circuit so that the address increments after the appropriate number of bytes.

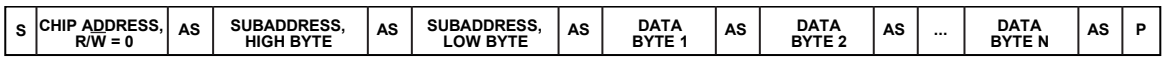

Figure 22. Single-Word I²C Write Format

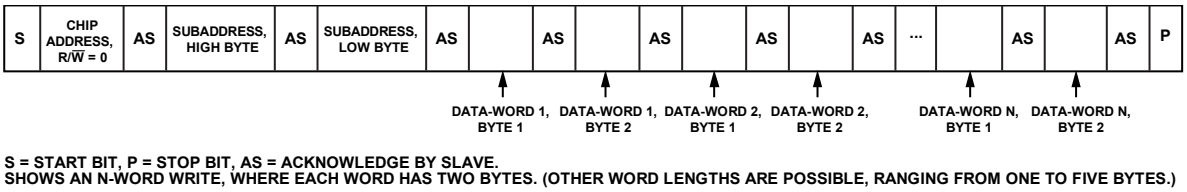

Figure 23. Burst Mode I²C Write Format

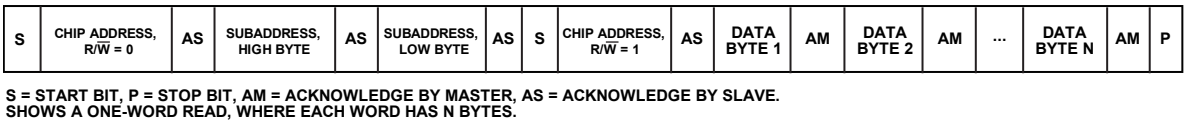

Figure 24. Single-Word I²C Read Format

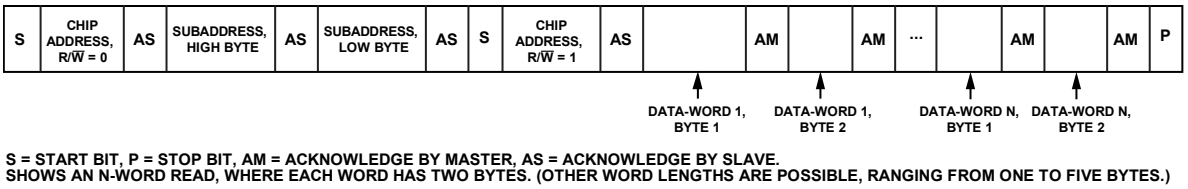

Figure 25. Burst Mode I²C Read Format

SIGNAL PROCESSING

The ADAU1401A is designed to provide all audio signal processing functions commonly used in stereo or multichannel playback systems. The signal processing flow is designed using the SigmaStudio software, which allows graphical entry and real-time control of all signal processing functions.

Many of the signal processing functions are coded using full, 56-bit, double-precision arithmetic data. The input and output word lengths of the DSP core are 24 bits. Four extra headroom bits are used in the processor to allow internal gains of up to 24 dB without clipping. Additional gains can be achieved by initially scaling down the input signal in the DSP signal flow.

NUMERIC FORMATS

DSP systems commonly use a standard numeric format. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The ADAU1401A uses the same numeric format for both the parameter and data values. The format is as described in the Numerical Format: 5.23 section.

Numerical Format: 5.23

Linear range: −16.0 to (+16.0 − 1 LSB)

Examples:
1000 0000 0000 0000 0000 0000 0000 = −16.0
1110 0000 0000 0000 0000 0000 0000 = −4.0
1111 1000 0000 0000 0000 0000 0000 = −1.0
1111 1110 0000 0000 0000 0000 0000 = −0.25
1111 1111 0011 0011 0011 0011 0011 = −0.1
1111 1111 1111 1111 1111 1111 1111 = (1 LSB below 0.0)
0000 0000 0000 0000 0000 0000 0000 = 0.0
0000 0000 1100 1100 1100 1100 1101 = 0.1
0000 0010 0000 0000 0000 0000 0000 = 0.25
0000 1000 0000 0000 0000 0000 0000 = 1.0
0010 0000 0000 0000 0000 0000 0000 = 4.0
0111 1111 1111 1111 1111 1111 1111 = (16.0 − 1 LSB).

The serial port accepts up to 24 bits on the input and is sign-extended to the full 28 bits of the DSP core. This allows internal gains of up to 24 dB without internal clipping.

A digital clipper circuit is used between the output of the DSP core and the DACs or serial port outputs (see Figure 29). This clips the top four bits of the signal to produce a 24-bit output with a range of 1.0 (minus 1 LSB) to −1.0. Figure 29 indicates the maximum signal levels at each point in the data flow in both binary and decibel levels.

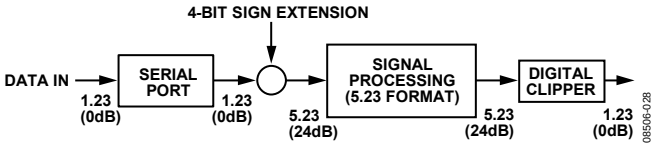

Figure 29. Numeric Precision and Clipping Structure

PROGRAMMING

On power-up, the ADAU1401A default program passes the unprocessed input signals to the outputs (shown in Figure 13), but the outputs are muted by default (see the Power-Up Sequence section). There are 1024 instruction cycles per audio sample, resulting in about 50 MIPS being available. The SigmaDSP runs in a stream-oriented manner, meaning that all 1024 instructions are executed each sample period. The ADAU1401A can also be set to accept double- or quad-speed inputs by reducing the number of instructions per sample that are set in the DSP core control register.

The part can be easily programmed using SigmaStudio (see Figure 30), a graphical tool provided by Analog Devices. No knowledge of writing line-level DSP code is required. More information about SigmaStudio can be found at www.analog.com.

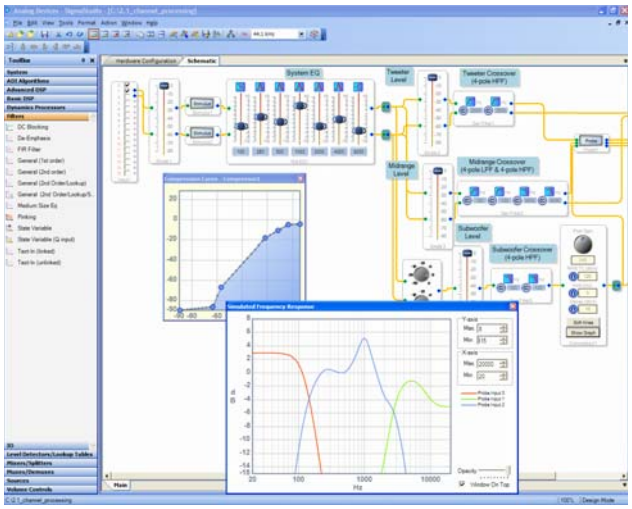

Figure 30. SigmaStudio Screen Shot

RAMS AND REGISTERS

Table 21. RAM Map and Read/Write Modes

Memory	Size	Address Range	Read	Write	Write Modes
Parameter RAM	1024 × 32	0 to 1023 (0x0000 to 0x03FF)	Yes	Yes	Direct write,[1] safeload write
Program RAM	1024 × 40	1024 to 2047 (0x0400 to 0x07FF)	Yes	Yes	Direct write[1]

[1] Internal registers should be cleared first to prevent clicks and pops.

ADDRESS MAPS

Table 21 shows the RAM map, whereas Table 32 shows the ADAU1401A register map. The address space encompasses a set of registers and two RAMs: one RAM holds the signal processing parameters and the other RAM holds the program instructions. The program RAM and parameter RAM are initialized on power-up from on-board boot ROMs (see the Power-Up Sequence section).

All RAMs and registers have a default value of all 0s, except for the program RAM, which is loaded with the default program (see the Initialization section).

PARAMETER RAM

The parameter RAM is 32 bits wide and occupies Address 0 to Address 1023. Each parameter is padded with four 0s before the MSB to extend the 28-bit word to a full 4-byte width. The parameter RAM is initialized to all 0s on power-up. The data of the parameter RAM is in twos complement, 5.23 format. This means that the coefficients can range from +16.0 (minus 1 LSB) to −16.0, with 1.0 represented by the binary word 0000 1000 0000 0000 0000 0000 0000 or by the hexadecimal word 0x00 0x80 0x00 0x00.

The parameter RAM can be written using one of the two following methods: a direct read/write or a safeload write.

Direct Read/Write

The direct read/write method allows direct access to the program RAM and parameter RAM. This mode of operation is typically used when loading a new RAM using burst mode addressing. The clear registers bit in the DSP core control register should be set to 0 when this mode is used to prevent clicks and pops in the outputs. Note that this mode can be used during live program execution, but because there is no handshaking between the core and the control port, the parameter RAM is unavailable to the DSP core during control writes, resulting in clicks and pops in the audio stream.

Safeload Write

Up to five safeload registers can be loaded with the parameter RAM address and data. The data is then transferred to the requested address when the RAM is not busy. This method can be used for dynamic updates while live program material is playing through the ADAU1401A. For example, a complete update of one biquad section can occur in one audio frame while the RAM is not busy. This method is not available for writing to the program RAM or control registers.

DATA RAM

The ADAU1401A data RAM is used to store audio data-words for processing. For the most part, this process is transparent to the user. The user cannot address the RAM space, which has a size of 2k words, directly from the control port.

Data RAM utilization should be considered when implementing blocks that require large amounts of data RAM space, such as delays. The SigmaDSP core processes delay times in one-sample increments; therefore, the total pool of delay available to the user equals 2048 multiplied by the sample period. For a f_S of 48 kHz, the pool of available delay is a maximum of about 43 ms. In practice, this much data memory is not available to the user because every block in a design uses a few data memory locations for its processing. In most DSP programs, this does not significantly impact the total delay time. The SigmaStudio compiler manages the data RAM and indicates if the number of addresses needed in the design exceeds the maximum number available.

READ/WRITE DATA FORMATS

The read/write formats of the control port are designed to be byte oriented. This allows easy programming of common microcontroller chips. To fit into a byte-oriented format, 0s are appended to the data fields before the MSB to extend the data-word to eight bits. For example, 28-bit words written to the parameter RAM are appended with four leading 0s to equal 32 bits (four bytes), whereas 40-bit words written to the program RAM are not appended with 0s because they are already a full five bytes. These zero-padded data fields are appended to a 3-byte field consisting of a 7-bit chip address, a read/write bit, and an 11-bit RAM/register address. The control port knows how many data bytes to expect based on the address given in the first three bytes.

The total number of bytes for a single-location write command can vary from four bytes (for a control register write) to eight bytes (for a program RAM write). Burst mode can be used to fill contiguous register or RAM locations. A burst mode write begins by writing the address and data of the first RAM or register location to be written. Rather than ending the control port transaction (by issuing a stop command in I^2C mode or by bringing the CLATCH signal high in SPI mode after the data-word), as would be done in a single-address write, the next data-word can be immediately written without specifying its address. The ADAU1401A control port auto-increments the address of each write, even across the boundaries of different RAMs and registers. Table 23 and Table 25 show examples of burst mode writes.

Table 22. Parameter RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes[4:6]
CHIP_ADR[6:0], $\overline{W}$/R	000000, PARAM_ADR[9:8]	PARAM_ADR[7:0]	0000, PARAM[27:24]	PARAM[23:0]

Table 23. Parameter RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes[4:6]	Bytes[7:10]	Bytes[11:14]
CHIP_ADR[6:0], $\overline{W}$/R	000000, PARAM_ADR[9:8]	PARAM_ADR[7:0]	0000, PARAM[27:24]	PARAM[23:0]	…	…
			<—PARAM_ADR—>		PARAM_ADR + 1	PARAM_ADR + 2

Table 24. Program RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Bytes[3:7]
CHIP_ADR[6:0], $\overline{W}$/R	00000, PROG_ADR[10:8]	PROG_ADR[7:0]	PROG[39:0]

Table 25. Program RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Bytes[3:7]	Bytes[8:12]	Bytes[13:17]
CHIP_ADR[6:0], $\overline{W}$/R	00000, PROG_ADR[10:8]	PROG_ADR[7:0]	PROG[39:0]	…	…
			<—PROG_ADR—>	PROG_ADR + 1	PROG_ADR + 2

Table 26. Control Register Read/Write Format (Core, Serial Out 0, Serial Out 1)

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
CHIP_ADR[6:0], $\overline{W}$/R	0000, REG_ADR[11:8]	REG_ADR[7:0]	Data[15:8]	Data[7:0]

Table 27. Control Register Read/Write Format (RAM Configuration, Serial Input)

Byte 0	Byte 1	Byte 2	Byte 3
CHIP_ADR[6:0], $\overline{W}$/R	0000, REG_ADR[11:8]	REG_ADR[7:0]	Data[7:0]

Table 28. Data Capture Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
CHIP_ADR[6:0], $\overline{W}$/R	0000, DATA_CAPTURE_ADR[11:8]	DATA_CAPTURE_ADR[7:0]	000, PROGCOUNT[10:6][1]	PROGCOUNT[5:0],[1] REGSEL[1:0][2]

[1] PROGCOUNT[10:0] is the value of the program counter when the data capture occurs (the table of values is generated by the SigmaStudio compiler).
[2] REGSEL[1:0] selects one of four registers (see the Address 2074 and Address 2075 (0X081A and 0X081B)—Data Capture Registers section).

Table 29. Data Capture (Control Port Readback) Register Read Format

Byte 0	Byte 1	Byte 2	Bytes[3:5]
CHIP_ADR[6:0], $\overline{W}$/R	0000, DATA_CAPTURE_ADR[11:8]	DATA_CAPTURE_ADR[7:0]	Data[23:0]

Table 30. Safeload Address Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
CHIP_ADR[6:0], $\overline{W}$/R	0000, SAFELOAD_ADR[11:8]	SAFELOAD_ADR[7:0]	000000, PARAM_ADR[9:8]	PARAM_ADR[7:0]

Table 31. Safeload Data Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Bytes[5:7]
CHIP_ADR[6:0], $\overline{W}$/R	0000, SAFELOAD_ADR[11:8]	SAFELOAD_ADR[7:0]	00000000	0000, Data[27:24]	Data[23:0]

ADDRESS 2056 (0x0808)—GPIO PIN SETTING REGISTER

This register allows the user to set the GPIO pins through the control port. High or low settings can be directly written to or read from this register after setting the GPIO pin setting register control port write mode bit (GPCW) in the DSP core control register. This register is updated once every LRCLK frame ($1/f_S$).

Table 35. GPIO Pin Setting Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	0	MP11	MP10	MP09	MP08	MP07	MP06	MP05	MP04	MP03	MP02	MP01	MP00	0x0000

Table 36. GPIO Pin Setting Register Bit Descriptions

Bit Name	Description
MP[11:0]	Setting of the corresponding multipurpose pin when controlled through SPI or I^2C

ADDRESS 2064 TO ADDRESS 2068 (0x0810 TO 0x0814)—SAFELOAD DATA REGISTERS

Many applications require real-time microcontroller control of signal processing parameters, such as filter coefficients, mixer gains, multichannel virtualizing parameters, or dynamics processing curves. When controlling a biquad filter, for example, all of the parameters must be updated at the same time. Doing so prevents the filter from executing with a mix of old and new coefficients for one or two audio frames, thus avoiding temporary instability and transients that may take a long time to decay. To accomplish this, the ADAU1401A uses safeload data registers to simultaneously load a set of five 28-bit values to the desired parameter RAM address. Five registers are used because a biquad filter uses five coefficients and, as previously mentioned, it is desirable to do a complete update in one transaction.

The first step in performing a safeload operation is writing the parameter address to one of the safeload address registers (Address 2069 to Address 2073). The 10-bit data-word to be written is the address in parameter RAM to which the safeload is being performed. After this address is written, the 28-bit data-word can be written to the corresponding safeload data register (Address 2064 to Address 2068).

The data formats for these writes are detailed in Table 30 and Table 31. Table 39 outlines how each of the five address registers maps to its corresponding data register.

After the address and data registers are loaded, set the initiate safeload transfer bit in the DSP core control register to initiate the loading into RAM. Each of the five safeload registers takes one of the 1024 core instructions to load into the parameter RAM. The total program lengths should, therefore, be limited to 1019 cycles (1024 minus 5) to ensure that the SigmaDSP core always has at least five cycles available. The safeload is guaranteed to occur within one LRCLK period (21 μs for a f_S of 48 kHz) of the initiate safeload transfer bit being set.

The safeload logic automatically sends data to be loaded into RAM from only those safeload registers that have been written to since the last safeload operation. For example, if two parameters are to be updated in the RAM, only two of the five safeload registers must be written. When the initiate safeload transfer bit is asserted, only data from those two registers are sent to the RAM; the other three registers are not sent to the RAM and may hold old or invalid data.

Table 39. Safeload Address and Data Register Mapping

Safeload Register	Safeload Address Register	Safeload Data Register
Safeload Data 0	2069	2064
Safeload Data 1	2070	2065
Safeload Data 2	2071	2066
Safeload Data 3	2072	2067
Safeload Data 4	2073	2068

Table 40. Safeload Data Registers Bit Map

D31 D15	D30 D14	D29 D13	D28 D12	D27 D11	D26 D10	D25 D9	D24 D8	D39 D23 D7	D38 D22 D6	D37 D21 D5	D36 D20 D4	D35 D19 D3	D34 D18 D2	D33 D17 D1	D32 D16 D0	Default
								SD39	SD38	SD37	SD36	SD35	SD34	SD33	SD32	0x00
SD31	SD30	SD29	SD28	SD27	SD26	SD25	SD24	SD23	SD22	SD21	SD20	SD19	SD18	SD17	SD16	0x0000
SD15	SD14	SD13	SD12	SD11	SD10	SD09	SD08	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00	0x0000

Table 41. Safeload Data Registers Bit Descriptions

Bit Name	Description
SD[39:0]	Safeload data. Data (program, parameters, register contents) to be loaded into the RAMs or registers.

ADDRESS 2069 TO ADDRESS 2073 (0x0815 TO 0x0819)—SAFELOAD ADDRESS REGISTERS

Table 42. Safeload Address Registers Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	0	SA11	SA10	SA09	SA08	SA07	SA06	SA05	SA04	SA03	SA02	SA01	SA00	0x0000

Table 43. Safeload Address Registers Bit Descriptions

Bit Name	Description
SA[11:0]	Safeload address. Address of the data that is to be loaded into the RAMs or registers.

ADDRESS 2082 (0x0822)—AUXILIARY ADC AND POWER CONTROL REGISTER

Table 55. Auxiliary ADC and Power Control Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	FIL1	FIL0	AAPD	VBPD	VRPD	RSVD	D0PD	D1PD	D2PD	D3PD	0x0000

Table 56. Auxiliary ADC and Power Control Register Bit Descriptions

Bit Name	Description	
FIL[1:0]	Auxiliary ADC filtering	
	Settings	**Function**
	00	4-bit hysteresis (12-bit level)
	01	5-bit hysteresis (12-bit level)
	10	Filter and hysteresis bypassed
	11	Low-pass filter bypassed
AAPD	ADC power-down (both ADCs)	
VBPD	Voltage reference buffer power-down	
VRPD	Voltage reference power-down	
D0PD	DAC0 power-down	
D1PD	DAC1 power-down	
D2PD	DAC2 power-down	
D3PD	DAC3 power-down	

ADDRESS 2084 (0x0824)—AUXILIARY ADC ENABLE REGISTER

Table 57. Auxiliary ADC Enable Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
AAEN	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x0000

Table 58. Auxiliary ADC Enable Register Bit Descriptions

Bit Name	Description
AAEN	Enable the auxiliary ADC

ADDRESS 2086 (0x0826)—OSCILLATOR POWER-DOWN REGISTER

Table 59. Oscillator Power-Down Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	OPD	RSVD	RSVD	0x0000

Table 60. Oscillator Power-Down Register Bit Descriptions

Bit Name	Description
OPD	Oscillator power-down. Powers down the oscillator.

ADDRESS 2087 (0x0827)—DAC SETUP REGISTER

To properly initialize the DACs, Bits DS[1:0] in this register should be set to 01.

Table 61. DAC Setup Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	DS1	DS0	0x0000

Table 62. DAC Setup Register Bit Descriptions

Bit Name	Description	
DS[1:0]	DAC setup.	
	Settings	**Function**
	00	Reserved
	01	Initialize DACs
	10	Reserved
	11	Reserved

clock polarity and data input modes. The valid data formats are I²S, left-justified, right-justified (24-/20-/18-/16-bit), and 8-channel TDM. In all modes except for the right-justified modes, the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but are truncated internally. Proper operation of the right-justified modes requires that there be exactly 64 BCLKs per audio frame. The TDM data is input on SDATA_IN0. The LRCLK in TDM mode can be input to the ADAU1401A either as a 50/50 duty cycle clock or as a bit-wide pulse.

In TDM mode, the ADAU1401A can be a master for 48 kHz and 96 kHz data, but not for 192 kHz data. Table 64 lists the modes in which the serial output port can function.

Table 64. Serial Output Port Master/Slave Mode Capabilities

f_S	2-Channel Modes (I²S, Left Justified, Right Justified)	8-Channel TDM
48 kHz	Master and slave	Master and slave
96 kHz	Master and slave	Master and slave
192 kHz	Master and slave	Slave only

The serial input and output control registers allow the user to control clock polarities, clock frequencies, clock types, and data format. In all modes except for the right-justified modes (MSB delayed by 8, 12, or 16 bits), the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but are truncated internally. Proper operation of the right-justified modes requires the LSB to align with the edge of the LRCLK. The default settings of all serial port control registers correspond to 2-channel I²S mode. All register settings apply to both master and slave modes unless otherwise noted.

The function of each multipurpose pin in serial data port mode is shown in Table 65. Pin MP0 to Pin MP5 support digital data input to the ADAU1401A, and Pin MP6 to Pin MP11 handle digital data output from the DSP. The configuration of the serial data input port is set in the serial input control register (see Table 51), and the configuration of the corresponding output port is controlled with the serial output control register (see Table 49). The clocks of the input port function only as slaves, whereas the output port clocks can be set to function as either masters or slaves. The MP4 (INPUT_LRCLK) and MP5 (INPUT_BCLK) pins are used to clock the SDATA_INx (MP0 to MP3) signals, and the MP10 (OUTPUT_LRCLK) and MP11 (OUTPUT_BCLK) pins are used to clock the SDATA_OUTx (MP6 to MP9) signals.

If an external ADC is connected as a slave to the ADAU1401A, use both the input and output port clocks. The MP10 (OUTPUT_LRCLK) and MP11 (OUTPUT_BCLK) pins must be set to master mode and be connected externally to the MP4 (INPUT_LRCLK) and MP5 (INPUT_BCLK) pins, as well as to the external ADC clock input pins. The data is output from the external ADC into the SigmaDSP on the MP0, MP1, MP2, or MP3 (SDATA_INx) pin.

Connections to an external DAC are handled exclusively by the output port pins. The MP10 (OUTPUT_LRCLK) and MP11 (OUTPUT_BCLK) pins can be set to function as either masters or slaves, and the MP6 to MP9 (SDATA_OUTx) pins are used to output data from the SigmaDSP to the external DAC.

Table 66 describes the proper configurations for standard audio data formats.

Table 65. Multipurpose Pin Serial Data Port Functions

Multipurpose Pin	Function
MP0	SDATA_IN0/TDM_IN
MP1	SDATA_IN1
MP2	SDATA_IN2
MP3	SDATA_IN3
MP4	INPUT_LRCLK (slave only)
MP5	INPUT_BCLK (slave only)
MP6	SDATA_OUT0/TDM_OUT
MP7	SDATA_OUT1
MP8	SDATA_OUT2
MP9	SDATA_OUT3
MP10	OUTPUT_LRCLK (master or slave)
MP11	OUTPUT_BCLK (master or slave)

Table 66. Data Format Configurations

Format	LRCLK Polarity	LRCLK Type	BCLK Polarity	MSB Position
I²S (see Figure 32)	Frame begins on falling edge	Clock	Data changes on falling edge	Delayed from LRCLK edge by 1 BCLK
Left-Justified (see Figure 33)	Frame begins on rising edge	Clock	Data changes on falling edge	Aligned with LRCLK edge
Right-Justified (see Figure 34)	Frame begins on rising edge	Clock	Data changes on falling edge	Delayed from LRCLK edge by 8, 12, or 16 BCLKs
TDM with Clock (see Figure 35)	Frame begins on falling edge	Clock	Data changes on falling edge	Delayed from start of word clock by 1 BCLK
TDM with Pulse (see Figure 36)	Frame begins on rising edge	Pulse	Data changes on falling edge	Delayed from start of word clock by 1 BCLK

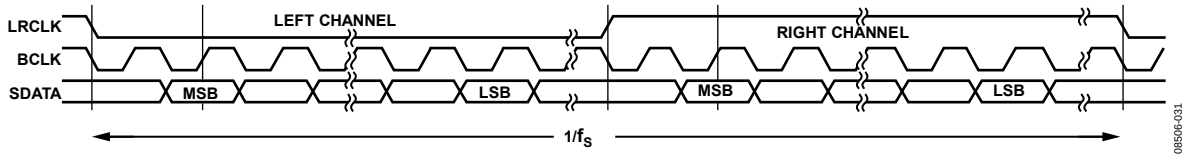

Figure 32. I²S Mode—16 Bits to 24 Bits per Channel

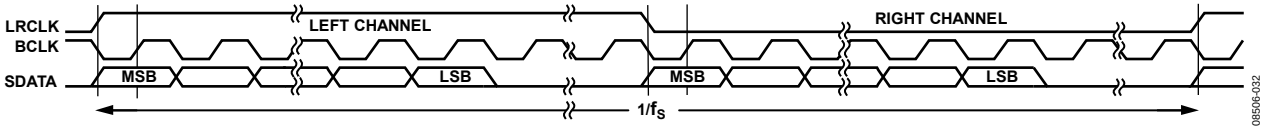

Figure 33. Left-Justified Mode—16 Bits to 24 Bits per Channel

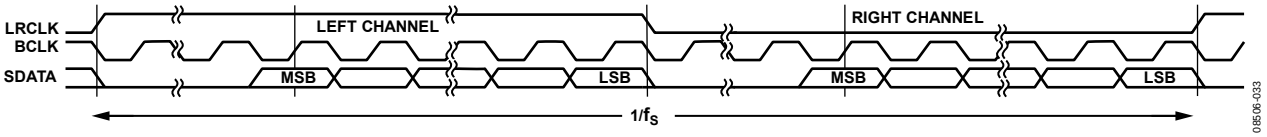

Figure 34. Right-Justified Mode—16 Bits to 24 Bits per Channel

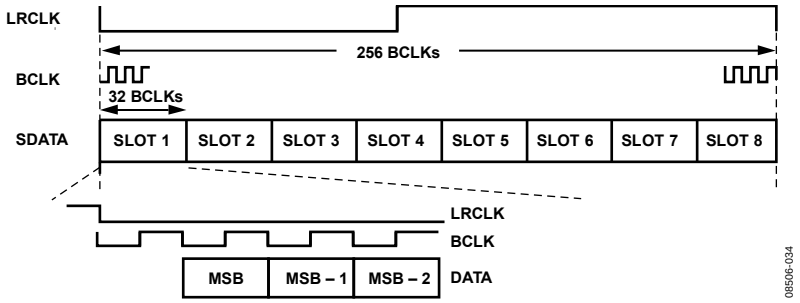

Figure 35. TDM Mode

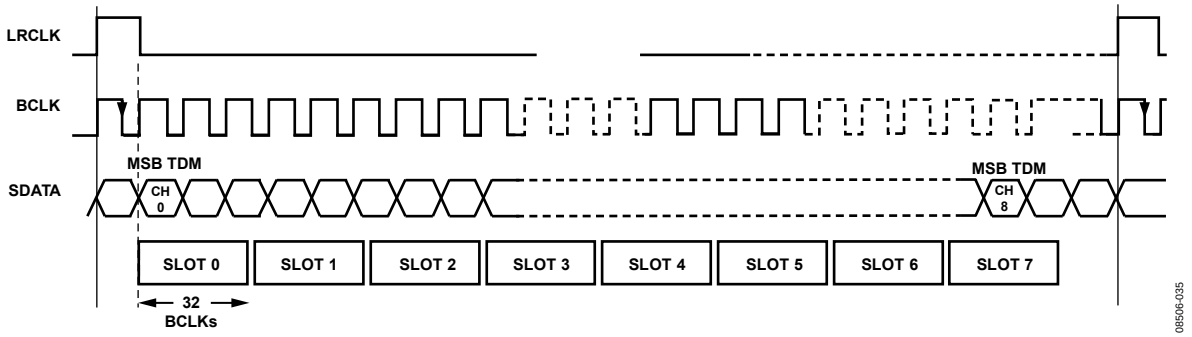

Figure 36. TDM Mode with Pulse Word Clock

LAYOUT RECOMMENDATIONS

PARTS PLACEMENT

The ADC input voltage-to-current resistors and the ADC current set resistor should be placed as close as possible to the 2, 3, and 4 input pins.

All 100 nF bypass capacitors, which are recommended for every analog, digital, and PLL power/ground pair, should be placed as close as possible to the ADAU1401A. The 3.3 V and 1.8 V signals on the board should also each be bypassed with a single bulk capacitor (10 µF to 47 µF).

All traces in the crystal oscillator circuit (see Figure 14) should be kept as short as possible to minimize stray capacitance. In addition, avoid long board traces connected to any of these components because such traces may affect crystal startup and operation.

GROUNDING

A single ground plane should be used in the application layout. Components in an analog signal path should be placed away from digital signals.

TYPICAL APPLICATION SCHEMATICS

SELF-BOOT MODE

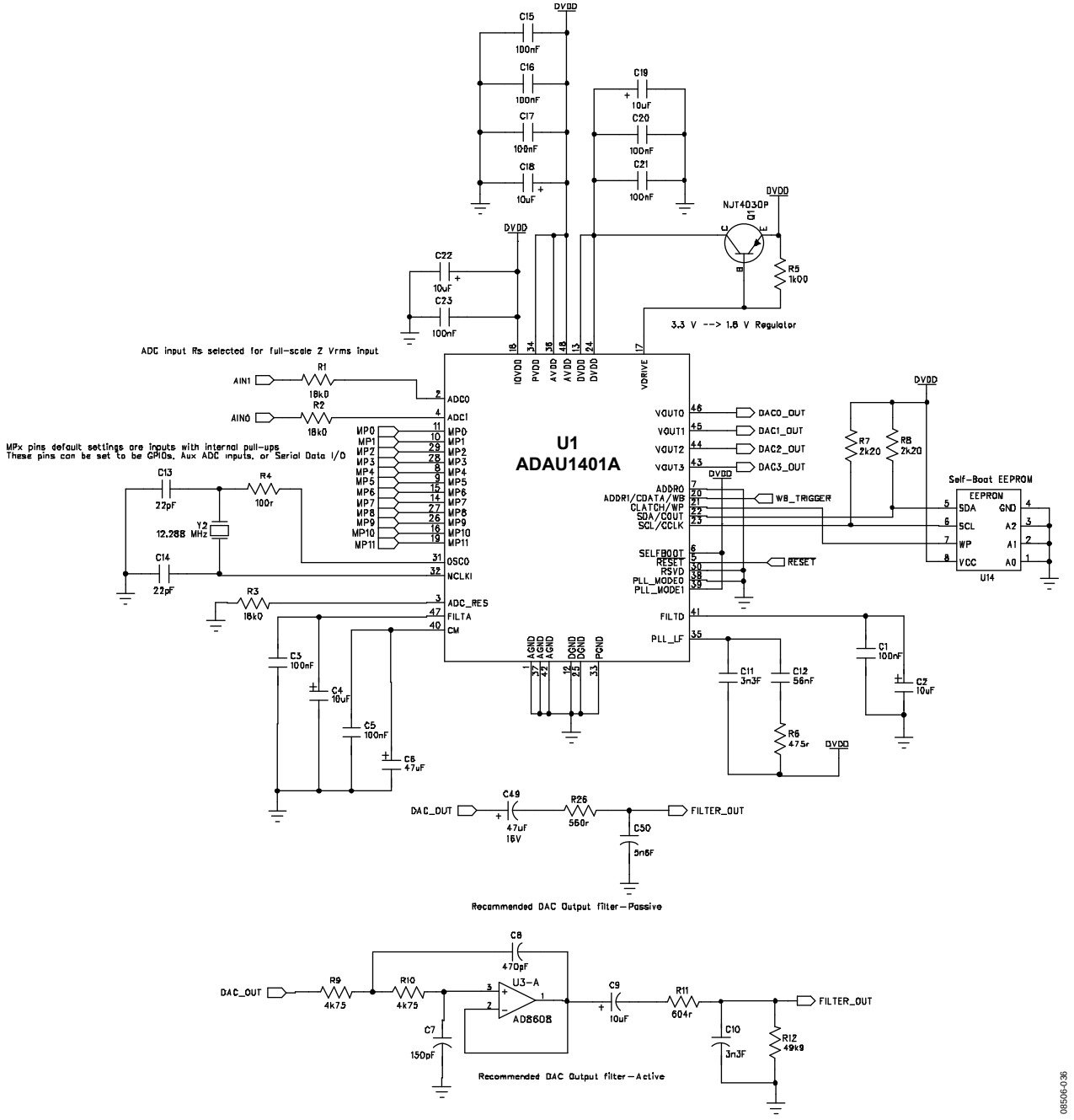

Figure 37. Self-Boot Mode Schematic

I²C CONTROL

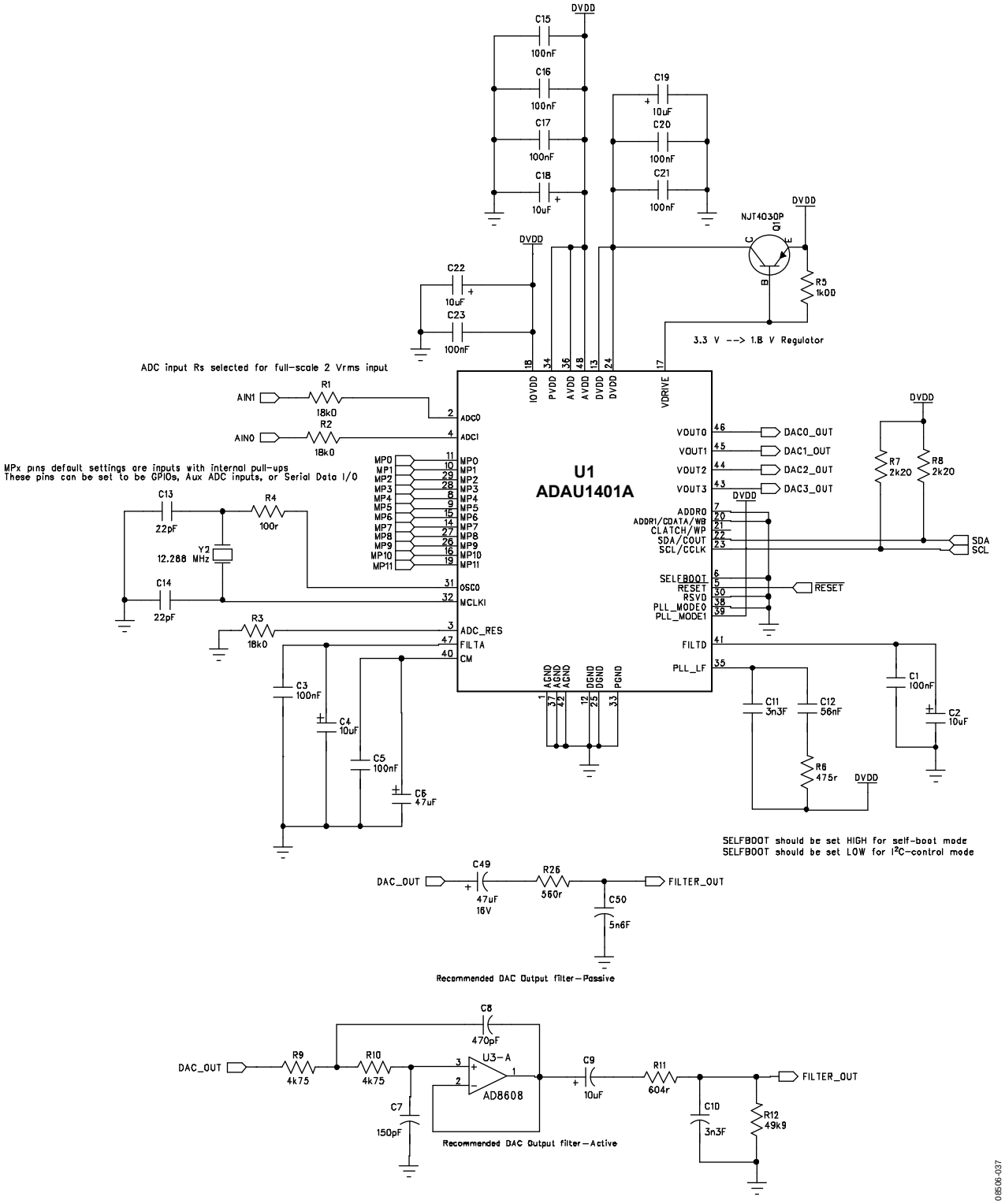

Figure 38. I²C Control Schematic