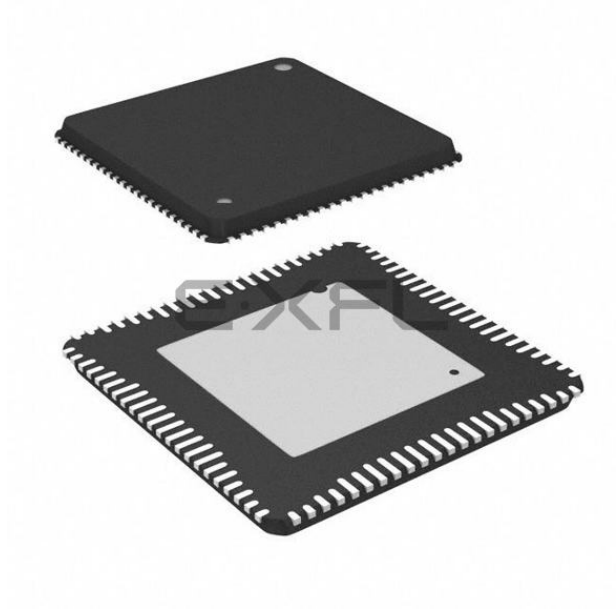

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	294.912MHz
Non-Volatile Memory	ROM (64kB)
On-Chip RAM	192kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad, CSP
Supplier Device Package	88-LFCSP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1463wbcpz300rl

Table 19. Example System Initialization Register Write Sequence[1]

Address	Data	Register/Memory	Description
N/A	N/A	N/A	Toggle SS/ADDR0 three times to enable SPI slave mode, if necessary.
0xF890	0x00, 0x00	SOFT_RESET	Enter soft reset.
0xF890	0x00, 0x01	SOFT_RESET	Exit soft reset.
0xF000	0x00, 0x60	PLL_CTRL0	Set feedback divider to 96 (this is the default power-on setting).
0xF001	0x00, 0x02	PLL_CTRL1	Set PLL input clock divider to 4.
0xF002	0x00, 0x01	PLL_CLK_SRC	Set clock source to PLL clock.
0xF005	0x00, 0x05	MCLK_OUT	Enable MCLK output (12.288 MHz).
0xF003	0x00, 0x01	PLL_ENABLE	Enable PLL.
N/A	N/A	N/A	Wait for PLL lock (see the Power-Up Sequence section); the maximum PLL lock time is 10.666 ms.
0xF050	0x4F, 0xFF	POWER_ENABLE0	Enable power for all major systems except Clock Generator 3 (Clock Generator 3 is rarely used in most systems).
0xF051	0x00, 0x00	POWER_ENABLE1	Disable power for subsystems like PDM microphones, S/PDIF, and the ADC if they are not being used in the system.
0xF899	0x00, 0x00	SECONDPAGE_ENABLE	Toggle the SECONDPAGE_ENABLE to point at host port memory, Page 1.
0xC000	Data generated by SigmaStudio	Program RAM data (Page 1)	Download the lower half of program RAM contents using a block write (data provided by SigmaStudio compiler).
0x0000	Data generated by SigmaStudio	DM0 RAM data (Page 1)	Download the lower half of Data Memory 0 (DM0) using a block write (data provided by SigmaStudio compiler).
0x6000	Data generated by SigmaStudio	DM1 RAM data (Page 1)	Download the lower half of Data Memory 1 (DM1) using a block write (data provided by SigmaStudio compiler).
0xF899	0x00,0x01	SECONDPAGE_ENABLE	Toggle the SECONDPAGE_ENABLE to point at host port memory Page 1.
0xC000	Data generated by SigmaStudio	Program RAM data (Page 2)	Download the upper half of Program RAM contents using a block write (data provided by SigmaStudio compiler).
0x0000	Data generated by SigmaStudio	DM0 RAM data (Page 2)	Download the upper half of DM0 using a block write (data provided by SigmaStudio compiler).
0x6000	Data generated by SigmaStudio	DM1 RAM data (Page 2)	Download the upper half of DM1 using a block write (data provided by SigmaStudio compiler).
0xF404	0x00, 0x00	START_ADDRESS	Set program start address as defined by the SigmaStudio compiler.
0xF401	0x00, 0x02	START_PULSE	Set DSP core start pulse to internally generated pulse.
N/A	N/A	N/A	Configure any other registers that require nondefault values.
0xF402	0x00, 0x00	START_CORE	Stop the core.
0xF402	0x00, 0x01	START_CORE	Start the core.
N/A	N/A	N/A	Wait 50 µs for initialization program to execute.

[1] N/A means not applicable.

Master Clock, PLL, and Clock Generators Registers

An overview of the registers related to the master clock, PLL, and clock generators is listed in Table 22. For a more detailed description, see the PLL Configuration Registers section and the Clock Generator Registers section.

Table 22. Master Clock, PLL, and Clock Generator Registers

Address	Register	Description
0xF000	PLL_CTRL0	PLL feedback divider
0xF001	PLL_CTRL1	PLL prescale divider
0xF002	PLL_CLK_SRC	PLL clock source
0xF003	PLL_ENABLE	PLL enable
0xF004	PLL_LOCK	PLL lock
0xF005	MCLK_OUT	CLKOUT control
0xF006	PLL_WATCHDOG	Analog PLL watchdog control
0xF020	CLK_GEN1_M	Denominator (M) for Clock Generator 1
0xF021	CLK_GEN1_N	Numerator (N) for Clock Generator 1
0xF022	CLK_GEN2_M	Denominator (M) for Clock Generator 2
0xF023	CLK_GEN2_N	Numerator (N) for Clock Generator 2
0xF024	CLK_GEN3_M	Denominator (M) for Clock Generator 3
0xF025	CLK_GEN3_N	Numerator (N) for Clock Generator 3
0xF026	CLK_GEN3_SRC	Input reference for Clock Generator 3
0xF027	CLK_GEN3_LOCK	Lock bit for Clock Generator 3 input reference

POWER SUPPLIES, VOLTAGE REGULATOR, AND HARDWARE RESET

Power Supplies

The ADAU1463/ADAU1467 are supplied by four power supplies: IOVDD, DVDD, AVDD, and PVDD.

- IOVDD (input/output supply) sets the reference voltage for all digital input and output pins. It can be any value ranging from 1.8 V − 5% to 3.3 V + 10%. To use the I²C/SPI control ports or any of the digital input or output pins, the IOVDD supply must be present.
- DVDD (digital supply) powers the DSP core and supporting digital logic circuitry. It must be 1.2 V ± 5%.
- AVDD (analog supply) powers the analog auxiliary ADC circuitry. It must be supplied even if the auxiliary ADCs are not in use.
- PVDD (PLL supply) powers the PLL and acts as a reference for the voltage controlled oscillator (VCO). It must be supplied even if the PLL is not in use.

Table 23. Power Supply Details

Supply	Voltage	Externally Supplied	Description
IOVDD (Input/ Output)	1.8 V − 5% to 3.3 V + 10%	Yes	
DVDD (Digital)	1.2 V ± 5%	Optional	Can be derived from IOVDD using an internal LDO regulator
AVDD (Analog)	3.3 V ± 10%	Yes	
PVDD (PLL)	3.3 V ± 10%	Yes	

Voltage Regulator

The ADAU1463/ADAU1467 include a linear regulator that can generate the 1.2 V supply required by the DSP core and other internal digital circuitry from the I/O supply (IOVDD), which can range from 1.8 V − 5% to 3.3 V + 10%. A simplified block diagram of the internal structure of the regulator is shown in Figure 22.

For proper operation, the linear regulator requires several external components. A PNP bipolar junction transistor acts as an external pass device to bring the higher IOVDD voltage down to the lower DVDD voltage, thus externally dissipating the power of the IC package. Ensure that the transistor is able to dissipate at least 1 W in the worst case. Place a 1 kΩ resistor between the transistor emitter and base to help stabilize the regulator for varying loads. This resistor placement also guarantees that current is always flowing into the VDRIVE pin, even for minimal regulator loads. Figure 21 shows the connection of the external components.

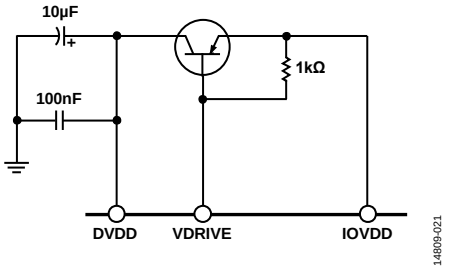


Figure 21. External Components Required for Voltage Regulator Circuit

If an external supply is provided to DVDD, ground the VDRIVE pin. The regulator continues to draw a small amount of current (approximately 100 µA) from the IOVDD supply. Do not use the regulator to provide a voltage supply to external ICs. There are no control registers associated with the regulator.

Note that there is only one set of control registers at Address 0xF000 to Address 0xFBFF. The value of SECONDPAGE_ENABLE has no effect on these registers.

For example,

- A write on the slave port to Address 0x6000 while SECONDPAGE_ENABLE is set to 0 (on Page 1) changes the value of Address 0x0000 in DM1 memory.
- A write on the slave port to Address 0xAFFF while SECONDPAGE_ENABLE is set to 0 (on Page 1) changes the value of Address 0x4FFF in DM1 memory.
- A write on the slave port to Address 0x6000 while SECONDPAGE_ENABLE is set to 1 (on Page 2) changes the value of Address 0x5000 in DM1 memory.
- A write on the slave port to Address 0xAFFF while SECONDPAGE_ENABLE is set to 1 (on Page 2) changes the value of Address 0x9FFF in DM1 memory.

Table 25. Control Port Pin Functions

Pin Name	I²C Slave Mode	SPI Slave Mode
SS/ADDR0	Address 0 (Bit 1 of the address word, input to the ADAU1463/ADAU1467)	Slave select (input to the ADAU1463/ADAU1467)
SCLK/SCL	Clock (input to the ADAU1463/ADAU1467)	Clock (input to the ADAU1463/ADAU1467)
MOSI/ADDR1	Address 1 (Bit 2 of the address word, input to the ADAU1463/ADAU1467)	Data; master out, slave in (input to the ADAU1463/ADAU1467)
MISO/SDA	Data (bidirectional, open-collector)	Data; master in, slave out (output from the ADAU1463/ADAU1467)

Auxiliary Output Mode

The received data on the S/PDIF receiver can be converted to a TDM8 stream, bypass the SigmaDSP core, and be output directly on a serial data output pin. This mode of operation is called auxiliary output mode. Configure this mode using Register 0xF608 (SPDIF_AUX_EN). The TDM8 output from the S/PDIF receiver regroups the recovered data in a TDM like format, as shown in Table 46.

The S/PDIF receiver, when operating in auxiliary output mode, also recovers the embedded BCLK_OUTx and LRCLK_OUTx signals in the S/PDIF stream and outputs them on the corresponding BCLK_OUTx and LRCLK_OUTx pins in master mode when Register 0xF608 (SPDIF_AUX_EN), Bits[3:0] (TDMOUT) are configured to enable auxiliary output mode. The selected BCLK_OUTx signal has a frequency of 256× the recovered sample rate, and the LRCLK_OUTx signal is a 50% duty cycle square wave that has the same frequency as the audio sample rate (see Table 144).

Table 46. S/PDIF Auxiliary Output Mode, TDM8 Data Format

TDM8 Channel	Description of Data Format
0	8 zero bits followed by 24 audio bits, recovered from the left audio channel of the S/PDIF stream
1	28 zero bits followed by the left parity bit, left validity bit, left user data, and left channel status
2	30 zero bits followed by the compression type bit (COMPR_TYPE) (0b0 = AC3, 0b1 = DTS) and the audio type bit (AUDIO_TYPE) (0 = PCM, 1 = compressed)
3	No data
4	8 zero bits followed by 24 audio bits, recovered from the right audio channel of the S/PDIF stream
5	28 zero bits followed by the right parity bit, right validity bit, right user data, and right channel status
6	No data
7	31 zero bits followed by the block start signal

S/PDIF Receiver Inputs to DSP Core

The S/PDIF receiver input must pass through an ASRC to guarantee that it is synchronous to the DSP core. The two channels from the S/PDIF receiver can be selected as the audio source to ASRCs in the routing matrix. When the source is the S/PDIF receiver, the serial input channel that is specified is ignored.

Table 47. S/PDIF Input Mapping to SigmaStudio Channels

Channel in S/PDIF Receiver Data Stream	S/PDIF Input Channels in SigmaStudio
Left	0
Right	1

S/PDIF Audio Outputs from DSP Core to S/PDIF Transmitter

The output signal of the S/PDIF transmitter can come from the DSP core or directly from the S/PDIF receiver. The selection is controlled by Register 0xF1C0 (SPDIFTX_INPUT). When the signal comes from the DSP core, use the S/PDIF output cells in SigmaStudio.

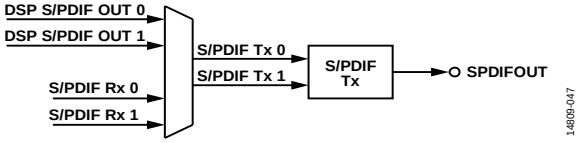


Figure 69. S/PDIF Transmitter Source Selection

Table 48. S/PDIF Output Mapping from SigmaStudio Channels

Channel in S/PDIF Transmitter Data Stream	S/PDIF Output Channel in SigmaStudio
Left	0
Right	1

S/PDIF Interface Registers

An overview of the registers related to the S/PDIF interface is shown in Table 49. For a more detailed description, refer to the S/PDIF Interface Registers section.

MULTIPURPOSE PINS

A total of 25 pins are available for use as GPIOs that are multiplexed with other functions, such as clock inputs/outputs. Because these pins have multiple functions, they are referred to as multipurpose pins, or MPx pins.

Multipurpose pins can be configured in several modes using the MPx_MODE registers:

- Hardware input from pin
- Software input (written via I²C or SPI slave control port)
- Hardware output with internal pull-up resistor
- Hardware output without internal pull-up resistor
- PDM microphone data input
- Flag output from panic manager
- Slave select line for master SPI port

When configured in hardware input mode, a debounce circuit is available to avoid data glitches.

When operating in GPIO mode, the pin status is updated once per sample, which means that the state of a GPIO (MPx pin) cannot change more than once in a sample period.

General-Purpose Inputs to the DSP Core

When a multipurpose pin is configured as a general-purpose input, its value can be used as a control logic signal in the DSP program, which is configured using SigmaStudio. Figure 73 shows the location of the general-purpose input cell within the SigmaStudio toolbox.

The 26 available general-purpose inputs in SigmaStudio map to the corresponding 26 multipurpose pins; however, their data is valid only if the corresponding multipurpose pin is configured as an input using the MPx_MODE registers. Figure 75 shows all of the general-purpose inputs as they appear in the SigmaStudio signal flow.

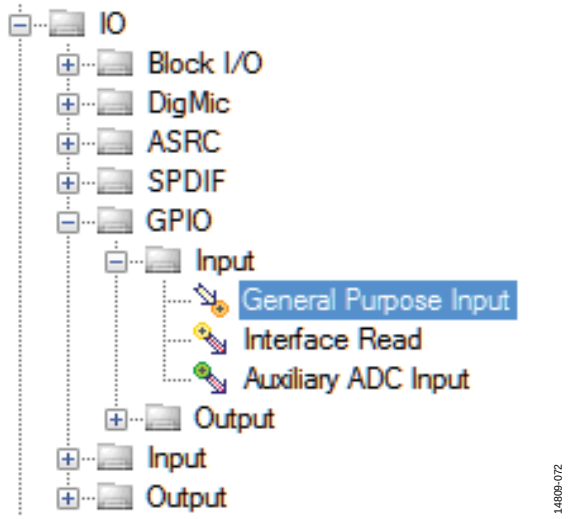


Figure 73. General-Purpose Input in the SigmaStudio Toolbox

General-Purpose Outputs from the DSP Core

When a multipurpose pin is configured as a general-purpose output, a Boolean value is output from the DSP program to the corresponding multipurpose pin. Figure 74 shows the location of the general-purpose input cell within the SigmaStudio toolbox.

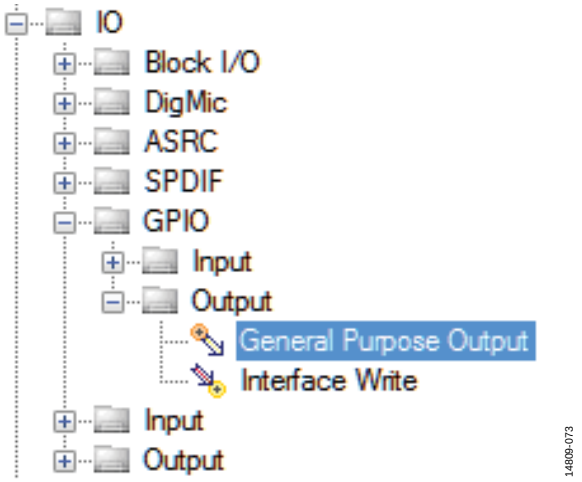


Figure 74. General-Purpose Output in the SigmaStudio Toolbox

The four multipliers are 64-bit double precision, capable of multiplying an 8.56 format number by an 8.24 number. The multiply accumulators consist of 16 registers, with a depth of 80 bits. The core can access RAM with a load/store width of 256 bits (eight 32-bit words per frame). The two ALUs have an 80-bit width and operate on numbers in 24.56 format. The 24.56-bit format provides more than 42 dB of headroom.

It is possible to create combinations of time domain and frequency domain processing, using block and sample frame interrupts. Sixteen data address generator (DAG) registers are available, and circular buffer addressing is possible.

Many of the signal processing functions are coded using full, 64-bit, double precision arithmetic. The serial port input and output word lengths are 24 bits; however, eight extra headroom bits are used in the processor to allow internal gains of up to 48 dB without clipping. Additional gains can be achieved by initially scaling down the input signal in the DSP signal flow.

Numeric Formats

DSP systems commonly use a standard numeric format. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The same numeric format is used for both the parameter and data values.

A digital clipper circuit is used within the DSP core before outputting to the serial port outputs, ASRCs, and S/PDIF. This circuit clips the top seven bits (and the least significant bit) of the signal to produce a 24-bit output with a range of +1.0 (minus 1 LSB) to −1.0. Figure 79 shows the maximum signal levels at each point in the data flow in both binary and decibel levels.

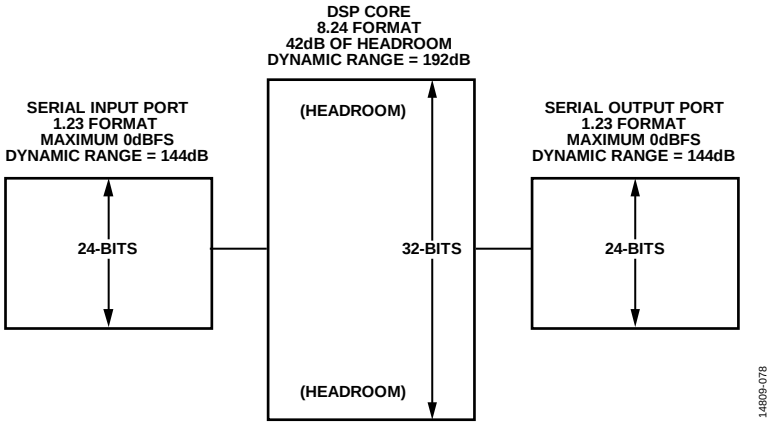


Figure 79. Signal Range for 1.23 Format (Serial Ports, ASRCs) and 8.24 Format (DSP Core)

Numerical Format: 8.24

The linear range for the 8.24 format is −128.0 to (+128.0 − 1 LSB). The dynamic range (ratio of the largest possible signal level to the smallest possible nonzero signal level) is 192 dB.

The following is an example of this numerical format:

```
0b 1000 0000 0000 0000 0000 0000 0000 0000 = 0x80000000 = −128.0
0b 1110 0000 0000 0000 0000 0000 0000 0000 = 0xE0000000 = −32.0
0b 1111 1000 0000 0000 0000 0000 0000 0000 = 0xF8000000 = −8.0
0b 1111 1110 0000 0000 0000 0000 0000 0000 = 0xFE000000 = −2
0b 1111 1111 0000 0000 0000 0000 0000 0000 = 0xFF000000 = −1
0b 1111 1111 1000 0000 0000 0000 0000 0000 = 0xFF800000 = −0.5
0b 1111 1111 1110 0110 0110 0110 0110 0110 = 0xFFE66666 = −0.1
0b 1111 1111 1111 1111 1111 1111 1111 1111 = 0xFFFFFFFF = −0.00000005 (1 LSB below 0.0)
0b 0000 0000 0000 0000 0000 0000 0000 0000 = 0x00000000 = 0.0
0b 0000 0000 0000 0000 0000 0000 0000 0001 = 0x00000001 = 0.00000005 (1 LSB above 0.0)
0b 0000 0000 0001 1001 1001 1001 1001 1001 = 0x00199999 = 0.1
0b 0000 0000 0100 0000 0000 0000 0000 0000 = 0x00400000 = 0.25
0b 0000 0000 1000 0000 0000 0000 0000 0000 = 0x00800000 = 0.5
0b 0000 0001 0000 0000 0000 0000 0000 0000 = 0x01000000 = 1.0
0b 0000 0010 0000 0000 0000 0000 0000 0000 = 0x02000000 = 2.0
0b 0111 1111 1111 1111 1111 1111 1111 1111 = 0x7FFFFFFF = 127.99999994 (1 LSB below 128.0)
```

Numerical Format: 32.0

The 32.0 format is used for logic signals in the DSP program flow that are integers. The linear range is −2,147,483,648 to +2,147,483,647. The dynamic range (ratio of the largest possible signal level to the smallest possible nonzero signal level) is 192 dB.

The following is an example of this numerical format:

```
0b 1000 0000 0000 0000 0000 0000 0000 0000 = 0x80000000 = −2147483648
0b 1000 0000 0000 0000 0000 0000 0000 0001 = 0x80000001 = −2147483647
0b 1000 0000 0000 0000 0000 0000 0000 0010 = 0x80000002 = −2147483646
0b 1100 0000 0000 0000 0000 0000 0000 0000 = 0xC0000000 = −1073741824
0b 1110 0000 0000 0000 0000 0000 0000 0000 = 0xE0000000 = −536870912
0b 1111 1111 1111 1111 1111 1111 1111 1100 = 0xFFFFFFFC = −4
0b 1111 1111 1111 1111 1111 1111 1111 1110 = 0xFFFFFFFE = −2
0b 1111 1111 1111 1111 1111 1111 1111 1111 = 0xFFFFFFFF = −1
0b 0000 0000 0000 0000 0000 0000 0000 0000 = 0x00000000 = 0
0b 0000 0000 0000 0000 0000 0000 0000 0001 = 0x00000001 = 1
0b 0000 0000 0000 0000 0000 0000 0000 0010 = 0x00000002 = 2
0b 0000 0000 0000 0000 0000 0000 0000 0011 = 0x00000003 = 3
0b 0000 0000 0000 0000 0000 0000 0000 0100 = 0x00000004 = 4
0b 0111 1111 1111 1111 1111 1111 1111 1110 = 0x7FFFFFFE = 2147483646
0b 0111 1111 1111 1111 1111 1111 1111 1111 = 0x7FFFFFFF = 2147483647
```

GLOBAL RAM AND CONTROL REGISTER MAP

The complete set of addresses accessible via the slave I²C/SPI control port is described in this section. The addresses are divided into two main parts: memory and registers.

RANDOM ACCESS MEMORY

The ADAU1467 has 1.28 Mb of data memory (40 kWords storing 32-bit data). The ADAU1463 has 512 kb of data (16 kWords storing 32-bit data).

The ADAU1463/ADAU1467 have 8 kWords of program memory. Program memory consists of 32-bit words. Op codes for the DSP core are either 32 bits or 64 bits; therefore, program instructions can take up one or two addresses in memory. The program memory has parity bit protection. The panic manager flags parity errors when they are detected.

Program memory can only be written or read when the core is stopped. The program memory is hardware protected so that it cannot be accidentally overwritten or corrupted at run time.

The DSP core is able to access directly all memory and registers.

Data memory acts as a storage area for both audio data and signal processing parameters, such as filter coefficients. The data memory has parity bit protection. The panic manager flags parity errors when they are detected. Modulo memory addressing is used in several audio processing algorithms. The boundaries between the fixed and rotating memories are set in SigmaStudio by the compiler, and they require no action on the part of the user.

Data and parameters assignment to the different memory spaces are handled in software. The modulo boundary locations are flexible.

A ROM table (of over 7 kWords), containing a set of commonly used constants, can be accessed by the DSP core. This memory increases the efficiency of audio processing algorithm development. The table includes information such as trigonometric tables, including sine, cosine, tangent, and hyperbolic tangent, twiddle factors for frequency domain processing, real mathematical constants, such as pi and factors of 2, and complex constants. The ROM table is not accessible from the I²C or SPI slave control port.

All memory addresses store 32 bits (4 bytes) of data. The memory spaces for the ADAU1467 are defined in Table 58. The memory spaces for the ADAU1463 are defined in Table 59.

Table 58. ADAU1467 Memory Map

Address Range	Length	Memory	Data-Word Size
0x0000 to 0x4FFF	20,480 words	DM0 (Data Memory 0)—lower (Page 1)	32 bits
0x0000 to 0x4FFF	20,480 words	DM0 (Data Memory 0)—upper (Page 2)	32 bits
0x6000 to 0xAFFF	20,480 words	DM1 (Data Memory 1)—lower (Page 1)	32 bits
0x6000 to 0xAFFF	20,480 words	DM1 (Data Memory 1)—upper (Page 2)	32 bits
0xC000 to 0xEFFF	12,288 words	Program memory—lower (Page 1)	32 bits
0xC000 to 0xEFFF	12,288 words	Program memory—upper (Page 2)	32 bits

Table 59. ADAU1463 Memory Map

Address Range	Length	Memory	Data-Word Size
0x0000 to 0x2FFF	12,288 words	DM0 (Data Memory 0)—lower (Page 1)	32 bits
0x0000 to 0x2FFF	12,288 words	DM0 (Data Memory 0)—upper (Page 2)	32 bits
0x6000 to 0x8FFF	12,288 words	DM1 (Data Memory 1)—lower (Page 1)	32 bits
0x6000 to 0x8FFF	12,288 words	DM1 (Data Memory 1)—lower (Page 2)	32 bits
0xC000 to 0xDFFF	8192 words	Program memory—lower (Page 1)	32 bits
0xC000 to 0xDFFF	8192 words	Program memory—lower (Page 2)	32 bits

CONTROL REGISTERS

All control registers store 16 bits (two bytes) of data. The register map is defined in Table 60.

Table 60. Control Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0xF000	PLL_CTRL0	[15:8]	RESERVED								0x0060	RW
		[7:0]	RESERVED	PLL_FBDIVIDER								
0xF001	PLL_CTRL1	[15:8]	RESERVED								0x0000	RW
		[7:0]	RESERVED						PLL_DIV			
0xF002	PLL_CLK_SRC	[15:8]	RESERVED								0x0000	RW
		[7:0]	RESERVED							CLKSRC		
0xF003	PLL_ENABLE	[15:8]	RESERVED								0x0000	RW
		[7:0]	RESERVED							PLL_ENABLE		
0xF004	PLL_LOCK	[15:8]	RESERVED								0x0000	R
		[7:0]	RESERVED							PLL_LOCK		
0xF005	MCLK_OUT	[15:8]	RESERVED								0x0000	R
		[7:0]	RESERVED					CLKOUT_RATE		CLKOUT_ENABLE		
0xF006	PLL_WATCHDOG	[15:8]	RESERVED								0x0001	R
		[7:0]	RESERVED							PLL_WATCHDOG		
0xF020	CLK_GEN1_M	[15:8]	RESERVED							CLOCKGEN1_M[8]	0x0006	RW
		[7:0]	CLOCKGEN1_M[7:0]									
0xF021	CLK_GEN1_N	[15:8]	RESERVED							CLOCKGEN1_N[8]	0x0001	RW
		[7:0]	CLOCKGEN1_N[7:0]									
0xF022	CLK_GEN2_M	[15:8]	RESERVED							CLOCKGEN2_M[8]	0x0009	RW
		[7:0]	CLOCKGEN2_M[7:0]									
0xF023	CLK_GEN2_N	[15:8]	RESERVED							CLOCKGEN2_N[8]	0x0001	RW
		[7:0]	CLOCKGEN2_N[7:0]									
0xF024	CLK_GEN3_M	[15:8]	CLOCKGEN3_M[15:8]								0x0000	RW
		[7:0]	CLOCKGEN3_M[7:0]									
0xF025	CLK_GEN3_N	[15:8]	CLOCKGEN3_N[15:8]								0x0000	RW
		[7:0]	CLOCKGEN3_N[7:0]									
0xF026	CLK_GEN3_SRC	[15:8]	RESERVED								0x000E	RW
		[7:0]	RESERVED			CLK_GEN3_SRC	FREF_PIN					
0xF027	CLK_GEN3_LOCK	[15:8]	RESERVED								0x0000	R
		[7:0]	RESERVED							GEN3_LOCK		
0xF050	POWER_ENABLE0	[15:8]	RESERVED			CLK_GEN3_PWR	CLK_GEN2_PWR	CLK_GEN1_PWR	ASRCBANK1_PWR	ASRCBANK0_PWR	0x0000	RW
		[7:0]	SOUT3_PWR	SOUT2_PWR	SOUT1_PWR	SOUT0_PWR	SIN3_PWR	SIN2_PWR	SIN1_PWR	SIN0_PWR		
0xF051	POWER_ENABLE1	[15:8]	RESERVED								0x0000	RW
		[7:0]	RESERVED			PDM1_PWR	PDM0_PWR	TX_PWR	RX_PWR	ADC_PWR		
0xF100 to 0xF107	ASRC_INPUTx	[15:8]	RESERVED								0x0000	RW
		[7:0]	ASRC_SIN_CHANNEL					ASRC_SOURCE				
0xF140 to 0xF147	ASRC_OUT_RATEx	[15:8]	RESERVED								0x0000	RW
		[7:0]	RESERVED				ASRC_RATE					
0xF180 to 0xF197	SOUT_SOURCEx	[15:8]	RESERVED								0x0000	RW
		[7:0]	RESERVED		SOUT_ASRC_SELECT			SOUT_SOURCE				
0xF1C0	SPDIFTX_INPUT	[15:8]	RESERVED								0x0000	RW
		[7:0]	RESERVED						SPDIFTX_SOURCE			
0xF200 to 0xF21C	SERIAL_BYTE_x_0	[15:8]	LRCLK_SRC			BCLK_SRC			LRCLK_MODE	LRCLK_POL	0x0000	RW
		[7:0]	BCLK_POL	WORD_LEN		DATA_FMT		TDM_MODE				

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0xF462	PROG_CNTR_CLEAR	[15:8]	RESERVED								0x0000	RW
		[7:0]	RESERVED							PROG_CNTR_CLEAR		
0xF463	PROG_CNTR_LENGTH0	[15:8]	RESERVED								0x0000	R
		[7:0]	PROG_LENGTH_MSB									
0xF464	PROG_CNTR_LENGTH1	[15:8]	PROG_LENGTH_LSB[15:8]								0x0000	R
		[7:0]	PROG_LENGTH_LSB[7:0]									
0xF465	PROG_CNTR_MAXLENGTH0	[15:8]	RESERVED								0x0000	R
		[7:0]	PROG_MAXLENGTH_MSB									
0xF466	PROG_CNTR_MAXLENGTH1	[15:8]	PROG_MAXLENGTH_LSB[15:8]								0x0000	R
		[7:0]	PROG_MAXLENGTH_LSB[7:0]									
0xF467	PANIC_PARITY_MASK1	[15:8]	RESERVED			DM0_BANK1_SUBBANK4_MASK	DM0_BANK1_SUBBANK3_MASK	DM0_BANK1_SUBBANK2_MASK	DM0_BANK1_SUBBANK1_MASK	DM0_BANK1_SUBBANK0_MASK	0x0000	RW
		[7:0]	RESERVED			DM0_BANK0_SUBBANK4_MASK	DM0_BANK0_SUBBANK3_MASK	DM0_BANK0_SUBBANK2_MASK	DM0_BANK0_SUBBANK1_MASK	DM0_BANK0_SUBBANK0_MASK		
0xF468	PANIC_PARITY_MASK2	[15:8]	RESERVED			DM0_BANK3_SUBBANK4_MASK	DM0_BANK3_SUBBANK3_MASK	DM0_BANK3_SUBBANK2_MASK	DM0_BANK3_SUBBANK1_MASK	DM0_BANK3_SUBBANK0_MASK	0x0000	RW
		[7:0]	RESERVED			DM0_BANK2_SUBBANK4_MASK	DM0_BANK2_SUBBANK3_MASK	DM0_BANK2_SUBBANK2_MASK	DM0_BANK2_SUBBANK1_MASK	DM0_BANK2_SUBBANK0_MASK		
0xF469	PANIC_PARITY_MASK3	[15:8]	RESERVED			DM1_BANK1_SUBBANK4_MASK	DM1_BANK1_SUBBANK3_MASK	DM1_BANK1_SUBBANK2_MASK	DM1_BANK1_SUBBANK1_MASK	DM1_BANK1_SUBBANK0_MASK	0x0000	RW
		[7:0]	RESERVED			DM1_BANK0_SUBBANK4_MASK	DM1_BANK0_SUBBANK3_MASK	DM1_BANK0_SUBBANK2_MASK	DM1_BANK0_SUBBANK1_MASK	DM1_BANK0_SUBBANK0_MASK		
0xF46A	PANIC_PARITY_MASK4	[15:8]	RESERVED			DM1_BANK3_SUBBANK4_MASK	DM1_BANK3_SUBBANK3_MASK	DM1_BANK3_SUBBANK2_MASK	DM1_BANK3_SUBBANK1_MASK	DM1_BANK3_SUBBANK0_MASK	0x0000	RW
		[7:0]	RESERVED			DM1_BANK2_SUBBANK4_MASK	DM1_BANK2_SUBBANK3_MASK	DM1_BANK2_SUBBANK2_MASK	DM1_BANK2_SUBBANK1_MASK	DM1_BANK2_SUBBANK0_MASK		
0xF46B	PANIC_PARITY_MASK5	[15:8]	RESERVED		PM_BANK1_SUBBANK5_MASK	PM_BANK1_SUBBANK4_MASK	PM_BANK1_SUBBANK3_MASK	PM_BANK1_SUBBANK2_MASK	PM_BANK1_SUBBANK1_MASK	PM_BANK1_SUBBANK0_MASK	0x0000	RW
		[7:0]	RESERVED		PM_BANK0_SUBBANK5_MASK	PM_BANK0_SUBBANK4_MASK	PM_BANK0_SUBBANK3_MASK	PM_BANK0_SUBBANK2_MASK	PM_BANK0_SUBBANK1_MASK	PM_BANK0_SUBBANK0_MASK		
0xF46C	PANIC_CODE1	[15:8]	RESERVED			ERR_DM0B1SB4	ERR_DM0B1SB3	ERR_DM0B1SB2	ERR_DM0B1SB1	ERR_DM0B1SB0	0x0000	R
		[7:0]	RESERVED			ERR_DM0B0SB4	ERR_DM0B0SB3	ERR_DM0B0SB2	ERR_DM0B0SB1	ERR_DM0B0SB0		
0xF46D	PANIC_CODE2	[15:8]	RESERVED			ERR_DM0B3SB4	ERR_DM0B3SB3	ERR_DM0B3SB2	ERR_DM0B3SB1	ERR_DM0B3SB0	0x0000	R
		[7:0]	RESERVED			ERR_DM0B2SB4	ERR_DM0B2SB3	ERR_DM0B2SB2	ERR_DM0B2SB1	ERR_DM0B2SB0		
0xF46E	PANIC_CODE3	[15:8]	RESERVED			ERR_DM1B1SB4	ERR_DM1B1SB3	ERR_DM1B1SB2	ERR_DM1B1SB1	ERR_DM1B1SB0	0x0000	R
		[7:0]	RESERVED			ERR_DM1B0SB4	ERR_DM1B0SB3	ERR_DM1B0SB2	ERR_DM1B0SB1	ERR_DM1B0SB0		
0xF46F	PANIC_CODE4	[15:8]	RESERVED			ERR_DM1B3SB4	ERR_DM1B3SB3	ERR_DM1B3SB2	ERR_DM1B3SB1	ERR_DM1B3SB0	0x0000	R
		[7:0]	RESERVED			ERR_DM1B2SB4	ERR_DM1B2SB3	ERR_DM1B2SB2	ERR_DM1B2SB1	ERR_DM1B2SB0		
0xF470	PANIC_CODE5	[15:8]	RESERVED		ERR_PM_B1SB5	ERR_PM_B1SB4	ERR_PM_B1SB3	ERR_PM_B1SB2	ERR_PM_B1SB1	ERR_PM_B1SB0	0x0000	R
		[7:0]	RESERVED		ERR_PM_B0SB5	ERR_PM_B0SB4	ERR_PM_B0SB3	ERR_PM_B0SB2	ERR_PM_B0SB1	ERR_PM_B0SB0		
0xF510 to 0xF51D	MPx_MODE	[15:8]	RESERVED					SS_SELECT			0x0000	RW
		[7:0]	DEBOUNCE_VALUE			MP_MODE				MP_ENABLE		
0xF520 to 0xF52D	MPx_WRITE	[15:8]	RESERVED								0x0000	RW
		[7:0]	RESERVED							MP_REG_WRITE		
0xF530 to 0xF53D	MPx_READ	[15:8]	RESERVED								0x0000	R
		[7:0]	RESERVED							MP_REG_READ		

Table 74. Bit Descriptions for CLK_GEN3_SRC

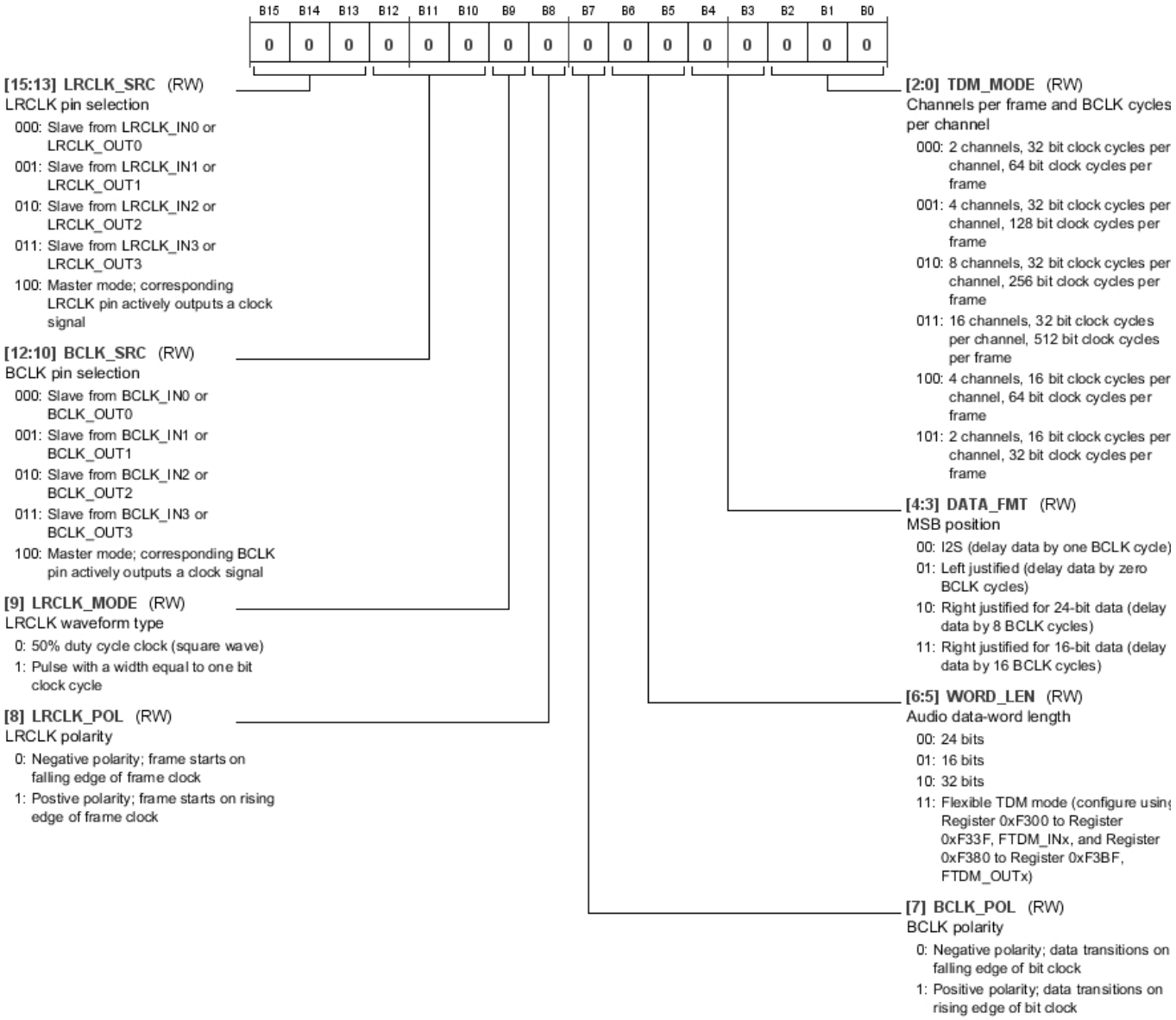
Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	CLK_GEN3_SRC		Reference source for Clock Generator 3. This bit selects the reference of Clock Generator 3. If set to use an external reference clock, Bits[3:0] define the source pin. Otherwise, the PLL output is used as the reference clock. When an external reference clock is used for Clock Generator 3, the resulting base output frequency of Clock Generator 3 is the frequency of the input reference clock multiplied by the Clock Generator 3 numerator, divided by 1024. For example: if Bit 4 (CLK_GEN3_SRC) = 0b1 (an external reference clock is used); Bits[3:0] (FREF_PIN) = 0b1110 (the input signal of the S/PDIF receiver is used as the reference source); the sample rate of the S/PDIF input signal = 48 kHz; and the numerator of Clock Generator 3 = 2048; the resulting base output sample rate of Clock Generator 3 is 48 kHz × 2048/1024 = 96 kHz.	0x0	RW
		0	Reference signal provided by PLL output; multiply the frequency of that signal by N and divide it by M.		
		1	Reference signal provided by the signal input to the hardware pin defined by Bits[3:0] (FREF_PIN); multiply the frequency of that signal by N (and then divide by 1024) to get the resulting sample rate. M is ignored.		
[3:0]	FREF_PIN		Input reference for Clock Generator 3. If Clock Generator 3 is set up to lock to an external reference clock (Bit 4 (CLK_GEN3_SRC) = 0b1), these bits allow the user to specify which pin is receiving the reference clock. The signal input to the corresponding pin must be a 50% duty cycle square wave clock representing the reference sample rate.	0xE	RW
		0000	Input reference source is SS_M/MP0.		
		0001	Input reference source is MOSI_M/MP1.		
		0010	Input reference source is SCL_M/SCLK_M/MP2.		
		0011	Input reference source is SDA_M/MISO_M/MP3.		
		0100	Input reference source is LRCLK_OUT0/MP4.		
		0101	Input reference source is LRCLK_OUT1/MP5.		
		0110	Input reference source is MP6.		
		0111	Input reference source is MP7.		
		1000	Input reference source is LRCLK_OUT2/MP8.		
		1001	Input reference source is LRCLK_OUT3/MP9.		
		1010	Input reference source is LRCLK_IN0/MP10.		
		1011	Input reference source is LRCLK_IN1/MP11.		
		1100	Input reference source is LRCLK_IN2/MP12.		
		1101	Input reference source is LRCLK_IN3/MP13.		
		1110	Input reference source is S/PDIF receiver (recovered frame clock).		

SERIAL PORT CONFIGURATION REGISTERS

Serial Port Control 0 Register

Address: 0xF200 to 0xF21C (Increments of 0x4), Reset: 0x0000, Name: SERIAL_BYTE_x_0

These eight registers configure several settings for the corresponding serial input and serial output ports. Channel count, MSB position, data-word length, clock polarity, clock sources, and clock type are configured using these registers. On the input side, Register 0xF200 (SERIAL_BYTE_0_0) corresponds to SDATA_IN0; Register 0xF204 (SERIAL_BYTE_1_0) corresponds to SDATA_IN1; Register 0xF208 (SERIAL_BYTE_2_0) corresponds to SDATA_IN2; and Register 0xF20C (SERIAL_BYTE_3_0) corresponds to SDATA_IN3. On the output side, Register 0xF210 (SERIAL_BYTE_4_0) corresponds to SDATA_OUT0; Register 0xF214 (SERIAL_BYTE_5_0) corresponds to SDATA_OUT1; Register 0xF218 (SERIAL_BYTE_6_0) corresponds to SDATA_OUT2; and Register 0xF21C (SERIAL_BYTE_7_0) corresponds to SDATA_OUT3.



Panic Mask 1 Register

Address: 0xF424, Reset: 0x0000, Name: PANIC_WD_MASK

The panic manager checks and reports watchdog errors. Register 0xF424 (PANIC_WD_MASK) allows the user to configure whether watchdog errors are reported to the panic manager or ignored.

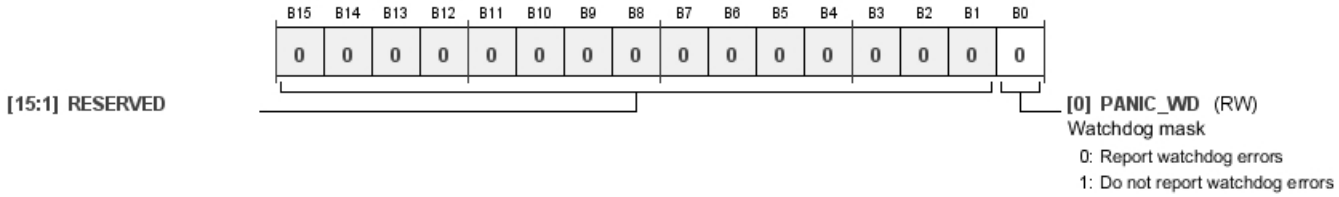


Table 98. Bit Descriptions for PANIC_WD_MASK

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	PANIC_WD		Watchdog mask.	0x0	RW
		0	Report watchdog errors.		
		1	Do not report watchdog errors.		

Panic Mask 2 Register

Address: 0xF425, Reset: 0x0000, Name: PANIC_STACK_MASK

The panic manager checks and reports stack errors. Register 0xF425 (PANIC_STACK_MASK) allows the user to configure whether stack errors are reported to the panic manager or ignored.

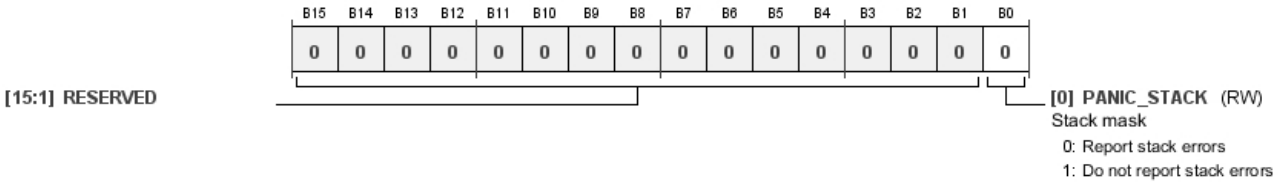


Table 99. Bit Descriptions for PANIC_STACK_MASK

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	PANIC_STACK		Stack mask.	0x0	RW
		0	Report stack errors.		
		1	Do not report stack errors.		

Program Counter Length, Bits[23:16] Register

Address: 0xF463, Reset: 0x0000, Name: PROG_CNTR_LENGTH0

This register, in combination with Register 0xF464 (PROG_CNTR_LENGTH1), keeps track of the peak value reached by the program counter during the last audio frame or block. It can be cleared using Register 0xF462 (PROG_CNTR_CLEAR).

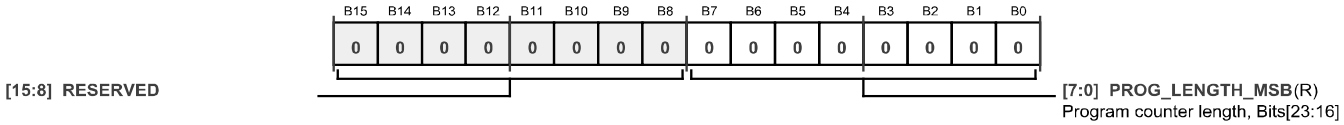


Table 111. Bit Descriptions for PROG_CNTR_LENGTH0

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x0	RW
[7:0]	PROG_LENGTH_MSB		Program counter length, Bits[23:16]	0x00	R

Program Counter Length, Bits[15:0] Register

Address: 0xF464, Reset: 0x0000, Name: PROG_CNTR_LENGTH1

This register, in combination with Register 0xF463 (PROG_CNTR_LENGTH0), keeps track of the peak value reached by the program counter during the last audio frame or block. It can be cleared using Register 0xF462 (PROG_CNTR_CLEAR).

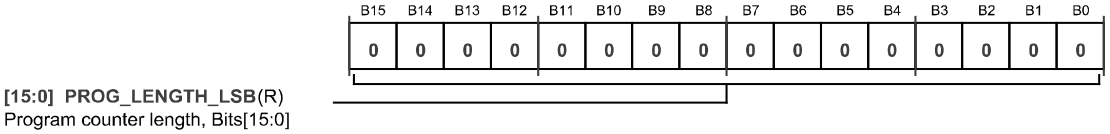


Table 112. Bit Descriptions for PROG_CNTR_LENGTH1

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	PROG_LENGTH_LSB		Program counter length, Bits[15:0]	0x0000	R

Program Counter Maximum Length, Bits[23:16] Register

Address: 0xF465, Reset: 0x0000, Name: PROG_CNTR_MAXLENGTH0

This register, in combination with Register 0xF466 (PROG_CNTR_MAXLENGTH1), keeps track of the highest peak value reached by the program counter since the DSP core started. It can be cleared using Register 0xF462 (PROG_CNTR_CLEAR).

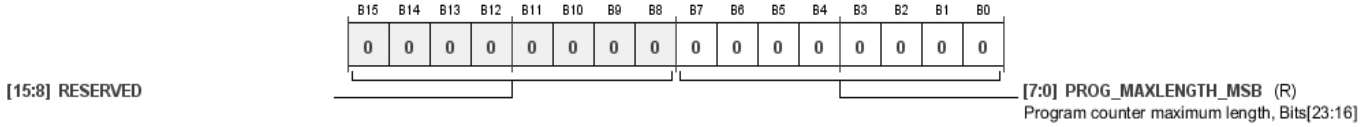


Table 113. Bit Descriptions for PROG_CNTR_MAXLENGTH0

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x0	RW
[7:0]	PROG_MAXLENGTH_MSB		Program counter maximum length, Bits[23:16]	0x00	R

Bits	Bit Name	Settings	Description	Reset	Access
9	ASRC_RAMP1		ASRC 7 to ASRC 4 mute disable. ASRC 7 to ASRC 4 (Channel 15 to Channel 8) are defined as ASRC Block 1. This bit enables or disables mute ramping for all ASRCs in Block 1. If this bit is 0b1, Bit 7 (ASRC7M), Bit 6 (ASRC6M), Bit 5 (ASRC5M), and Bit 4 (ASRC4M) are ignored, and the outputs of ASRC 7 to ASRC 4 are active at all times.	0x0	RW
		0	Enabled.		
		1	Disabled; ASRC 7 to ASRC 4 never mute automatically and cannot be muted manually.		
8	ASRC_RAMP0		ASRC 3 to ASRC 0 mute disable. ASRC 3 to ASRC 0 (Channel 7 to Channel 0) are defined as ASRC Block 0. This bit enables or disables mute ramping for all ASRCs in Block 0. If this bit is 0b1, Bit 3 (ASRC3M), Bit 2 (ASRC2M), Bit 1 (ASRC1M), and Bit 0 (ASRC0M) are ignored, and the outputs of ASRC 3 to ASRC 0 are active at all times.	0x0	RW
		0	Enabled.		
		1	Disabled; ASRC 3 to ASRC 0 never mute automatically and cannot be muted manually.		
7	ASRC7M		ASRC 7 manual mute.	0x0	RW
		0	Not muted.		
		1	Muted.		
6	ASRC6M		ASRC 6 manual mute.	0x0	RW
		0	Not muted.		
		1	Muted.		
5	ASRC5M		ASRC 5 manual mute.	0x0	RW
		0	Not muted.		
		1	Muted.		
4	ASRC4M		ASRC 4 manual mute.	0x0	RW
		0	Not muted.		
		1	Muted.		
3	ASRC3M		ASRC 3 manual mute.	0x0	RW
		0	Not muted.		
		1	Muted.		
2	ASRC2M		ASRC 2 manual mute.	0x0	RW
		0	Not muted.		
		1	Muted.		
1	ASRC1M		ASRC 1 manual mute.	0x0	RW
		0	Not muted.		
		1	Muted.		
0	ASRC0M		ASRC 0 manual mute.	0x0	RW
		0	Not muted.		
		1	Muted.		

S/PDIF Receiver Loss of Lock Detection Register

Address: 0xF605, Reset: 0x0000, Name: SPDIF_LOSS_OF_LOCK

This bit monitors the S/PDIF lock status and checks to see if the lock is lost during operation of the S/PDIF receiver on the ADAU1467 and ADAU1463. This condition can arise when, for example, a valid S/PDIF input signal was present for an extended period of time, but signal integrity worsened for a brief period, causing the receiver to then lose its lock to the input signal. In this case, Bit 0 (LOSS_OF_LOCK) transitions from 0b0 to 0b1 and remains set at 0b1 indefinitely. This indicates that, at some point during the operation of the device, lock to the input stream was lost. Bit 0 (LOSS_OF_LOCK) stays high at 0b1 until Register 0xF604 (SPDIF_RESTART), Bit 0 (RESTART_AUDIO), is set to 0b1, which clears Bit 0 (LOSS_OF_LOCK) back to 0b0. At that point, Register 0xF604 (SPDIF_RESTART), Bit 0 (RESTART_AUDIO), can be reset to 0b0 if required.

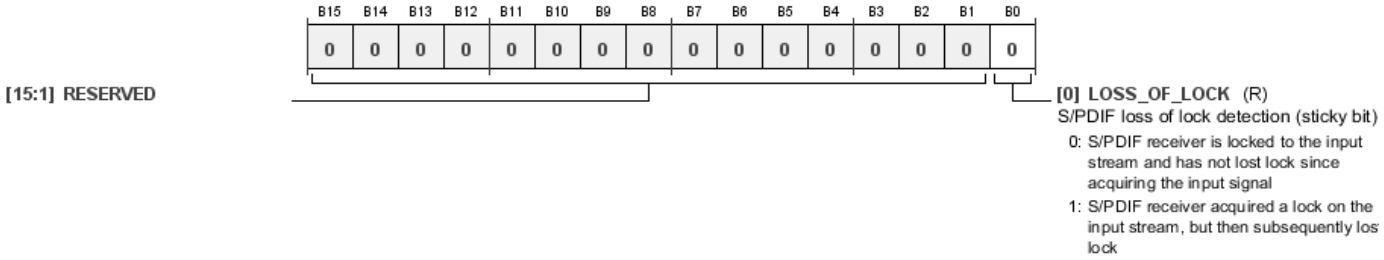


Table 141. Bit Descriptions for SPDIF_LOSS_OF_LOCK

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	LOSS_OF_LOCK		S/PDIF loss of lock detection (sticky bit).	0x0	R
		0	S/PDIF receiver is locked to the input stream and has not lost lock since acquiring the input signal.		
		1	S/PDIF receiver acquired a lock on the input stream but then subsequently lost lock.		

S/PDIF RECEIVER MCLK SPEED SELECTION REGISTER

Address: 0xF606, Reset: 0x0001, Name: SPDIF_RX_MCLKSPEED

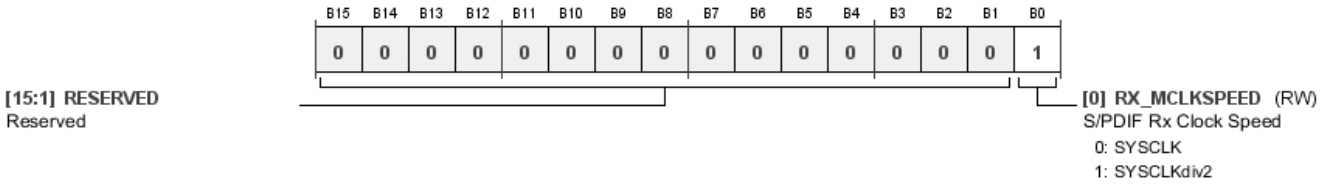


Table 142. Bit Descriptions for SPDIF_RX_MCLKSPEED

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0000	RW
0	RX_MCLKSPEED	S/PDIF Rx clock speed. 0: SYSCLK (higher rates). 1: SYSCLK ± 2 (lower rates).	0x1	RW

S/PDIF Transmitter User Data Bits (Left) Register

Address: 0xF6C0 to 0xF6CB (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_UD_LEFT_x

These 12 registers allow the 192 user data bits encoded on the left channel of the output data stream of the S/PDIF transmitter on the ADAU1467 and ADAU1463 to be configured manually. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

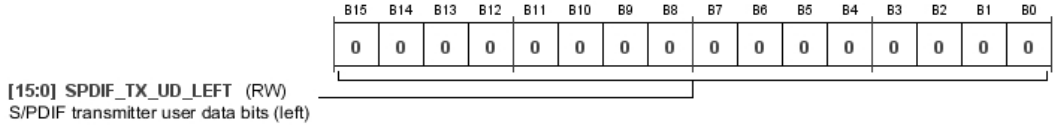


Table 159. Bit Descriptions for SPDIF_TX_UD_LEFT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_UD_LEFT		S/PDIF transmitter user data bits (left).	0x0000	RW

S/PDIF Transmitter User Data Bits (Right) Register

Address: 0xF6D0 to 0xF6DB (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_UD_RIGHT_x

These 12 registers allow the 192 user data bits encoded on the right channel of the output data stream of the S/PDIF transmitter on the ADAU1463 and ADAU1467 to be configured manually. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

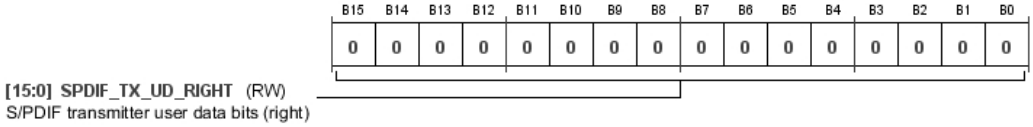


Table 160. Bit Descriptions for SPDIF_TX_UD_RIGHT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_UD_RIGHT		S/PDIF transmitter user data bits (right).	0x0000	RW

S/PDIF Transmitter Validity Bits (Left) Register

Address: 0xF6E0 to 0xF6EB (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_VB_LEFT_x

These 12 registers allow the 192 validity bits encoded on the left channel of the output data stream of the S/PDIF transmitter on the ADAU1463 and ADAU1467 to be configured manually. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

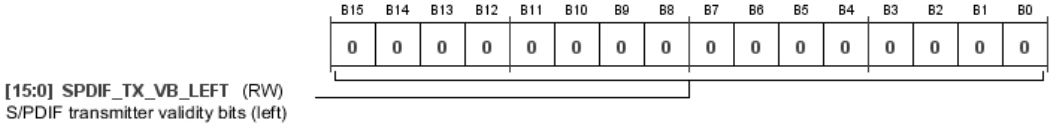


Table 161. Bit Descriptions for SPDIF_TX_VB_LEFT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_VB_LEFT		S/PDIF transmitter validity bits (left).	0x0000	RW

S/PDIF Transmitter Validity Bits (Right) Register

Address: 0xF6F0 to 0xF6FB (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_VB_RIGHT_x

These 12 registers allow the 192 validity bits encoded on the right channel of the output data stream of the S/PDIF transmitter on the ADAU1463 and ADAU1467 to be configured manually. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

Table 162. Bit Descriptions for SPDIF_TX_VB_RIGHT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_VB_RIGHT		S/PDIF transmitter validity bits (right).	0x0000	RW

S/PDIF Transmitter Parity Bits (Left) Register

Address: 0xF700 to Address 0xF70B (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_PB_LEFT_x

These 12 registers allow the 192 parity bits encoded on the left channel of the output data stream of the S/PDIF transmitter on the ADAU1463 and ADAU1467 to be configured manually. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

Table 163. Bit Descriptions for SPDIF_TX_PB_LEFT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_PB_LEFT		S/PDIF transmitter parity bits (left).	0x0000	RW

S/PDIF Transmitter Parity Bits (Right) Register

Address: 0xF710 to Address 0xF71B (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_PB_RIGHT_x

These 12 registers allow the 192 parity bits encoded on the right channel of the output data stream of the S/PDIF transmitter on the ADAU1463 and ADAU1467 to be configured manually. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

Table 164. Bit Descriptions for SPDIF_TX_PB_RIGHT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_PB_RIGHT		S/PDIF transmitter parity bits (right).	0x0000	RW

MP14 PIN DRIVE STRENGTH AND SLEW RATE REGISTER

Address: 0xF7A8, Reset: 0x0018, Name: MP14_PIN

This register configures the drive strength, slew rate, and pull resistors for the MP14 pin.

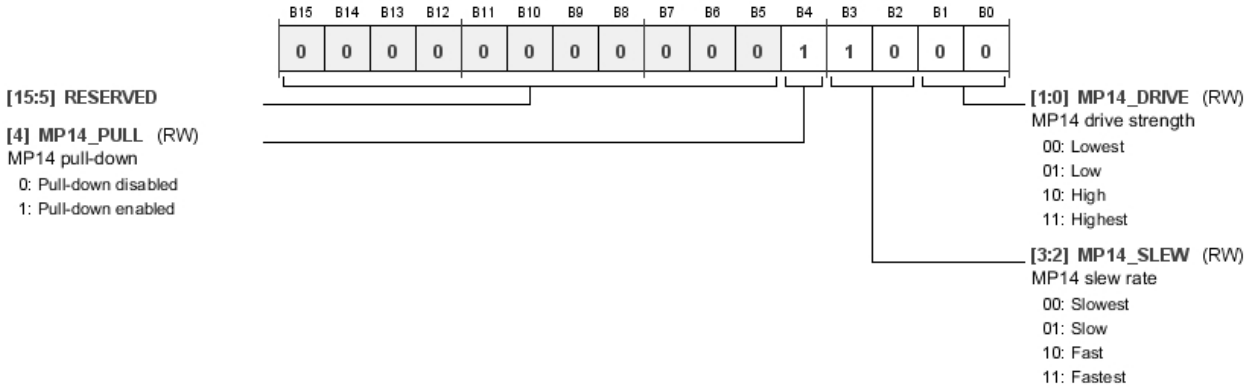


Table 183. Bit Descriptions for MP14_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	R
4	MP14_PULL		MP14 pull-down.	0x1	RW
		0	Pull-down disabled.		
		1	Pull-down enabled.		
[3:2]	MP14_SLEW		MP14 slew rate.	0x2	RW
		00	Slowest.		
		01	Slow.		
		10	Fast.		
		11	Fastest.		
[1:0]	MP14_DRIVE		MP14 drive strength.	0x0	RW
		00	Lowest.		
		01	Low.		
		10	High.		
		11	Highest.		

SDATA IN/OUT PINS DRIVE STRENGTH AND SLEW RATE REGISTERS

Address: 0xF7B0 to 0xF7B7, Reset: 0x0018, Name: SDATAIOx_PIN

This register configures the drive strength, slew rate, and pull resistors for the SDATIO0 pin.

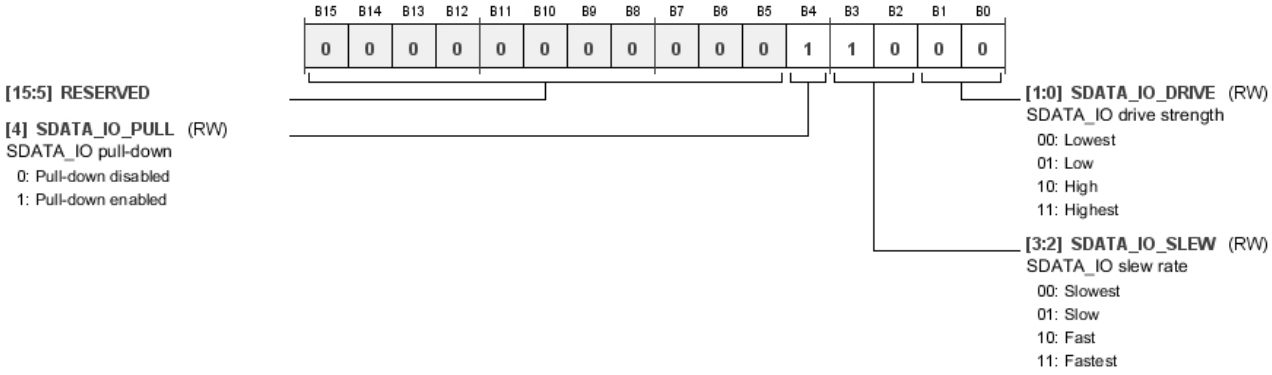


Table 185. Bit Descriptions for SDATA_IO0_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	R
4	SDATA_IO_PULL		SDATA_IO pull-down.	0x1	RW
		0	Pull-down disabled.		
		1	Pull-down enabled.		
[3:2]	SDATA_IO_SLEW		SDATA_IO slew rate.	0x2	RW
		00	Slowest.		
		01	Slow.		
		10	Fast.		
		11	Fastest.		
[1:0]	SDATA_IO_DRIVE		SDATA_IO drive strength.	0x0	RW
		00	Lowest.		
		01	Low.		
		10	High.		
		11	Highest.		