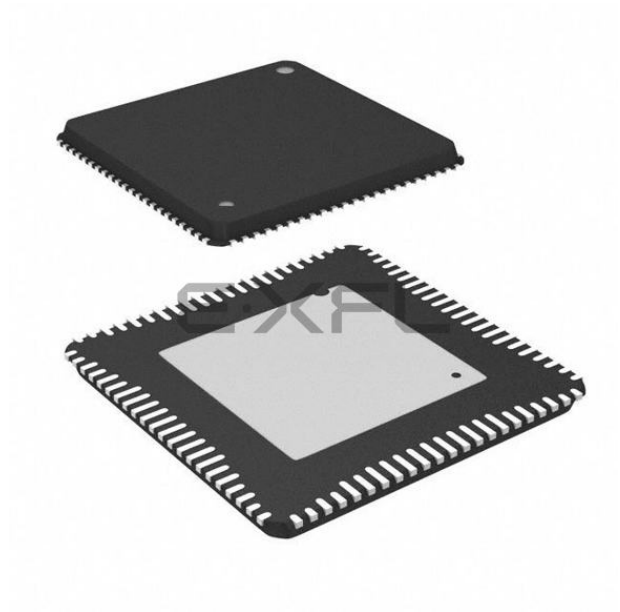

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	294.912MHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	320kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad, CSP
Supplier Device Package	88-LFCSP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1467wbcpz300rl

I²C Interface—Slave

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 11.

Parameter	Min	Typ	Max	Unit	Description
f_{SCL}			1000	kHz	SCL clock frequency
t_{SCLH}	0.26			µs	SCL pulse width high
t_{SCLL}	0.5			µs	SCL pulse width low
t_{SCS}	0.26			µs	Start and repeated start condition setup time
t_{SCH}	0.26			µs	Start condition hold time
t_{DS}	50			ns	Data setup time
t_{DH}			0.45	µs	Data hold time
t_{SCLR}			120	ns	SCL rise time
t_{SCLF}			120	ns	SCL fall time
t_{SDR}			120	ns	SDA rise time
t_{SDF}			120	ns	SDA fall time
t_{BFT}	0.5			µs	Bus free time between stop and start
t_{SUSTO}	0.26			µs	Stop condition setup time

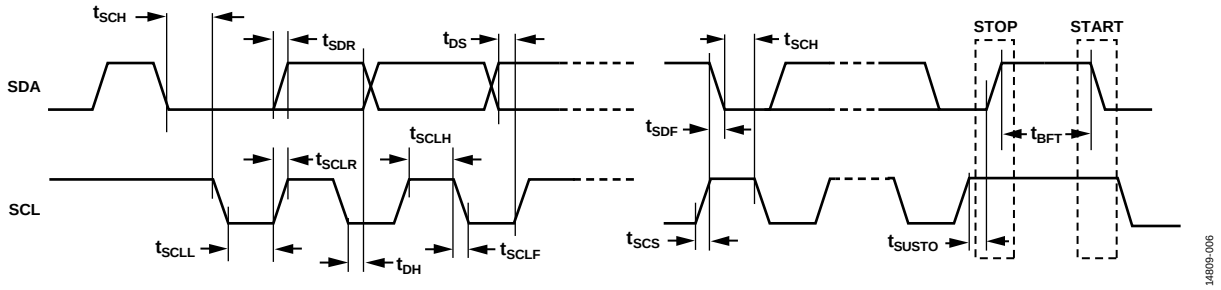


Figure 6. I²C Slave Port Timing Specifications

SPI Interface—Slave

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 13.

Parameter	Min	Typ	Max	Unit	Description
f_{SCLK_WRITE}			20	MHz	SCLK write frequency
f_{SCLK_READ}			20	MHz	SCLK read frequency
$t_{SCLKPWL}$	6			ns	SCLK pulse width low, SCLK = 20 MHz
$t_{SCLKPWH}$	21			ns	SCLK pulse width high, SCLK = 20 MHz
t_{SSS}	1			ns	SS setup to SCLK rising edge
t_{SSH}	2			ns	SS hold from SCLK rising edge
t_{SSPWH}	10			ns	SS pulse width high
t_{MOSIS}	1			ns	MOSI setup to SCLK rising edge
t_{MOSIH}	2			ns	MOSI hold from SCLK rising edge
t_{MISOD}			39	ns	MISO valid output delay from SCLK falling edge

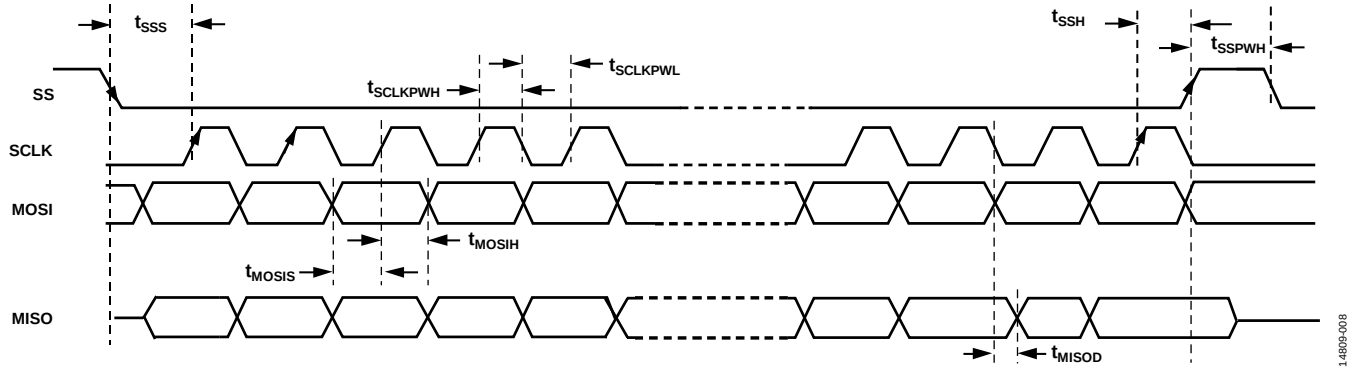
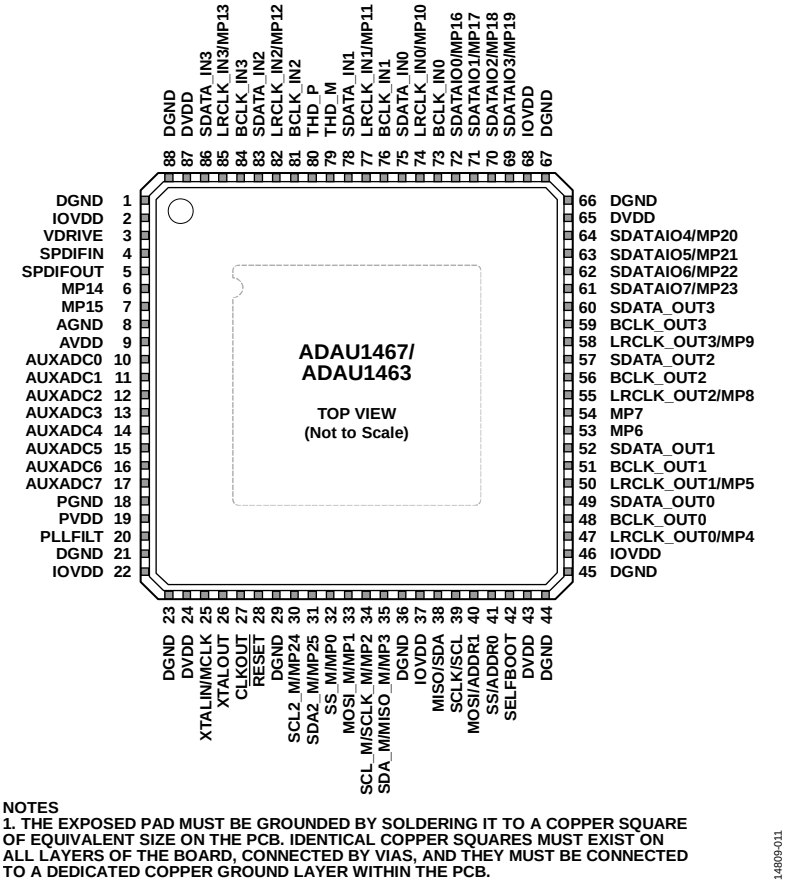


Figure 8. SPI Slave Port Timing Specifications

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE GROUNDED BY SOLDERING IT TO A COPPER SQUARE OF EQUIVALENT SIZE ON THE PCB. IDENTICAL COPPER SQUARES MUST EXIST ON ALL LAYERS OF THE BOARD, CONNECTED BY VIAS, AND THEY MUST BE CONNECTED TO A DEDICATED COPPER GROUND LAYER WITHIN THE PCB.

14809-011

Figure 11. Pin Configuration

Table 18. Pin Function Descriptions

Pin No.	Mnemonic	Internal Pull Resistor	Description
1	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors section and the Grounding section.
2	IOVDD	None	Input/Output Supply, 1.8 V − 5% to 3.3 V + 10%. Bypass this pin with decoupling capacitors to Pin 1 (DGND). See the Power Supply Bypass Capacitors section and the Grounding section.
3	VDRIVE	None	Positive Negative Positive (PNP) Bipolar Junction Transistor Base Drive Bias Pin for the Digital Supply Regulator. Connect VDRIVE to the base of an external PNP pass transistor (ON Semi NSS1C300ET4G is recommended). If an external supply is provided directly to DVDD, connect the VDRIVE pin to ground.
4	SPDIFIN	None	Input to the Integrated Sony/PDIF Receiver. Disconnect this pin when not in use. This pin is biased internally to IOVDD/2.
5	SPDIFOUT	Configurable	Output from the Integrated Sony/PDIF Transmitter. Disconnect this pin when not in use. This pin is biased internally to IOVDD/2.
6	MP14	Configurable	Multipurpose, General-Purpose Input/Output (GPIO) 14. Disconnect this pin when not in use.
7	MP15	Configurable	Multipurpose, GPIO 15. Disconnect this pin when not in use.
8	AGND	None	Analog Ground Reference for the Auxiliary ADC. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors section and the Grounding section.
9	AVDD	None	Analog Supply for the Auxiliary ADC. This supply muust be 3.3 V ± 10%. Bypass this pin with decoupling capacitors to Pin 8 (AGND). See the Power Supply Bypass Capacitors section and the Grounding section.

A sample timing diagram for a multiple word SPI write operation (burst write) to a register is shown in Figure 34. A sample timing diagram of a single word SPI read operation is shown in Figure 35. The MISO/SDA pin transitions from being three-state to being driven at the beginning of Byte 3. In this example, Byte 0 through Byte 2 contain the addresses and the R/$\overline{W}$ bit, and subsequent bytes carry the data. A sample timing diagram of a multiple word SPI read operation (burst read) is shown in Figure 36. In Figure 34 to Figure 36, rising edges on SCLK/SCL are indicated with an arrow, signifying that the data lines are sampled on the rising edge.

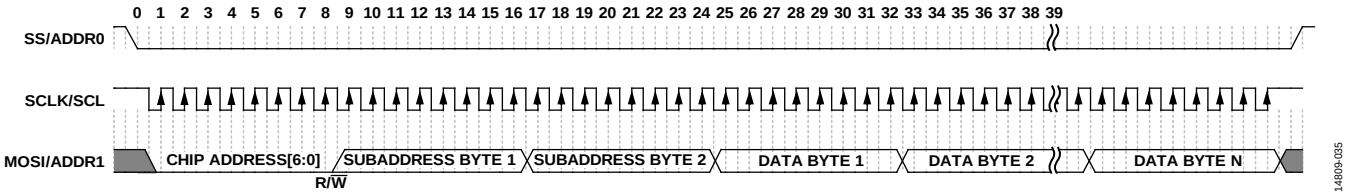


Figure 34. SPI Slave Write Clocking (Burst Write Mode, N Bytes)

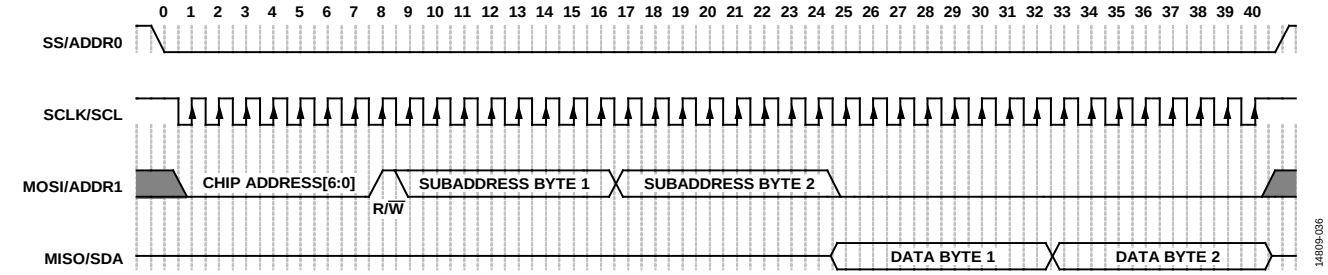


Figure 35. SPI Slave Read Clocking (Single Word Mode, Two Bytes)

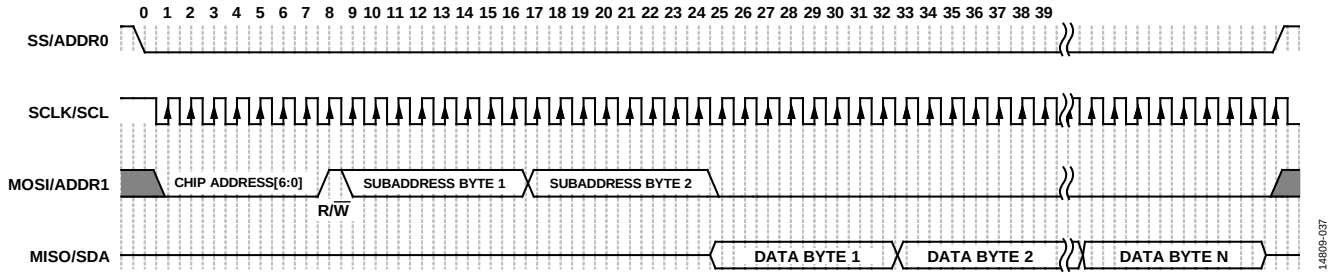


Figure 36. SPI Slave Read Clocking (Burst Read Mode, N Bytes)

Table 36. Serial Output Pin Mapping from SigmaStudio Channels[1]

Output Channel in SigmaStudio	Serial Output Pin	Position in I²S Stream (2-Channel)	Position in TDM4 Stream	Position in TDM8 Stream	Position in TDM16 Stream
0	SDATA_OUT0	Left	0	0	0
1	SDATA_OUT0	Right	1	1	1
2	SDATA_OUT0	Not applicable	2	2	2
3	SDATA_OUT0	Not applicable	3	3	3
4	SDATA_OUT0	First SDATAIOx left	First SDATAIOx	4	4
5	SDATA_OUT0	First SDATAIOx right	First SDATAIOx	5	5
6	SDATA_OUT0	Not applicable	First SDATAIOx	6	6
7	SDATA_OUT0	Not applicable	First SDATAIOx	7	7
8	SDATA_OUT0	Second SDATAIOx left	Second SDATAIOx	First SDATAIOx	8
9	SDATA_OUT0	Second SDATAIOx right	Second SDATAIOx	First SDATAIOx	9
10	SDATA_OUT0	Not applicable	Second SDATAIOx	First SDATAIOx	10
11	SDATA_OUT0	Not applicable	Second SDATAIOx	First SDATAIOx	11
12	SDATA_OUT0	Third SDATAIOx left	Third SDATAIOx	First SDATAIOx	12
13	SDATA_OUT0	Third SDATAIOx right	Third SDATAIOx	First SDATAIOx	13
14	SDATA_OUT0	Not applicable	Third SDATAIOx	First SDATAIOx	14
15	SDATA_OUT0	Not applicable	Third SDATAIOx	First SDATAIOx	15
16	SDATA_OUT1	Left	0	0	0
17	SDATA_OUT1	Right	1	1	1
18	SDATA_OUT1	Not applicable	2	2	2
19	SDATA_OUT1	Not applicable	3	3	3
20	SDATA_OUT1	First SDATAIOx left	First SDATAIOx	4	4
21	SDATA_OUT1	First SDATAIOx right	First SDATAIOx	5	5
22	SDATA_OUT1	Not applicable	First SDATAIOx	6	6
23	SDATA_OUT1	Not applicable	First SDATAIOx	7	7
24	SDATA_OUT1	Second SDATAIOx left	Second SDATAIOx	First SDATAIOx	8
25	SDATA_OUT1	Second SDATAIOx right	Second SDATAIOx	First SDATAIOx	9
26	SDATA_OUT1	Not applicable	Second SDATAIOx	First SDATAIOx	10
27	SDATA_OUT1	Not applicable	Second SDATAIOx	First SDATAIOx	11
28	SDATA_OUT1	Third SDATAIOx left	Third SDATAIOx	First SDATAIOx	12
29	SDATA_OUT1	Third SDATAIOx right	Third SDATAIOx	First SDATAIOx	13
30	SDATA_OUT1	Not applicable	Third SDATAIOx	First SDATAIOx	14
31	SDATA_OUT1	Not applicable	Third SDATAIOx	First SDATAIOx	15
32	SDATA_OUT2	Left	0	0	Not applicable
33	SDATA_OUT2	Right	1	1	Not applicable
34	SDATA_OUT2	Not applicable	2	2	Not applicable
35	SDATA_OUT2	Not applicable	3	3	Not applicable
36	SDATA_OUT2	SDATAIOx left	First SDATAIOx	4	Not applicable
37	SDATA_OUT2	SDATAIOx right	First SDATAIOx	5	Not applicable
38	SDATA_OUT2	Not applicable	First SDATAIOx	6	Not applicable
39	SDATA_OUT2	Not applicable	First SDATAIOx	7	Not applicable
40	SDATA_OUT3	Left	0	0	Not applicable
41	SDATA_OUT3	Right	1	1	Not applicable
42	SDATA_OUT3	Not applicable	2	2	Not applicable
43	SDATA_OUT3	Not applicable	3	3	Not applicable
44	SDATA_OUT3	SDATAIOx left	First SDATAIOx	4	Not applicable
45	SDATA_OUT3	SDATAIOx right	First SDATAIOx	5	Not applicable
46	SDATA_OUT3	Not applicable	First SDATAIOx	6	Not applicable
47	SDATA_OUT3	Not applicable	First SDATAIOx	7	Not applicable

[1] Any of the eight SDATAIOx pins can be assigned to any output.

Address	Register	Description
0xF18E	SOUT_SOURCE14	Source of data for serial output port (Channel 28 and Channel 29)
0xF18F	SOUT_SOURCE15	Source of data for serial output port (Channel 30 and Channel 31)
0xF190	SOUT_SOURCE16	Source of data for serial output port (Channel 32 and Channel 33)
0xF191	SOUT_SOURCE17	Source of data for serial output port (Channel 34 and Channel 35)
0xF192	SOUT_SOURCE18	Source of data for serial output port (Channel 36 and Channel 37)
0xF193	SOUT_SOURCE19	Source of data for serial output port (Channel 38 and Channel 39)
0xF194	SOUT_SOURCE20	Source of data for serial output port (Channel 40 and Channel 41)
0xF195	SOUT_SOURCE21	Source of data for serial output port (Channel 42 and Channel 43)
0xF196	SOUT_SOURCE22	Source of data for serial output port (Channel 44 and Channel 45)
0xF197	SOUT_SOURCE23	Source of data for serial output port (Channel 46 and Channel 47)
0xF1C0	SPDIFTX_INPUT	S/PDIF transmitter data selector

FLEXIBLE TDM INTERFACE

The flexible TDM interface is available as an optional mode of operation on the SDATA_IN2 and SDATA_IN3 serial input ports, as well as on the SDATA_OUT2 and SDATA_OUT3 serial output ports. To use flexible TDM mode, the corresponding serial ports must be set in flexible TDM mode (SERIAL_BYTE_x_0 register, Bits[6:5] (WORD_LEN) = 0b11 and SERIAL_BYTE_x_0 register, Bits[2:0] = 0b010). Flexible TDM input mode requires that both SDATA_IN2 and SDATA_IN3 be configured for flexible TDM mode. Likewise, flexible TDM output mode requires that both SDATA_OUT2 and SDATA_OUT3 pins be configured for flexible TDM mode.

The flexible TDM interface provides byte addressable data placement in the input and output data streams on the corresponding serial data input/output pins. Each data stream is configured like a standard 8-channel TDM interface, with a total of 256 data bits (or 32 bytes) in the span of an audio frame. Because flexible TDM mode runs on two pins simultaneously, and each pin has 32 bytes of data, this means that there are a total of 64 data bytes. In flexible TDM input mode, each input channel inside the device can select its source data from any of the 64 input data bytes. In flexible TDM output mode, any serial output channel can be routed to any of the 64 output data bytes.

Flexible TDM Input

In flexible TDM input mode, two 256-bit data streams are input to the SDATA_IN2 and SDATA_IN3 pins. These 256 bits of data compose eight channels of four bytes each, for a total of 32 bytes on each pin, and a total of 64 bytes when both input pins are combined. The flexible TDM input functional block routes the desired input byte to a given byte in the serial input channels. Those serial input channels are then available as normal audio data in the audio routing matrix. The data can be passed to the DSP core, the ASRC inputs, or the serial outputs as needed.

A total of 64 control registers (FTDM_INx) can be configured to set up the mapping of input data bytes to the corresponding bytes in the serial input channels. Each byte in each serial input channel has a corresponding control register that selects the incoming data byte on the serial input pins that must be mapped to it. Figure 67 shows, from left to right, the data streams entering the serial input pins, the serial input channels, and the registers (see FTDM_INx, Register 0xF300 to Register 0xF33F) that correspond to each byte in the serial input channels.

Flexible TDM Output

In flexible TDM output mode, two 256-bit data streams are output from the SDATA_OUT2 and SDATA_OUT3 pins. These 256 bits of data compose eight channels of four bytes each, for a total of 32 bytes on each pin, and a total of 64 bytes when both input pins are combined. The flexible TDM output functional block routes the desired byte from the desired serial output channel to a given byte in the output streams. The serial output channels originate from the audio routing matrix, which is configured using the SOUT_SOURCEx control registers.

There are a total of 64 control registers (see FTDM_OUTx, Register 0xF380 to Register 0xF3BF) that can be configured to set up the mapping of the bytes in the serial output channels and the bytes in the data streams exiting the serial output pins. Each byte in the data streams being output from the serial output pins has a corresponding control register, which selects the desired byte from the desired serial output channel. Figure 68 shows, from left to right, the serial output channels originating from the routing matrix, the serial output pins and data streams, and the control registers (FTDM_OUTx) that correspond to each byte in the serial output data streams.

Flexible TDM Registers

An overview of the registers related to the flexible TDM interface is shown in Table 45. For a more detailed description, see the Flexible TDM Interface Registers section.

Table 45. Flexible TDM Registers

Address	Register	Description
0xF300	FTDM_IN0	FTDM mapping for the serial inputs (Channel 32, Bits[31:24])
0xF301	FTDM_IN1	FTDM mapping for the serial inputs (Channel 32, Bits[23:16])
0xF302	FTDM_IN2	FTDM mapping for the serial inputs (Channel 32, Bits[15:8])
0xF303	FTDM_IN3	FTDM mapping for the serial inputs (Channel 32, Bits[7:0])
0xF304	FTDM_IN4	FTDM mapping for the serial inputs (Channel 33, Bits[31:24])
0xF305	FTDM_IN5	FTDM mapping for the serial inputs (Channel 33, Bits[23:16])
0xF306	FTDM_IN6	FTDM mapping for the serial inputs (Channel 33, Bits[15:8])
0xF307	FTDM_IN7	FTDM mapping for the serial inputs Channel 33, Bits[7:0])
0xF308	FTDM_IN8	FTDM mapping for the serial inputs (Channel 34, Bits[31:24])
0xF309	FTDM_IN9	FTDM mapping for the serial inputs (Channel 34, Bits[23:16])
0xF30A	FTDM_IN10	FTDM mapping for the serial inputs (Channel 34, Bits[15:8])
0xF30B	FTDM_IN11	FTDM mapping for the serial inputs (Channel 34, Bits[7:0])
0xF30C	FTDM_IN12	FTDM mapping for the serial inputs (Channel 35, Bits[31:24])
0xF30D	FTDM_IN13	FTDM mapping for the serial inputs (Channel 35, Bits[23:16])
0xF30E	FTDM_IN14	FTDM mapping for the serial inputs (Channel 35, Bits[15:8])
0xF30F	FTDM_IN15	FTDM mapping for the serial inputs (Channel 35, Bits[7:0])
0xF310	FTDM_IN16	FTDM mapping for the serial inputs (Channel 36, Bits[31:24])
0xF311	FTDM_IN17	FTDM mapping for the serial inputs (Channel 36, Bits[23:16])
0xF312	FTDM_IN18	FTDM mapping for the serial inputs (Channel 36, Bits[15:8])
0xF313	FTDM_IN19	FTDM mapping for the serial inputs (Channel 36, Bits[7:0])
0xF314	FTDM_IN20	FTDM mapping for the serial inputs (Channel 37, Bits[31:24])
0xF315	FTDM_IN21	FTDM mapping for the serial inputs (Channel 37, Bits[23:16])
0xF316	FTDM_IN22	FTDM mapping for the serial inputs (Channel 37, Bits[15:8])
0xF317	FTDM_IN23	FTDM mapping for the serial inputs (Channel 37, Bits[7:0])
0xF318	FTDM_IN24	FTDM mapping for the serial inputs (Channel 38, Bits[31:24])
0xF319	FTDM_IN25	FTDM mapping for the serial inputs (Channel 38, Bits[23:16])
0xF31A	FTDM_IN26	FTDM mapping for the serial inputs (Channel 38, Bits[15:8])
0xF31B	FTDM_IN27	FTDM mapping for the serial inputs (Channel 38, Bits[7:0])
0xF31C	FTDM_IN28	FTDM mapping for the serial inputs (Channel 39, Bits[31:24])
0xF31D	FTDM_IN29	FTDM mapping for the serial inputs (Channel 39, Bits[23:16])
0xF31E	FTDM_IN30	FTDM mapping for the serial inputs (Channel 39, Bits[15:8])
0xF31F	FTDM_IN31	FTDM mapping for the serial inputs (Channel 39, Bits[7:0])
0xF320	FTDM_IN32	FTDM mapping for the serial inputs (Channel 40, Bits[31:24])
0xF321	FTDM_IN33	FTDM mapping for the serial inputs (Channel 40, Bits[23:16])
0xF322	FTDM_IN34	FTDM mapping for the serial inputs (Channel 40, Bits[15:8])
0xF323	FTDM_IN35	FTDM mapping for the serial inputs (Channel 40, Bits[7:0])
0xF324	FTDM_IN36	FTDM mapping for the serial inputs (Channel 41, Bits[31:24])
0xF325	FTDM_IN37	FTDM mapping for the serial inputs (Channel 41, Bits[23:16])
0xF326	FTDM_IN38	FTDM mapping for the serial inputs (Channel 41, Bits[15:8])
0xF327	FTDM_IN39	FTDM mapping for the serial inputs (Channel 41, Bits[7:0])
0xF328	FTDM_IN40	FTDM mapping for the serial inputs (Channel 42, Bits[31:24])
0xF329	FTDM_IN41	FTDM mapping for the serial inputs (Channel 42, Bits[23:16])
0xF32A	FTDM_IN42	FTDM mapping for the serial inputs (Channel 42, Bits[15:8])
0xF32B	FTDM_IN43	FTDM mapping for the serial inputs (Channel 42, Bits[7:0])
0xF32C	FTDM_IN44	FTDM mapping for the serial inputs (Channel 43, Bits[31:24])
0xF32D	FTDM_IN45	FTDM mapping for the serial inputs (Channel 43, Bits[23:16])
0xF32E	FTDM_IN46	FTDM mapping for the serial inputs (Channel 43, Bits[15:8])
0xF32F	FTDM_IN47	FTDM mapping for the serial inputs (Channel 43, Bits[7:0])

MULTIPURPOSE PINS

A total of 25 pins are available for use as GPIOs that are multiplexed with other functions, such as clock inputs/outputs. Because these pins have multiple functions, they are referred to as multipurpose pins, or MPx pins.

Multipurpose pins can be configured in several modes using the MPx_MODE registers:

- Hardware input from pin
- Software input (written via I²C or SPI slave control port)
- Hardware output with internal pull-up resistor
- Hardware output without internal pull-up resistor
- PDM microphone data input
- Flag output from panic manager
- Slave select line for master SPI port

When configured in hardware input mode, a debounce circuit is available to avoid data glitches.

When operating in GPIO mode, the pin status is updated once per sample, which means that the state of a GPIO (MPx pin) cannot change more than once in a sample period.

General-Purpose Inputs to the DSP Core

When a multipurpose pin is configured as a general-purpose input, its value can be used as a control logic signal in the DSP program, which is configured using SigmaStudio. Figure 73 shows the location of the general-purpose input cell within the SigmaStudio toolbox.

The 26 available general-purpose inputs in SigmaStudio map to the corresponding 26 multipurpose pins; however, their data is valid only if the corresponding multipurpose pin is configured as an input using the MPx_MODE registers. Figure 75 shows all of the general-purpose inputs as they appear in the SigmaStudio signal flow.

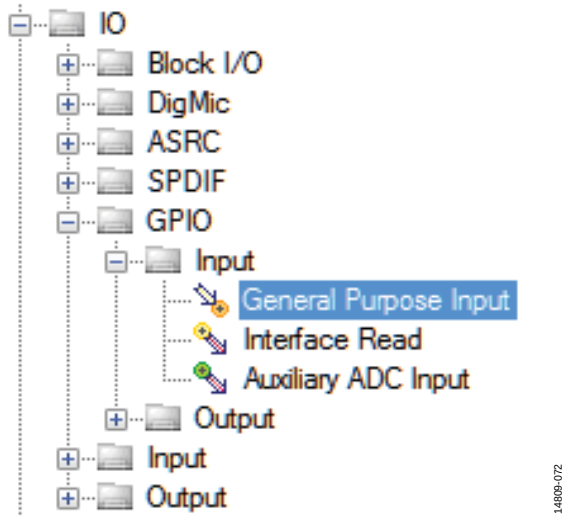


Figure 73. General-Purpose Input in the SigmaStudio Toolbox

General-Purpose Outputs from the DSP Core

When a multipurpose pin is configured as a general-purpose output, a Boolean value is output from the DSP program to the corresponding multipurpose pin. Figure 74 shows the location of the general-purpose input cell within the SigmaStudio toolbox.

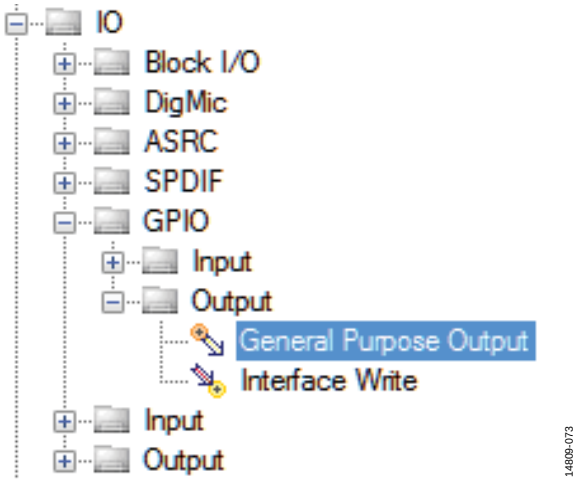


Figure 74. General-Purpose Output in the SigmaStudio Toolbox

Address	Register	Description
0xF5C5	MP19_MODE	Multipurpose pin mode (SDATAIO3/MP19)
0xF5C6	MP20_MODE	Multipurpose pin mode (SDATAIO4/MP20)
0xF5C7	MP21_MODE	Multipurpose pin mode (SDATAIO5/MP21)
0xF5C8	MP22_MODE	Multipurpose pin mode (SDATAIO6/MP22)
0xF5C9	MP23_MODE	Multipurpose pin mode (SDATAIO7/MP23)
0xF5CA	MP24_MODE	Multipurpose pin mode (SCL2_M/MP24)
0xF51D	MP25_MODE	Multipurpose pin mode (SDA2_M/MP25)
0xF520	MP0_WRITE	Multipurpose pin write value (SS_M/MP0)
0xF521	MP1_WRITE	Multipurpose pin write value (MOSI_M/MP1)
0xF522	MP2_WRITE	Multipurpose pin write value (SCL_M/SCLK_M/MP2)
0xF523	MP3_WRITE	Multipurpose pin write value (SDA_M/MISO_M/MP3)
0xF524	MP4_WRITE	Multipurpose pin write value (LRCLK_OUT0/MP4)
0xF525	MP5_WRITE	Multipurpose pin write value (LRCLK_OUT1/MP5)
0xF526	MP6_WRITE	Multipurpose pin write value (MP6)
0xF527	MP7_WRITE	Multipurpose pin write value (MP7)
0xF528	MP8_WRITE	Multipurpose pin write value (LRCLK_OUT2/MP8)
0xF529	MP9_WRITE	Multipurpose pin write value (LRCLK_OUT3/MP9)
0xF52A	MP10_WRITE	Multipurpose pin write value (LRCLK_IN0/MP10)
0xF52B	MP11_WRITE	Multipurpose pin write value (LRCLK_IN1/MP11)
0xF52C	MP12_WRITE	Multipurpose pin write value (LRCLK_IN2/MP12)
0xF52D	MP13_WRITE	Multipurpose pin write value (LRCLK_IN3/MP13)
0xF5D0	MP14_WRITE	Multipurpose pin write value (MP14)
0xF5D1	MP15_WRITE	Multipurpose pin write value (MP15)
0xF5D2	MP16_WRITE	Multipurpose pin write value (SDATAIO0/MP16)
0xF5D3	MP17_WRITE	Multipurpose pin write value (SDATAIO1/MP17)
0xF5D4	MP18_WRITE	Multipurpose pin write value (SDATAIO2/MP18)
0xF5D5	MP19_WRITE	Multipurpose pin write value (SDATAIO3/MP19)
0xF5D6	MP20_WRITE	Multipurpose pin write value (SDATAIO4/MP20)
0xF5D7	MP21_WRITE	Multipurpose pin write value (SDATAIO5/MP21)
0xF5D8	MP22_WRITE	Multipurpose pin write value (SDATAIO6/MP22)
0xF5D9	MP23_WRITE	Multipurpose pin write value (SDATAIO7/MP23)
0xF5DA	MP24_WRITE	Multipurpose pin write value (SCL2_M/MP24)
0xF52D	MP25_WRITE	Multipurpose pin write value (SDA2_M/MP25)
0xF530	MP0_READ	Multipurpose pin read value (SS_M/MP0)
0xF531	MP1_READ	Multipurpose pin read value (MOSI_M/MP1)
0xF532	MP2_READ	Multipurpose pin read value (SCL_M/SCLK_M/MP2)
0xF533	MP3_READ	Multipurpose pin read value (SDA_M/MISO_M/MP3)
0xF534	MP4_READ	Multipurpose pin read value (LRCLK_OUT0/MP4)
0xF535	MP5_READ	Multipurpose pin read value (LRCLK_OUT1/MP5)
0xF536	MP6_READ	Multipurpose pin read value (MP6)
0xF537	MP7_READ	Multipurpose pin read value (MP7)
0xF538	MP8_READ	Multipurpose pin read value (LRCLK_OUT2/MP8)
0xF539	MP9_READ	Multipurpose pin read value (LRCLK_OUT3/MP9)
0xF53A	MP10_READ	Multipurpose pin read value (LRCLK_IN0/MP10)
0xF53B	MP11_READ	Multipurpose pin read value (LRCLK_IN1/MP11)
0xF53C	MP12_READ	Multipurpose pin read value (LRCLK_IN2/MP12)
0xF53D	MP13_READ	Multipurpose pin read value (LRCLK_IN3/MP13)

Table 57. Pin Drive Strength, Slew Rate, and Pull Configuration Registers

Address	Register	Description
0xF780	BCLK_IN0_PIN	BCLK input pin drive strength and slew rate (BCLK_IN0)
0xF781	BCLK_IN1_PIN	BCLK input pin drive strength and slew rate (BCLK_IN1)
0xF782	BCLK_IN2_PIN	BCLK input pin drive strength and slew rate (BCLK_IN2)
0xF783	BCLK_IN3_PIN	BCLK input pin drive strength and slew rate (BCLK_IN3)
0xF784	BCLK_OUT0_PIN	BCLK output pin drive strength and slew rate (BCLK_OUT0)
0xF785	BCLK_OUT1_PIN	BCLK output pin drive strength and slew rate (BCLK_OUT1)
0xF786	BCLK_OUT2_PIN	BCLK output pin drive strength and slew rate (BCLK_OUT2)
0xF787	BCLK_OUT3_PIN	BCLK output pin drive strength and slew rate (BCLK_OUT3)
0xF788	LRCLK_IN0_PIN	LRCLK input pin drive strength and slew rate (LRCLK_IN0)
0xF789	LRCLK_IN1_PIN	LRCLK input pin drive strength and slew rate (LRCLK_IN1)
0xF78A	LRCLK_IN2_PIN	LRCLK input pin drive strength and slew rate (LRCLK_IN2)
0xF78B	LRCLK_IN3_PIN	LRCLK input pin drive strength and slew rate (LRCLK_IN3)
0xF78C	LRCLK_OUT0_PIN	LRCLK output pin drive strength and slew rate (LRCLK_OUT0)
0xF78D	LRCLK_OUT1_PIN	LRCLK output pin drive strength and slew rate (LRCLK_OUT1)
0xF78E	LRCLK_OUT2_PIN	LRCLK output pin drive strength and slew rate (LRCLK_OUT2)
0xF78F	LRCLK_OUT3_PIN	LRCLK output pin drive strength and slew rate (LRCLK_OUT3)
0xF790	SDATA_IN0_PIN	SDATA input pin drive strength and slew rate (SDATA_IN0)
0xF791	SDATA_IN1_PIN	SDATA input pin drive strength and slew rate (SDATA_IN1)
0xF792	SDATA_IN2_PIN	SDATA input pin drive strength and slew rate (SDATA_IN2)
0xF793	SDATA_IN3_PIN	SDATA input pin drive strength and slew rate (SDATA_IN3)
0xF794	SDATA_OUT0_PIN	SDATA output pin drive strength and slew rate (SDATA_OUT0)
0xF795	SDATA_OUT1_PIN	SDATA output pin drive strength and slew rate (SDATA_OUT1)
0xF796	SDATA_OUT2_PIN	SDATA output pin drive strength and slew rate (SDATA_OUT2)
0xF797	SDATA_OUT3_PIN	SDATA output pin drive strength and slew rate (SDATA_OUT3)
0xF798	SPDIF_TX_PIN	S/PDIF transmitter pin drive strength and slew rate
0xF799	SCLK_SCL_PIN	SCLK/SCL pin drive strength and slew rate
0xF79A	MISO_SDA_PIN	MISO/SDA pin drive strength and slew rate
0xF79B	SS_PIN	SS/ADDR0 pin drive strength and slew rate
0xF79C	MOSI_ADDR1_PIN	MOSI/ADDR1 pin drive strength and slew rate
0xF79D	SCLK_SCL_M_PIN	SCL_M/SCLK_M/MP2 pin drive strength and slew rate
0xF79E	MISO_SDA_M_PIN	SDA_M/MISO_M/MP3 pin drive strength and slew rate
0xF79F	SS_M_PIN	SS_M/MP0 pin drive strength and slew rate
0xF7A0	MOSI_M_PIN	MOSI_M/MP1 pin drive strength and slew rate
0xF7A1	MP6_PIN	MP6 pin drive strength and slew rate
0xF7A2	MP7_PIN	MP7 pin drive strength and slew rate
0xF7A3	CLKOUT_PIN	CLKOUT pin drive strength and slew rate

Table 74. Bit Descriptions for CLK_GEN3_SRC

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	CLK_GEN3_SRC		Reference source for Clock Generator 3. This bit selects the reference of Clock Generator 3. If set to use an external reference clock, Bits[3:0] define the source pin. Otherwise, the PLL output is used as the reference clock. When an external reference clock is used for Clock Generator 3, the resulting base output frequency of Clock Generator 3 is the frequency of the input reference clock multiplied by the Clock Generator 3 numerator, divided by 1024. For example: if Bit 4 (CLK_GEN3_SRC) = 0b1 (an external reference clock is used); Bits[3:0] (FREF_PIN) = 0b1110 (the input signal of the S/PDIF receiver is used as the reference source); the sample rate of the S/PDIF input signal = 48 kHz; and the numerator of Clock Generator 3 = 2048; the resulting base output sample rate of Clock Generator 3 is 48 kHz × 2048/1024 = 96 kHz.	0x0	RW
		0	Reference signal provided by PLL output; multiply the frequency of that signal by N and divide it by M.		
		1	Reference signal provided by the signal input to the hardware pin defined by Bits[3:0] (FREF_PIN); multiply the frequency of that signal by N (and then divide by 1024) to get the resulting sample rate. M is ignored.		
[3:0]	FREF_PIN		Input reference for Clock Generator 3. If Clock Generator 3 is set up to lock to an external reference clock (Bit 4 (CLK_GEN3_SRC) = 0b1), these bits allow the user to specify which pin is receiving the reference clock. The signal input to the corresponding pin must be a 50% duty cycle square wave clock representing the reference sample rate.	0xE	RW
		0000	Input reference source is SS_M/MP0.		
		0001	Input reference source is MOSI_M/MP1.		
		0010	Input reference source is SCL_M/SCLK_M/MP2.		
		0011	Input reference source is SDA_M/MISO_M/MP3.		
		0100	Input reference source is LRCLK_OUT0/MP4.		
		0101	Input reference source is LRCLK_OUT1/MP5.		
		0110	Input reference source is MP6.		
		0111	Input reference source is MP7.		
		1000	Input reference source is LRCLK_OUT2/MP8.		
		1001	Input reference source is LRCLK_OUT3/MP9.		
		1010	Input reference source is LRCLK_IN0/MP10.		
		1011	Input reference source is LRCLK_IN1/MP11.		
		1100	Input reference source is LRCLK_IN2/MP12.		
		1101	Input reference source is LRCLK_IN3/MP13.		
		1110	Input reference source is S/PDIF receiver (recovered frame clock).		

Bits	Bit Name	Settings	Description	Reset	Access
		0110	Internal rate (the base output rate of Clock Generator 1); see Register 0xF020 (CLK_GEN1_M) and Register 0xF021 (CLK_GEN1_N).		
		0111	Internal rate × 2 (the doubled output rate of Clock Generator 1); see Register 0xF020 (CLK_GEN1_M) and Register 0xF021 (CLK_GEN1_N).		
		1000	Internal rate × 4 (the quadrupled output rate of Clock Generator 1); see Register 0xF020 (CLK_GEN1_M) and Register 0xF021 (CLK_GEN1_N).		
		1001	Internal rate × (1/2) the halved output rate of Clock Generator 1); see Register 0xF020 (CLK_GEN1_M) and Register 0xF021 (CLK_GEN1_N).		
		1010	Internal rate × (1/3) (one-third output of Clock Generator 2); see Register 0xF022 (CLK_GEN2_M) and Register 0xF023 (CLK_GEN2_N).		
		1011	Internal rate × (1/4) (quartered output of Clock Generator 1); see Register 0xF020 (CLK_GEN1_M) and Register 0xF021 (CLK_GEN1_N).		
		1100	Internal rate × (1/6) (one-sixth output of Clock Generator 2); see Register 0xF022 (CLK_GEN2_M) and Register 0xF023 (CLK_GEN2_N).		

FLEXIBLE TDM INTERFACE REGISTERS

FTDM Mapping for the Serial Inputs Register

Address: 0xF300 to 0xF33F (Increments of 0x1), Reset: 0x0000, Name: FTDM_INx

These 64 registers correspond to the 64 bytes of data that combine to form the 16 audio channels derived from the data streams being input to the SDATA_IN2 and SDATA_IN3 pins.

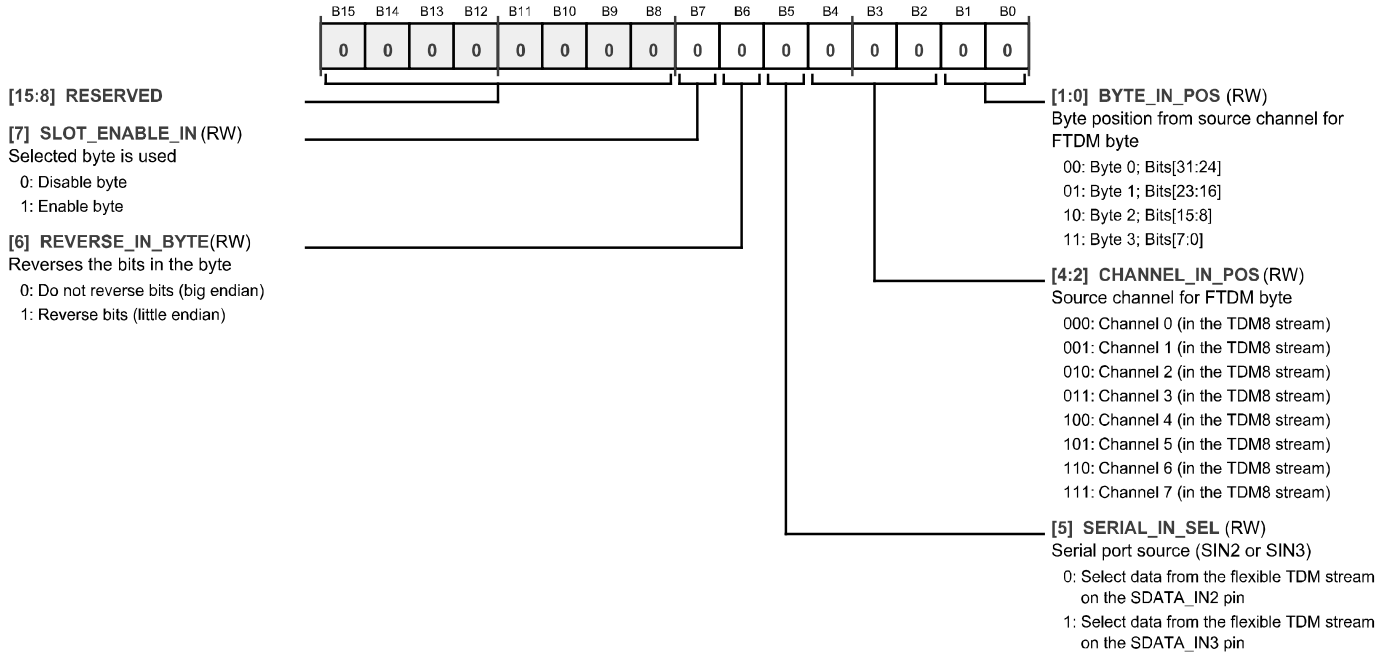


Table 87. Bit Descriptions for FTDM_INx

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x0	RW
7	SLOT_ENABLE_IN		Selected byte is used. This bit determines whether or not the slot is active. If active, valid data is input from the corresponding data slot on the selected channel of the selected input pin. If disabled, input data from the corresponding data slot on the selected channel of the selected input pin is ignored.	0x0	RW
		0	Disable byte.		
		1	Enable byte.		
6	REVERSE_IN_BYTE		Reverses the bits in the byte. This bit changes the endianness of the data bits within the byte by optionally reversing the order of the bits from MSB to LSB.	0x0	RW
		0	Do not reverse bits (big endian).		
		1	Reverse bits (little endian).		
5	SERIAL_IN_SEL		Serial port source (SDATA_IN2 or SDATA_IN3). If this bit = 0b0, the slot is mapped to Audio Channel 32 to Audio Channel 39. If this bit = 0b1, the slot is mapped to Audio Channel 40 to Audio Channel 47. The exact channel assignment is determined by Bits[4:2] (CHANNEL_IN_POS).	0x0	RW
		0	Select data from the flexible TDM stream on the SDATA_IN2 pin.		
		1	Select data from the flexible TDM stream on the SDATA_IN3 pin.		

Watchdog Maximum Count Register

Address: 0xF443, Reset: 0x0000, Name: WATCHDOG_MAXCOUNT

This register is designed to start counting at a specified number and decrement by 1 for each clock cycle of the system clock in the core. The counter is reset to the maximum value each time the program counter jumps to the beginning of the program to begin processing another audio frame (this is implemented in the DSP program code generated by SigmaStudio). If the counter reaches 0, a watchdog error flag is raised in the panic manager. The watchdog is typically set to begin counting from a number slightly larger than the maximum number of instructions expected to execute in the program, such that an error occurs if the program does not finish in time for the next incoming sample.

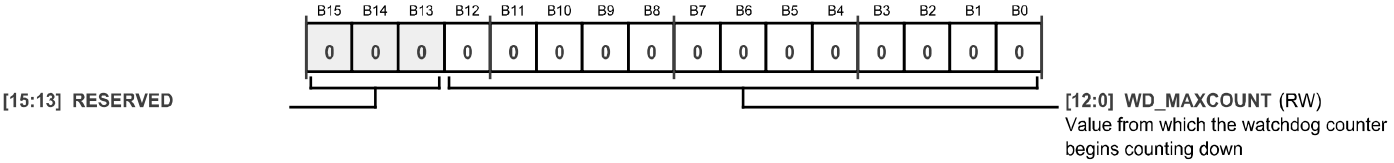


Table 104. Bit Descriptions for WATCHDOG_MAXCOUNT

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED			0x0	RW
[12:0]	WD_MAXCOUNT		Value from which the watchdog counter begins counting down.	0x0000	RW

Watchdog Prescale Register

Address: 0xF444, Reset: 0x0000, Name: WATCHDOG_PRESCALE

The watchdog prescaler is a number that is multiplied by the setting in Register 0xF443 (WATCHDOG_MAXCOUNT) to achieve very large counts for the watchdog, if necessary. Using the largest prescale factor of 128 × 1024 and the largest watchdog maximum count of 64 × 1024, a very large watchdog counter, on the order of 8.5 billion clock cycles, can be achieved.

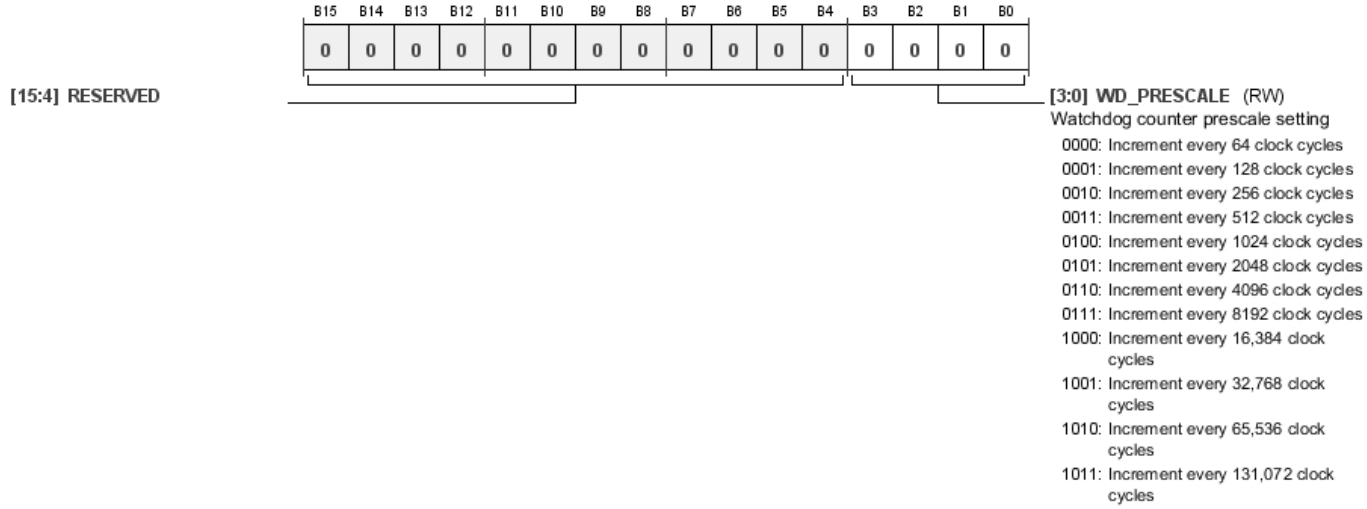


Table 105. Bit Descriptions for WATCHDOG_PRESCALE

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	RESERVED			0x0	RW
[3:0]	WD_PRESCALE		Watchdog counter prescale setting.	0x0	RW
		0000	Increment every 64 clock cycles.		
		0001	Increment every 128 clock cycles.		
		0010	Increment every 256 clock cycles.		
		0011	Increment every 512 clock cycles.		
		0100	Increment every 1024 clock cycles.		
		0101	Increment every 2048 clock cycles.		
		0110	Increment every 4096 clock cycles.		
		0111	Increment every 8192 clock cycles.		
		1000	Increment every 16,384 clock cycles.		

Program Counter Length, Bits[23:16] Register

Address: 0xF463, Reset: 0x0000, Name: PROG_CNTR_LENGTH0

This register, in combination with Register 0xF464 (PROG_CNTR_LENGTH1), keeps track of the peak value reached by the program counter during the last audio frame or block. It can be cleared using Register 0xF462 (PROG_CNTR_CLEAR).

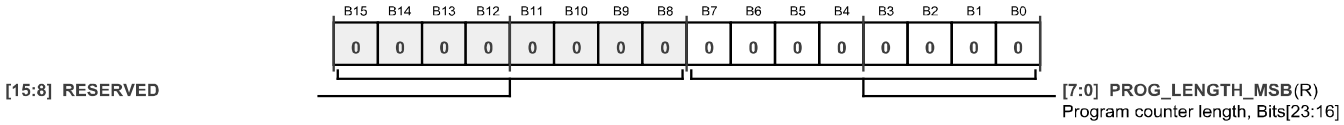


Table 111. Bit Descriptions for PROG_CNTR_LENGTH0

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x0	RW
[7:0]	PROG_LENGTH_MSB		Program counter length, Bits[23:16]	0x00	R

Program Counter Length, Bits[15:0] Register

Address: 0xF464, Reset: 0x0000, Name: PROG_CNTR_LENGTH1

This register, in combination with Register 0xF463 (PROG_CNTR_LENGTH0), keeps track of the peak value reached by the program counter during the last audio frame or block. It can be cleared using Register 0xF462 (PROG_CNTR_CLEAR).

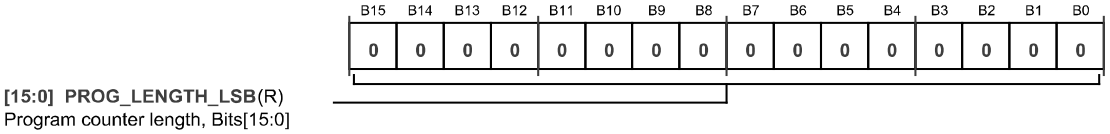


Table 112. Bit Descriptions for PROG_CNTR_LENGTH1

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	PROG_LENGTH_LSB		Program counter length, Bits[15:0]	0x0000	R

Program Counter Maximum Length, Bits[23:16] Register

Address: 0xF465, Reset: 0x0000, Name: PROG_CNTR_MAXLENGTH0

This register, in combination with Register 0xF466 (PROG_CNTR_MAXLENGTH1), keeps track of the highest peak value reached by the program counter since the DSP core started. It can be cleared using Register 0xF462 (PROG_CNTR_CLEAR).

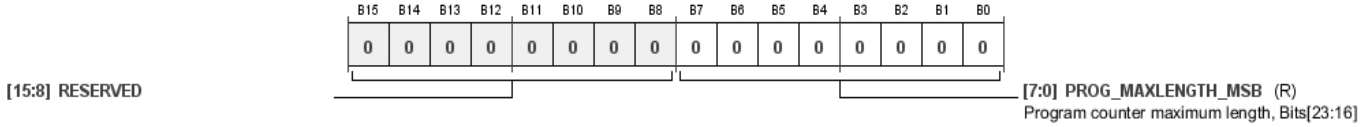


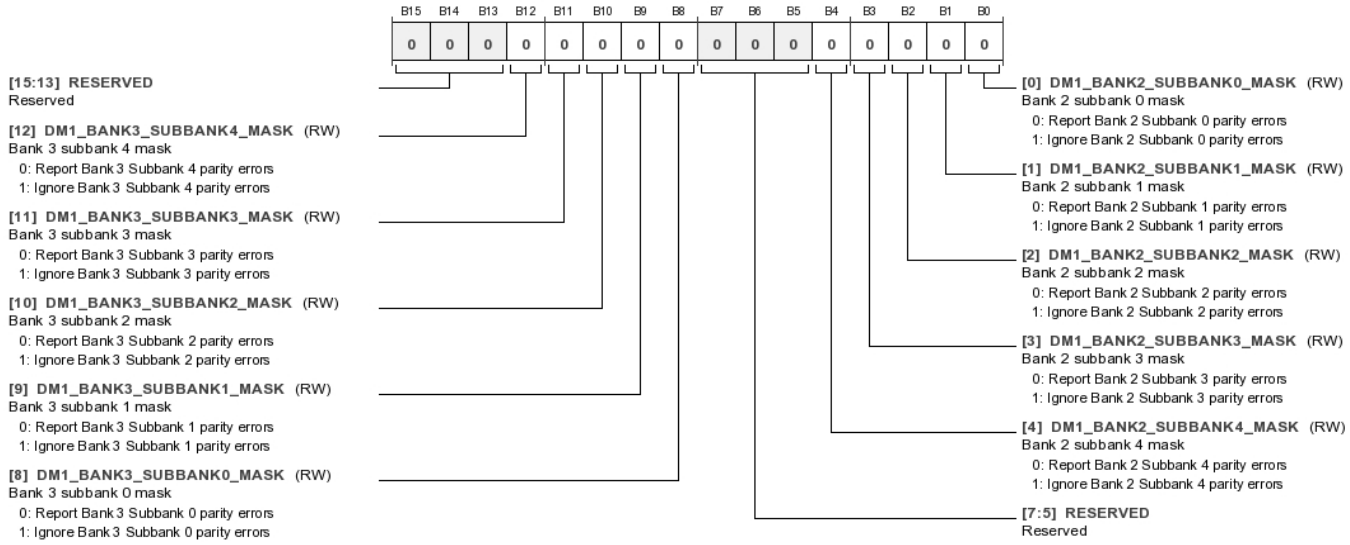
Table 113. Bit Descriptions for PROG_CNTR_MAXLENGTH0

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x0	RW
[7:0]	PROG_MAXLENGTH_MSB		Program counter maximum length, Bits[23:16]	0x00	R

Bits	Bit Name	Settings	Description	Reset	Access
10	DM1_BANK1_SUBBANK2_MASK		Bank 1 Subbank 2 mask.	0x0	RW
		0	Report Bank 1 Subbank 2 parity errors.		
		1	Ignore Bank 1 Subbank 2 parity errors.		
9	DM1_BANK1_SUBBANK1_MASK		Bank 1 Subbank 1 mask.	0x0	RW
		0	Report Bank 1 Subbank 1 parity errors.		
		1	Ignore Bank 1 Subbank 1 parity errors.		
8	DM1_BANK1_SUBBANK0_MASK		Bank 1 Subbank 0 mask.	0x0	RW
		0	Report Bank 1 Subbank 0 parity errors.		
		1	Ignore Bank 1 Subbank 0 parity errors.		
[7:5]	RESERVED		Reserved.	0x0	RW
4	DM1_BANK0_SUBBANK4_MASK		Bank 0 Subbank 4 mask.	0x0	RW
		0	Report Bank 0 Subbank 4 parity errors.		
		1	Ignore Bank 0 Subbank 4 parity errors.		
3	DM1_BANK0_SUBBANK3_MASK		Bank 0 Subbank 3 mask.	0x0	RW
		0	Report Bank 0 Subbank 3 parity errors.		
		1	Ignore Bank 0 Subbank 3 parity errors.		
2	DM1_BANK0_SUBBANK2_MASK		Bank 0 Subbank 2 mask.	0x0	RW
		0	Report Bank 0 Subbank 2 parity errors.		
		1	Ignore Bank 0 Subbank 2 parity errors.		
1	DM1_BANK0_SUBBANK1_MASK		Bank 0 Subbank 1 mask.	0x0	RW
		0	Report Bank 0 Subbank 1 parity errors.		
		1	Ignore Bank 0 Subbank 1 parity errors.		
0	DM1_BANK0_SUBBANK0_MASK		Bank 0 Subbank 0 mask.	0x0	RW
		0	Report Bank 0 Subbank 0 parity errors.		
		1	Ignore Bank 0 Subbank 0 parity errors.		

Panic Mask Parity DM1 Bank [3:2] Register

Address: 0xF46A, Reset: 0x0000, Name: PANIC_PARITY_MASK4



Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DEBOUNCE_VALUE		Debounce circuit setting. These bits configure the duration of the debounce circuitry when the corresponding pin is configured as an input (Bits[3:1] (MP_MODE) = 0b000).	0x0	RW
		0001	0.3 ms debounce.		
		0010	0.6 ms debounce.		
		0011	0.9 ms debounce.		
		0100	5.0 ms debounce.		
		0101	10.0 ms debounce.		
		0110	20.0 ms debounce.		
		0111	40.0 ms debounce.		
		0000	No debounce.		
[3:1]	MP_MODE		Pin mode (when multipurpose function is enabled). These bits select the function of the corresponding pin if it is enabled in multipurpose mode (Bit 0 (MP_ENABLE) = 0b1).	0x0	RW
		000	General-purpose digital input.		
		001	General-purpose input, driven by control port; sends its value to the DSP core, but that value can be overwritten by a direct register write.		
		010	General-purpose output with pull-up.		
		011	General-purpose output without pull-up.		
		100	PDM microphone data input.		
		101	Panic manager error flag output .		
		110	Slave select line for the master SPI port.		
0	MP_ENABLE		Function selection (multipurpose or clock/control). This bit selects whether the corresponding pin is used as a multipurpose pin or as its primary function (which could be either an audio clock or control bus pin).	0x0	RW
		0	Audio clock or control port function enabled; the settings of the MPx_MODE, MPx_WRITE, and MPx_READ registers are ignored.		
		1	Multipurpose function enabled.		

S/PDIF Receiver Validity Bits (Left) Register

Address: 0xF650 to 0xF65B (Increments of 0x1), Reset: 0x0000, Name: SPDIF_RX_VB_LEFT_x

These 12 registers store the 192 validity bits decoded from the left channel of the S/PDIF input stream on the ADAU1463 and ADAU1467.

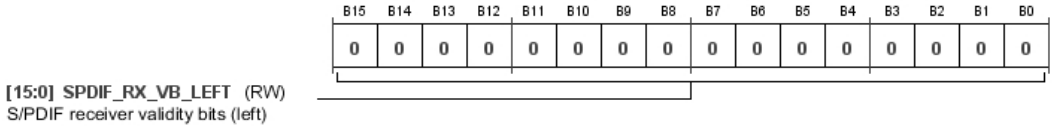


Table 150. Bit Descriptions for SPDIF_RX_VB_LEFT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_RX_VB_LEFT		S/PDIF receiver validity bits (left).	0x0000	R

S/PDIF Receiver Validity Bits (Right) Register

Address: 0xF660 to 0xF66B (Increments of 0x1), Reset: 0x0000, Name: SPDIF_RX_VB_RIGHT_x

These 12 registers store the 192 validity bits decoded from the left channel of the S/PDIF input stream on the ADAU1463 and ADAU1467.

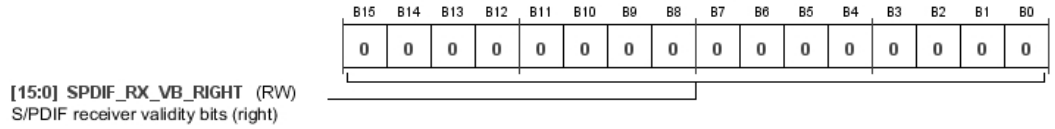


Table 151. Bit Descriptions for SPDIF_RX_VB_RIGHT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_RX_VB_RIGHT		S/PDIF receiver validity bits (right).	0x0000	R

S/PDIF Receiver Parity Bits (Left) Register

Address: 0xF670 to 0xF67B (Increments of 0x1), Reset: 0x0000, Name: SPDIF_RX_PB_LEFT_x

These 12 registers store the 192 parity bits decoded from the left channel of the S/PDIF input stream on the ADAU1463 and ADAU1467.

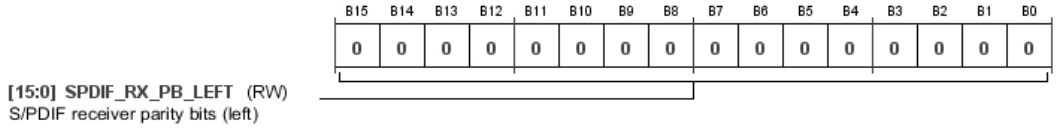


Table 152. Bit Descriptions for SPDIF_RX_PB_LEFT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_RX_PB_LEFT		S/PDIF receiver parity bits (left).	0x0000	R

S/PDIF Receiver Parity Bits (Right) Register

Address: 0xF680 to 0xF68B (Increments of 0x1), Reset: 0x0000, Name: SPDIF_RX_PB_RIGHT_x

These 12 registers store the 192 parity bits decoded from the right channel of the S/PDIF input stream on the ADAU1463 and ADAU1467.

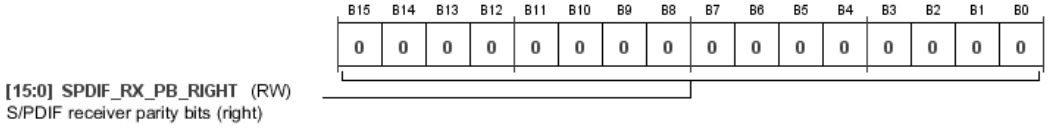


Table 153. Bit Descriptions for SPDIF_RX_PB_RIGHT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_RX_PB_RIGHT		S/PDIF receiver parity bits (right).	0x0000	R

HARDWARE INTERFACING REGISTERS

BCLK Input Pins Drive Strength and Slew Rate Register

Address: 0xF780 to 0xF783 (Increments of 0x1), Reset: 0x0018, Name: BCLK_INx_PIN

These registers configure the drive strength, slew rate, and pull resistors for the BCLK_INx pins. Register 0xF780 corresponds to BCLK_IN0, Register 0xF781 corresponds to BCLK_IN1, Register 0xF782 corresponds to BCLK_IN2, and Register 0xF783 corresponds to BCLK_IN3.

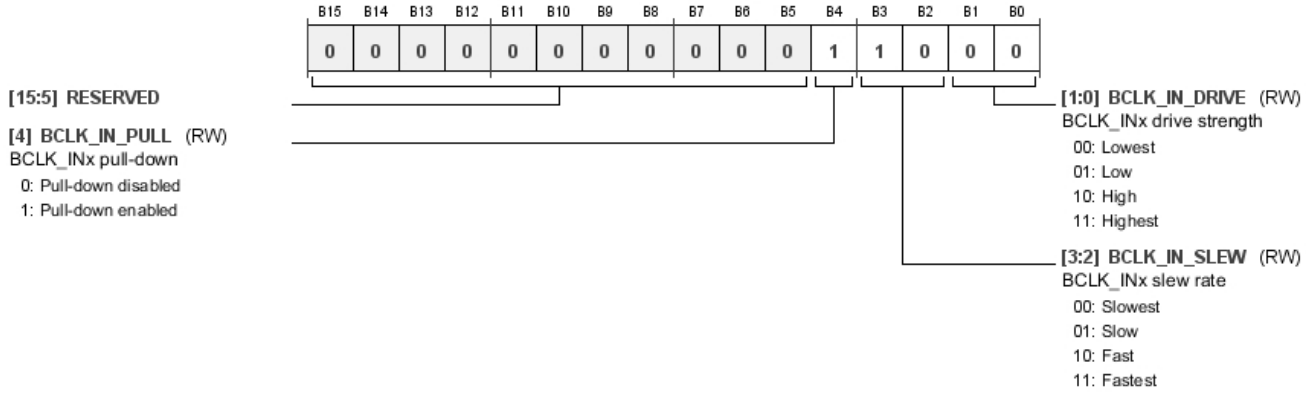


Table 165. Bit Descriptions for BCLK_INx_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED		Reserved.	0x0	RW
4	BCLK_IN_PULL		BCLK_INx pull-down.	0x1	RW
		0	Pull-down disabled.		
		1	Pull-down enabled.		
[3:2]	BCLK_IN_SLEW		BCLK_INx slew rate.	0x2	RW
		00	Slowest.		
		01	Slow.		
		10	Fast.		
		11	Fastest.		
[1:0]	BCLK_IN_DRIVE		BCLK_INx drive strength.	0x0	RW
		00	Lowest.		
		01	Low.		
		10	High.		
		11	Highest.		

SDA_M/MISO_M/MP3 Pin Drive Strength and Slew Rate Register

Address: 0xF79E, Reset: 0x0008, Name: MISO_SDA_M_PIN

This register configures the drive strength, slew rate, and pull resistors for the SDA_M/MISO_M/MP3 pin.

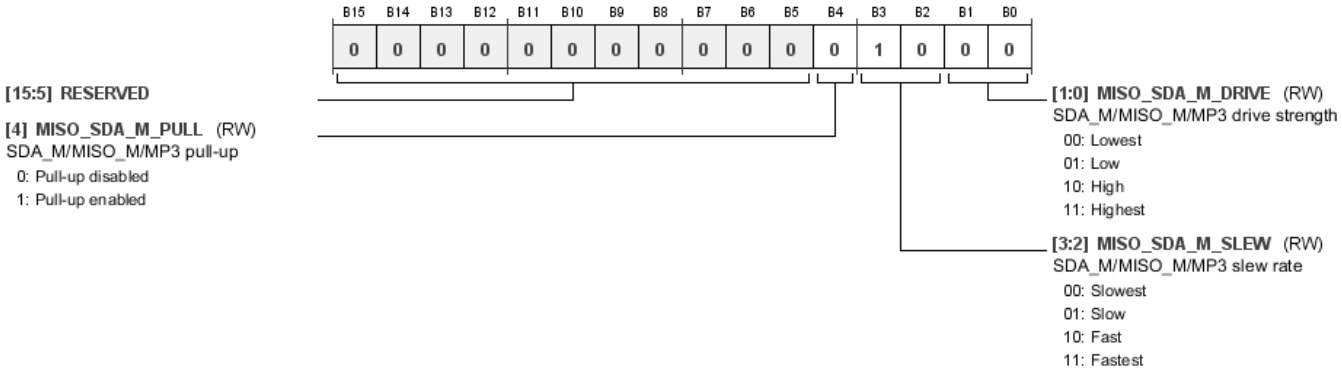


Table 177. Bit Descriptions for MISO_SDA_M_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED		Reserved.	0x0	RW
4	MISO_SDA_M_PULL		SDA_M/MISO_M/MP3 pull-up.	0x0	RW
		0	Pull-up disabled.		
		1	Pull-up enabled.		
[3:2]	MISO_SDA_M_SLEW		SDA_M/MISO_M/MP3 slew rate.	0x2	RW
		00	Slowest.		
		01	Slow.		
		10	Fast.		
		11	Fastest.		
[1:0]	MISO_SDA_M_DRIVE		SDA_M/MISO_M/MP3 drive strength.	0x0	RW
		00	Lowest.		
		01	Low.		
		10	High.		
		11	Highest.		