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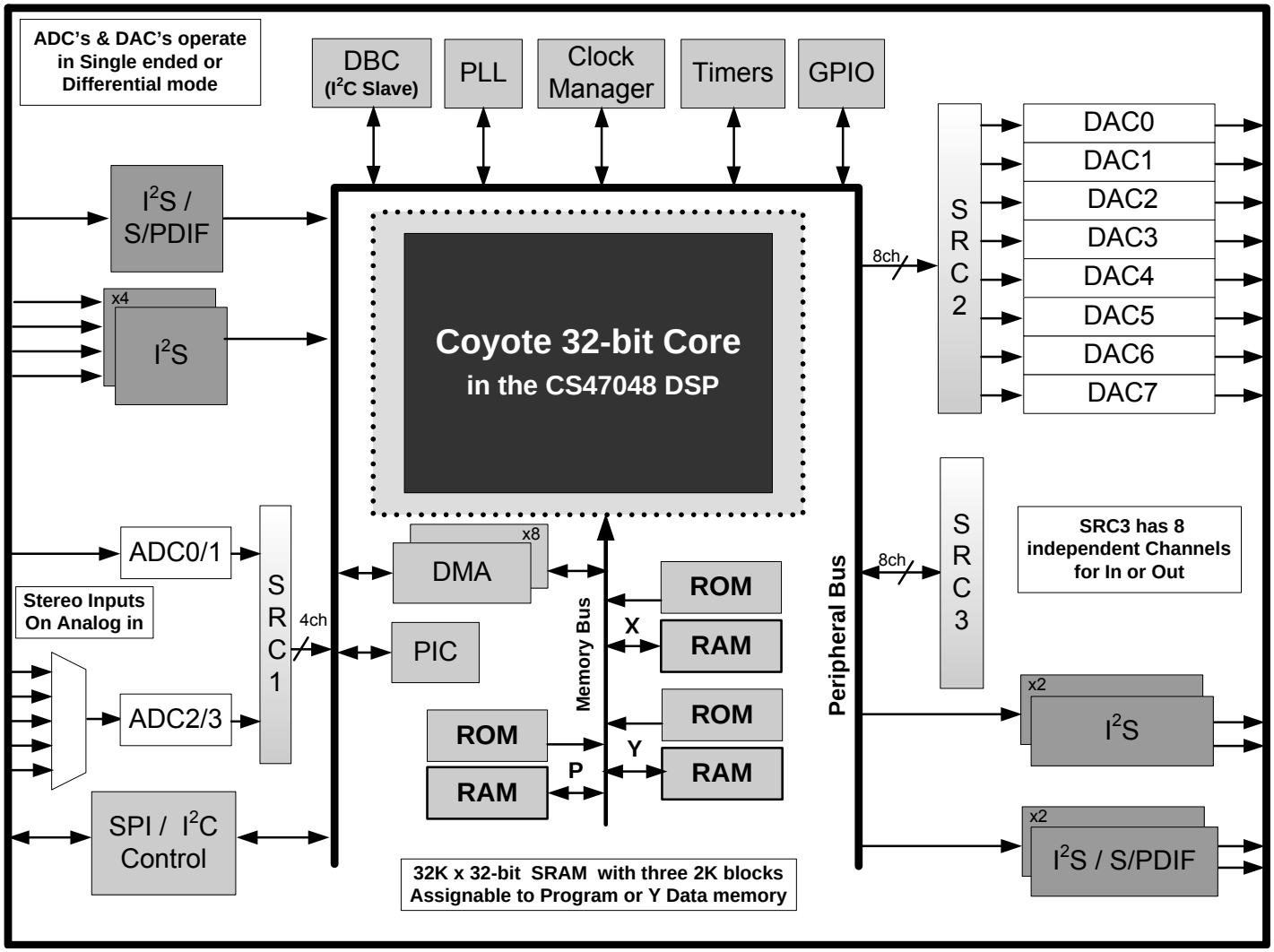
Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	I²C, SPI
Clock Rate	150MHz
Non-Volatile Memory	-
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/cs47024c-cqzr



CS47048 Block Diagram

3 Code Overlays

The suite of software available for the CS470xx family consists of an operating system (OS) and a library of overlays. The software components for the CS470xx family include:

1. *OS/Kernel*—Encompasses all non-audio processing tasks, including loading data from external serial memory, processing host messages, calling audio-processing subroutines, error concealment, etc.
2. *Decoder*—Any module that performs a compressed audio decode on IEC61937-packed data delivered via S/PDIF Rx or I²S input, such as Dolby Digital (AC3).
3. *Matrix-processor*—Any Module that performs a matrix decode on PCM data to produce more output channels than input channels (2Æn channels). Examples are Dolby® Pro Logic® IIx and SRS Circle Surround II®. Generally speaking, these modules increase the number of valid channels in the audio I/O buffer.
4. *Virtualizer-processor*—Any module that encodes PCM data into fewer output channels than input channels (nÆ2 channels) with the effect of providing “phantom” speakers to represent the physical audio channels that were eliminated. Examples are Dolby Headphone® 2 and Dolby® Virtual Speaker® 2. Generally speaking, these modules reduce the number of valid channels in the audio I/O buffer.
5. *Post-processors*—Any module that processes audio I/O buffer PCM data. Examples are bass management, audio manager, tone control, EQ, delay, customer-specific effects, and any post-processing algorithms available for the CS470xx DSP.

The bulk of standard overlays are stored in ROM within the CS470xx, but a small image is required to configure the overlays and boot the DSP. This small image can either be stored in an external serial flash/EEPROM, or downloaded via a host controller through the SPI/I²C serial port.

The overlay structure reduces the time required to reconfigure the DSP when a processing change is requested. Each overlay can be reloaded independently without disturbing the other overlays. For example, when a different post-processor is selected, the OS, does not need to be reloaded—only the new post-processor.

Table 3-1 lists the different configuration options available. Refer to the CS470xx Firmware User’s Manual for the latest listing of application codes and Cirrus Framework™ modules available. See Table 3-2, which provides a summary of the available channels for each type of input and output communication mode for members of the CS470xx family of DSPs.

Table 3-1. CS470xx Device Selection Guide

Features	CS47048-CQZ CS47048-DQZ	CS47028-CQZ CS47028-DQZ	CS47024-CQZ CS47024-DQZ
Primary Applications	• 4-In/8-Out Car Audio • High-end Digital TV • Dual Source/Dual Zone	• 2-In/8-Out Car Audio • Sound Bar • DVD Receiver	• 2-In/4-Out Car Audio • Digital TV • Portable Audio Docking Station • Portable DVD • DVD Mini / Receiver • Multimedia PC Speakers
Package	100-pin LQFP with Exposed Pad		
DSP Core	Cirrus Logic 32-bit Core		
SRAM	32K x 32-bit SRAM with three 2K blocks x 32-bit SRAM, assignable to either Y data or program memory		
Integrated DAC and ADC	• 2 Channels of ADC input: with integrated 5:1 analog mux • 2 additional channels of ADC input: without mux • 8 channels of DAC output	• 2 channels of ADC input: with integrated 5:1 analog mux • 8 channels of DAC output	• 2 channels of ADC input: with integrated 5:1 analog mux • 4 channels of DAC output
Configurable Serial Audio Inputs/Outputs	• Integrated 192 kHz S/PDIF Rx, 2 Integrated 192 kHz S/PDIF Tx • I2S support for 32-bit Samples @ 192 kHz • TDM Input modes (Up to 8 channels) • TDM Output modes (Up to 8 channels)		
Supports Different Fs Sample Rates	• Integrated hardware SRC blocks for all ADC and DAC channels • Additional 8-channel hardware SRC block • Dual-domain Fs on inputs (I2S and S/PDIF Rx) • Output can be master or slave		
Other Features	• Integrated Clock Manager/PLL with flexibility to operate from internal PLL, external crystal, external oscillator • Host Control and Boot via SPI/I²C Serial Interface • DSP Tool Set w/ Private Keys Protect Customer IP • Configurable GPIOs and External Interrupts • Hardware Watchdog Timer		

Table 3-2. CS470xx Channel Count

Product	PCM/TDM In[1]	TDM Out[1]	PCM Out	ADC with 5:1 Input Mux	ADC without Mux	DAC Out	S/PDIF In (Stereo Pairs)	S/PDIF Out (Stereo Pairs)
CS47048	• Up to 5 I2S lines, 2 channels per line or • 1 TDM line, up to 8 channels per line.	Up to 8 channels	**8**	**2**	**2**	**8**	**1**	**2**
CS47028	• Up to 5 I2S lines, 2 channels per line or • 1 TDM line, up to 8 channels per line.	Up to 8 channels	**8**	**2**	**0**	**8**	**1**	**2**
CS47024	• Up to 5 I2S lines, 2 channels per line or • 1 TDM line, up to 8 channels per line.	Up to 8 channels	**8**	**2**	**0**	**4**	**1**	**2**

1. Contact your Cirrus Logic representative to determine the TDM modes that are supported. The CS470xx can support up to 8 channels per line, but the DSP software provided for the IC can restrict this capability.

4 Hardware Functional Description

The CS470xx family, which includes the CS47048, CS47028, and CS47024 DSPs, is a true system-on-a-chip that combines a powerful 32-bit DSP engine with analog/digital audio inputs and analog/digital audio outputs. It can be integrated into a complex multi-DSP processing system, or stand alone in an audio product that requires analog-in and analog-out. A top level block diagram for the CS47048, CS47028, and CS47024 products are shown in Fig. 4-1, Fig. 4-2, and Fig. 4-3 respectively.

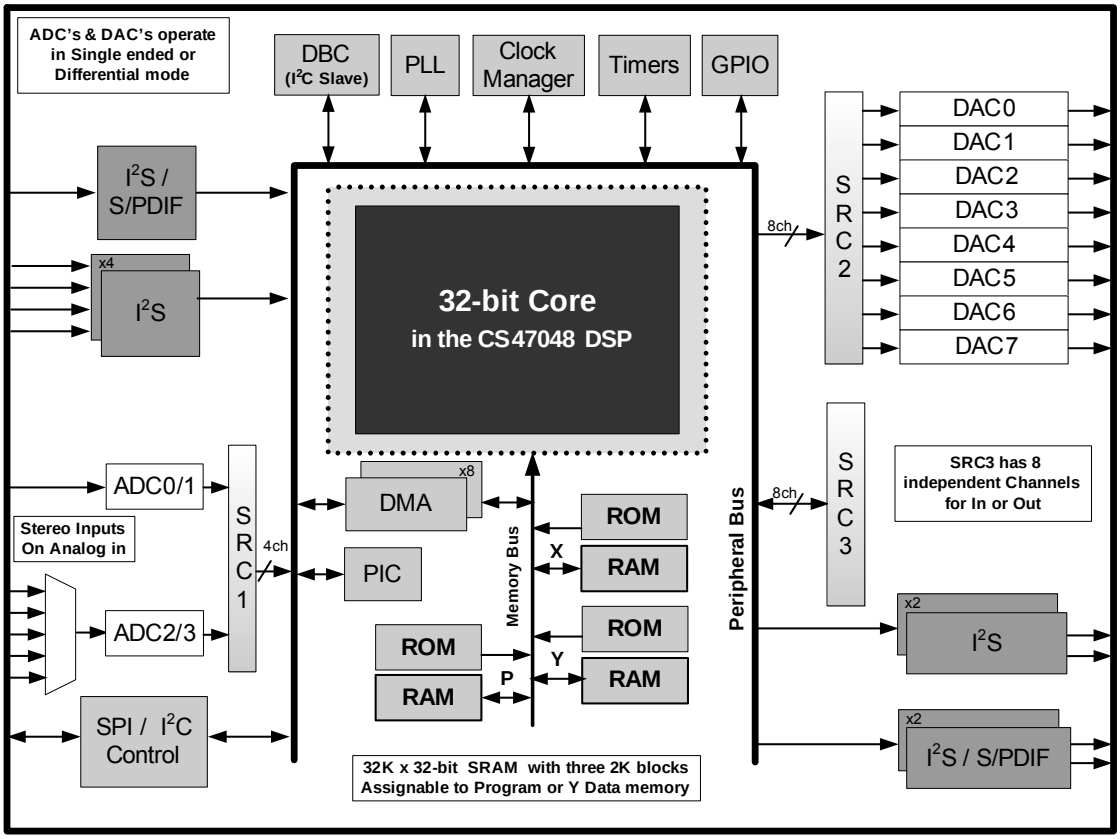


Figure 4-1. CS47048 Top-level Block Diagram

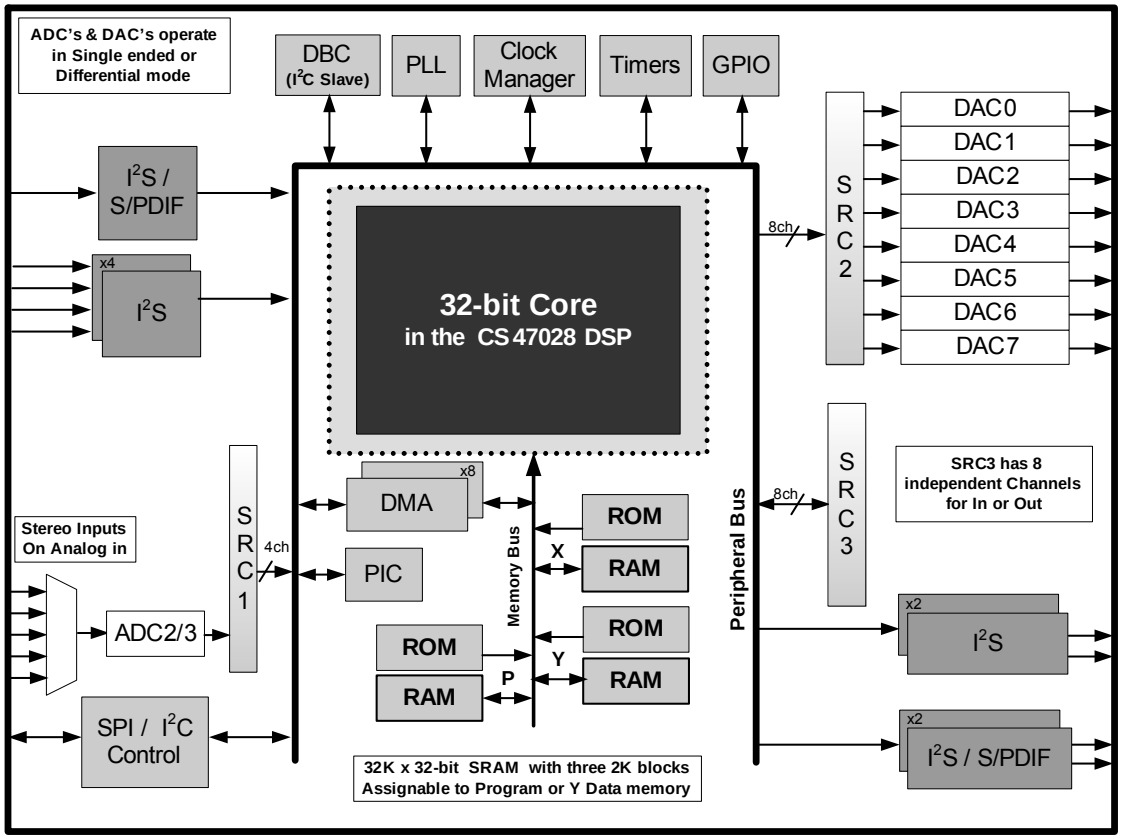


Figure 4-2. CS47028 Top-level Block Diagram

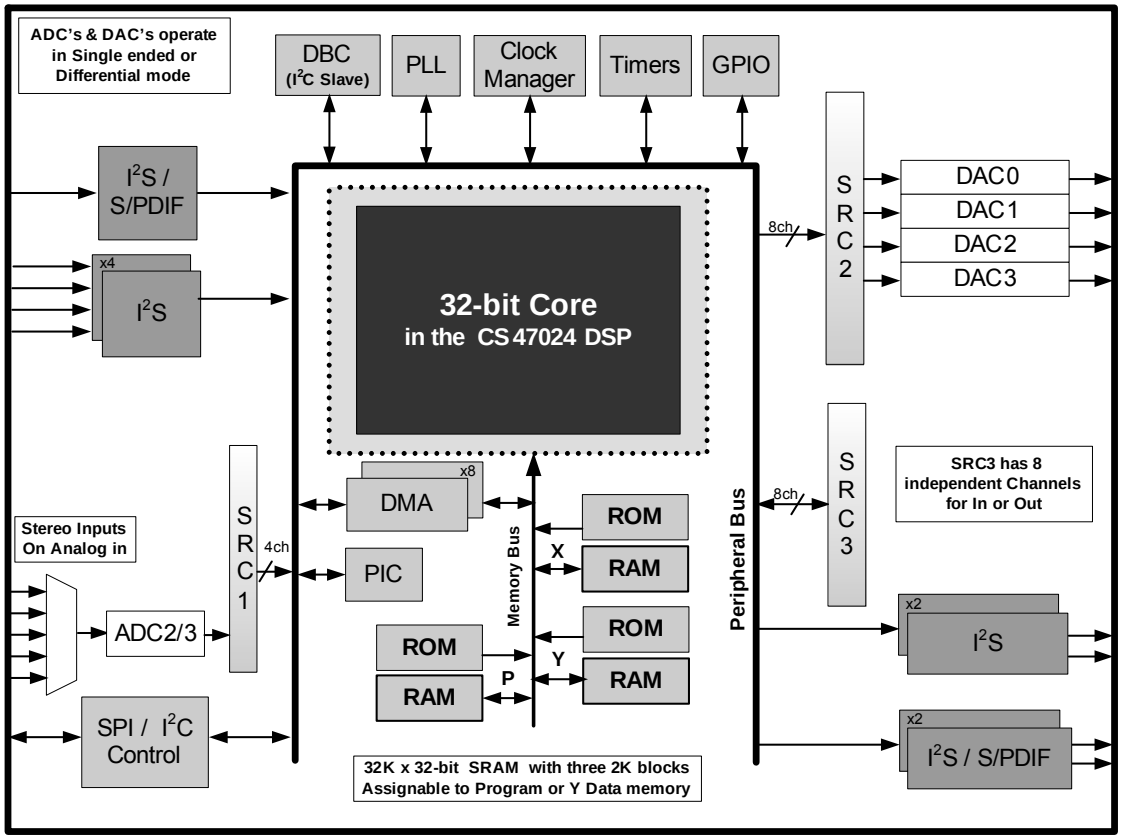


Figure 4-3. CS47024 Top-level Block Diagram

4.3.2 Digital to Analog Converter Port (DAC)

The DACs in the CS470xx devices feature dynamic range performance in excess of 100 dB. See Section 5.17 for more details on CS470xx DAC performance. The CS47024 device supports four simultaneous channels of digital-to-analog conversion. The CS47028 and CS47048 devices provide eight simultaneous channels of digital-to-analog conversion. The DACs have voltage mode outputs that can be connected either as single-ended or differential signals. The conversions are performed with Fs=96 kHz.

4.3.3 Digital Audio Input Port (DAI)

The input capabilities for each version of the CS470xx are summarized in Table 3-1 and Table 3-2.

Up to five DAI ports are available. Two of the DAI ports can be programmed to implement other functions. If the SPI mode is used, the DAI_DATA4 pin becomes the SCP_CS input. The integrated S/PDIF receiver can be used to take over the DAI_DATA3 pin.

The DAI port PCM inputs have a single slave-only clock domain. The S/PDIF receiver, if used, is a separate clock domain. The output of the S/PDIF Rx can then be converted through one of the internal SRC blocks to synchronize with the PCM input. The sample rate of the input clock domains can be determined automatically by the DSP, off-loading the task of monitoring the S/PDIF Rx from the host. A time-stamping feature provides the ability to also sample-rate convert the input data via software.The DAI port supports PCM format with word lengths up to 32 bits and sample rates as high as 192 kHz.

The DAI also supports a time division multiplexed (TDM) mode that packs up to 10 PCM audio channels on a single data line.

4.3.4 S/PDIF RX Input Port (DAI)

One of the PCM pins of the DAI can also be used as a DC-coupled, TTL-level S/PDIF Rx input capable of receiving and demodulating bi-phase encoded S/PDIF signals with Fs $\leq$ 192 kHz.

4.3.5 Digital Audio Output Port (DAO)

DAO port supports PCM resolutions of up to 32-bits. The port supports sample rates (Fs) as high as 192 kHz. The port can be configured as an independent clock domain mastered by the DSP, or as a clock slave if an external MCLK or SCLK/LRCLK source is available.

The DAO also supports a time division multiplexed (TDM) mode, that packs up to 8 channels of PCM audio on a single data line.

4.3.6 S/PDIF TX Output Port (DAO)

Two of the serial audio pins can be re-configured as S/PDIF TX pins that drive a bi-phase encoded S/PDIF signal (data with embedded clock on a single line).

4.3.7 Sample Rate Converters (SRC)

All CS470xx devices have at least two internal hardware SRC modules. One is directly associated with the ADCs and normally serves to convert data from the 96 kHz sampling rate of the ADCs to another Fs appropriate for mixing with other audio in the system.

The other SRC module is directly associated with the DACs and normally serves to convert data from the DSP into the 96 kHz sample rate needed by the DACs.

The CS47024, CS47028, and CS47048 devices have an additional stand-alone 8-channel SRC module. This SRC module can be used to make independent input clock domains synchronous (different Fs on PCM input and S/PDIF Rx).

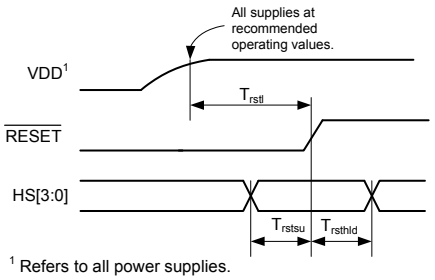


Figure 5-1. $\overline{\text{RESET}}$ Timing at Power-on

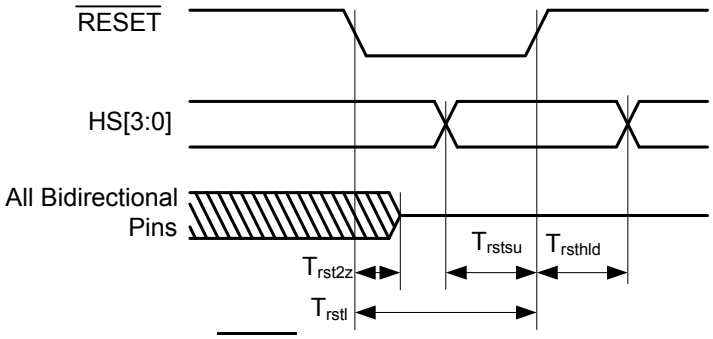


Figure 5-2. $\overline{\text{RESET}}$ Timing after Power is Stable

5.7 Digital Switching Characteristics–XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency[1]	F_{xtal}	12.288	24.576	MHz
XTI period	T_{clki}	41	81	ns
XTI high time	T_{clkih}	13.3	—	ns
XTI low time	T_{clkil}	13.3	—	ns
External Crystal Load Capacitance (parallel resonant)[2]	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR	—	50	Ω

1. Part characterized with the following crystal frequency values: 12.288 and 24.576 MHz.
2. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals that require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

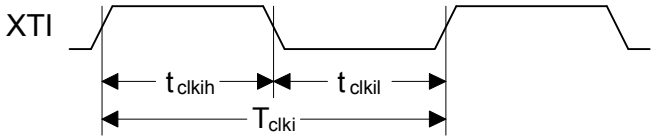


Figure 5-3. XTI Timing

5.8 Digital Switching Characteristics–Internal Clock

Parameter	Symbol	Min (2-layer Boards)	Min (4-layer Boards)	Max (2-layer Boards)	Max (4-layer Boards)	Unit
Internal DSP_CLK frequency[1]	F_{dclk}	(See Footnote 2)				MHz
CS47048-CQZ		F_{xtal}		147	147	
CS47048-DQZ		F_{xtal}		131	147	
CS47028-CQZ		F_{xtal}		147	147	
CS47028-DQZ		F_{xtal}		131	147	
CS47024-CQZ		F_{xtal}		147	147	
CS47024-DQZ		F_{xtal}		131	147	
Internal DSP_CLK period[1]	DCLKP					ns
CS47048-CQZ		6.8	6.8	$1/F_{xtal}$		
CS47048-DQZ		7.6	6.8	$1/F_{xtal}$		
CS47028-CQZ		6.8	6.8	$1/F_{xtal}$		
CS47028-DQZ		7.6	6.8	$1/F_{xtal}$		
CS47024-CQZ		6.8	6.8	$1/F_{xtal}$		
CS47024-DQZ		7.6	6.8	$1/F_{xtal}$		

1. After initial power-on reset, $F_{dclk} = F_{xtal}$. After initial kick-start commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.
2. See Section 5.7. for all references to F_{xtal}.

5.9 Digital Switching Characteristics–Serial Control Port–SPI Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
SCP_CLK frequency[1]	f_{spisck}	—	—	25	MHz
$\overline{\text{SCP\_CS}}$ falling to SCP_CLK rising	t_{spicss}	24	—	—	ns
SCP_CLK low time	t_{spickl}	20	—	—	ns
SCP_CLK high time	t_{spickh}	20	—	—	ns
Setup time SCP_MOSI input	t_{spidsu}	5	—	—	ns
Hold time SCP_MOSI input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MISO output valid	t_{spidov}	—	—	11	ns
SCP_CLK falling to $\overline{\text{SCP\_IRQ}}$ rising	$t_{spiirqh}$	—	—	27	ns
$\overline{\text{SCP\_CS}}$ rising to $\overline{\text{SCP\_IRQ}}$ falling	$t_{spiirql}$	0	—	—	ns
SCP_CLK low to $\overline{\text{SCP\_CS}}$ rising	t_{spicsh}	24	—	—	ns
$\overline{\text{SCP\_CS}}$ rising to SCP_MISO output high-Z	$t_{spicsdz}$	—	20	—	ns
SCP_CLK rising to $\overline{\text{SCP\_BSY}}$ falling	$t_{spicbsyl}$	—	3*DCLKP+20	—	ns

1. f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port can be limited by the firmware application. Flow control using the $\overline{\text{SCP\_BSY}}$ pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is $F_{xtal}/3$.

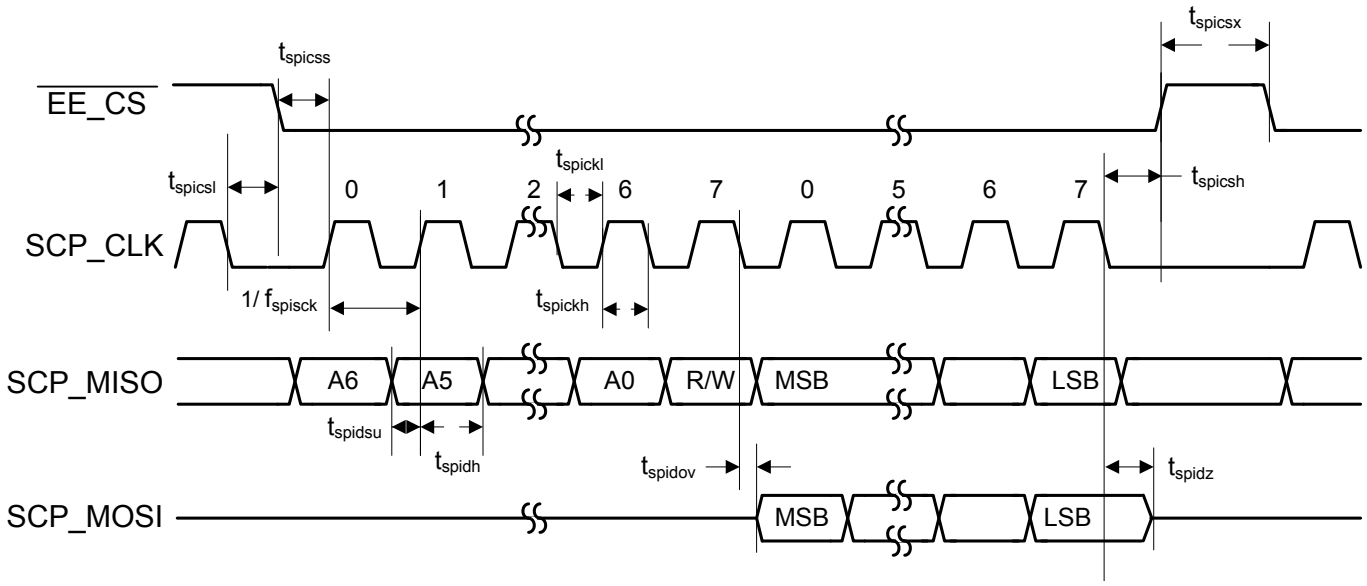


Figure 5-5. Serial Control Port–SPI Master Mode Timing

5.11 Digital Switching Characteristics–Serial Control Port I2C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	—	—	400	kHz
SCP_CLK rise time	t_{iicr}	—	—	150	ns
SCP_CLK fall time	t_{iicf}	—	—	150	ns
SCP_CLK low time	t_{iicckl}	1.25	—	—	µs
SCP_CLK high time	t_{iicckh}	1.25	—	—	µs
SCP_CLK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25	—	—	µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	—	—	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	—	—	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	—	—	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	110	—	—	ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	100	—	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	—	—	18	ns
SCP_CLK falling to $\overline{\text{SCP\_IRQ}}$ rising	$t_{iicirqh}$	—	—	3*DCLKP+40	ns
NAK condition to $\overline{\text{SCP\_IRQ}}$ low	$t_{iicirql}$	—	3*DCLKP+20	—	ns
SCP_CLK rising to $\overline{\text{SCB\_BSY}}$ low	$t_{iicbsyl}$	—	3*DCLKP+20	—	ns

1. f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port can be limited by the firmware application. Flow control using the $\overline{\text{SCP\_BSY}}$ pin should be implemented to prevent overflow of the input data buffer.

I2C Slave Address = 0x82

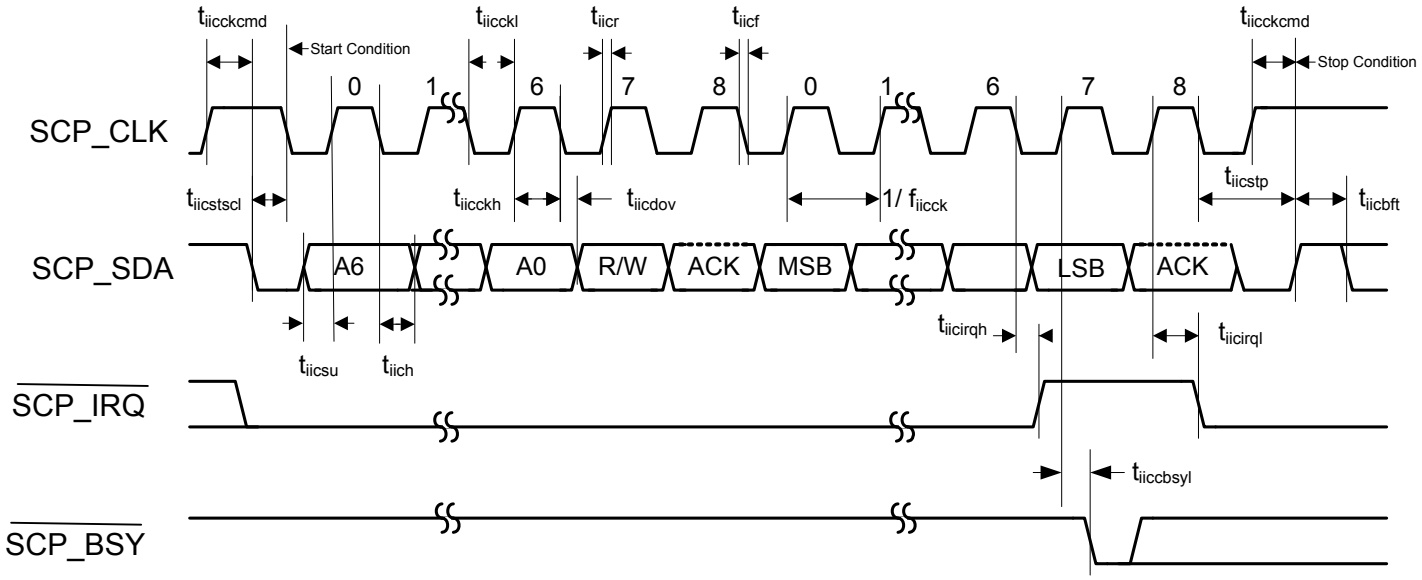


Figure 5-6. Serial Control Port–I2C Slave Mode Timing

5.12 Digital Switching Characteristics–Serial Control Port–I2C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency[1]	f_{iicck}	—	400	kHz
SCP_CLK rise time	t_{iicr}	—	150	ns
SCP_CLK fall time	t_{iicf}	—	150	ns
SCP_CLK low time	t_{iicckl}	1.25	—	µs
SCP_CLK high time	t_{iicckh}	1.25	—	µs
SCP_CLK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25	—	µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	—	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	—	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	—	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	110	—	ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	100	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	—	36	ns

1. f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port can be limited by the firmware application.

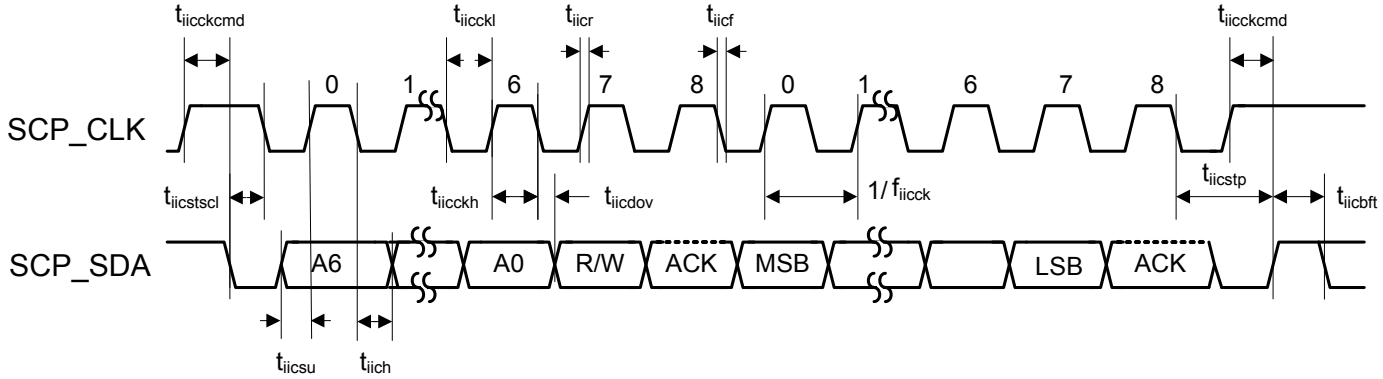


Figure 5-7. Serial Control Port–I2C Master Mode Timing

5.13 Digital Switching Characteristics–Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	20	—	ns
DAI_SCLK duty cycle	—	45	55	%
Setup time DAI_DATAn	t_{daidsu}	8	—	ns
Hold time DAI_DATAn	t_{daidh}	5	—	ns

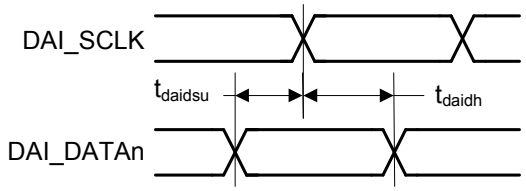


Figure 5-8. Digital Audio Input (DAI) Port Timing Diagram

5.14 Digital Switching Characteristics–Digital Audio Output Port

Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	20	—	ns
DAO_MCLK duty cycle	—	45	55	%
DAO_SCLK period for Master or Slave mode[1]	$T_{daosclk}$	20	—	ns
DAO_SCLK duty cycle for Master or Slave mode[1]	—	40	60	%
Master Mode (Output A1 Mode)[1,2]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO MCLK as an input	$t_{daomsck}$	—	19	ns
DAO_LRCLK to DAO_SCLK inactive edge[3]. See Fig. 5-9.	$t_{daomlrts}$	—	8	ns
DAO_SCLK inactive edge[3] to DAO_LRCLK. See Fig. 5-10.	$t_{daomstlr}$	—	8	ns
DAO_DATA[3:0] delay from DAO_SCLK inactive edge[3]	t_{daomdy}	—	8	ns
Slave Mode (Output A0 Mode)[4]				
DAO_SCLK active edge to DAO_LRCLK transition. See Fig. 5-11.	$t_{daosstlr}$	10	—	ns
DAO_LRCLK transition to DAO_SCLK active edge. See Fig. 5-12.	$t_{daoslrts}$	10	—	ns
DAO_Dx delay from DAO_SCLK inactive edge	t_{daosdv}	—	11	ns

1. Master mode timing specifications are characterized, not production tested.
2. Master mode is defined as the CS47048 driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.
3. The DAO_LRCLK transition can occur on either side of the edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.
4. Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.

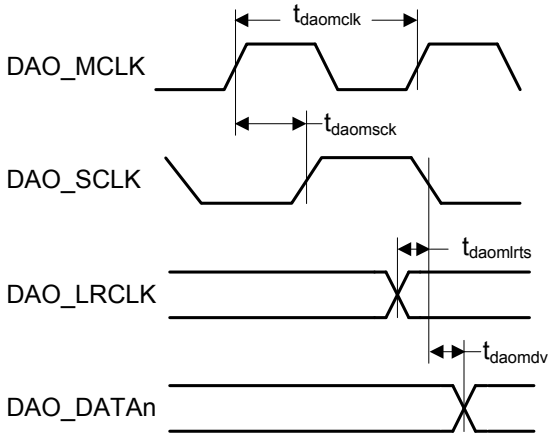


Figure 5-9. DAO_LRCLK Transition before DAO_SCLK Inactive Edge

5.16.2 Analog Input Characteristics (Automotive)

Test Conditions (unless otherwise specified): TA = –40–85°C; VDD = 1.8V±5%, VDDA (VA) = 3.3V±5%; kHz sine wave driven through the passive input filter (R_i = 10 kΩ) in Fig. 5-13 or Fig. 5-14; DSP running test application; Measurement Bandwidth is 10 Hz–20 kHz.

	Differential			Single-ended			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Fs = 96 kHz							
Dynamic Range[1,6,7] A-weighted Unweighted 40 kHz bandwidth unweighted	 97 94 —	 105 102 99	 — — —	 94 91 —	 102 99 96	 — — —	 dB dB dB
Total Harmonic Distortion + Noise[6,7] –1 dB –20 dB –60 dB 40 kHz bandwidth –1 dB	 — — — —	 –98 –82 –42 –90	 –90 — — —	 — — — —	 –95 –79 –39 –90	 –87 — — —	 dB dB dB dB
AIN_1A/B Interchannel Isolation[10]	—	95	—	—	95	—	dB
AID_[2.6]A/B MUX Interchannel Isolation	—	95	—	—	95	—	dB
DC Accuracy							
Interchannel Gain Mismatch	—	0.1	—	—	0.1	—	dB
Gain Drift	—	±120	—	—	±120	—	ppm/°C
Analog Input							
Full-scale Input Voltage[2,3]	3.3	3.7•VA	3.9	1.65	1.85•VA	1.95	V_{PP}
Differential Input Impedance[4]	—	400	—	—	—	—	Ω
Single-ended Input Impedance[5]	—	—	—	—	200	—	Ω
Common Mode Rejection Ratio (CMRR)[8]	—	60	—	—	—	—	dB
Parasitic Load Capacitance (C_L)[9]	—	—	20	—	—	20	pF

1. dB units referred to the typical full-scale voltage.
2. These full-scale values were measured with R_i=10k for both the single-ended and differential mode input circuits.
3. The full-scale voltage can be changed by scaling R_i.
   Differential Full-Scale (Vpp) = 3.7*VDDA*(Ri+200)/(10k+200)
   Single-Ended Full-Scale (Vpp) = 1.85*VDDA*(Ri+200)/(10k+200)
4. Measured between AIN_xx+ and AN_xx–.
5. Measured between AIN_xx+ and AGND.
6. Decreasing full-scale voltage by reducing R_i causes the noise floor to increase.
7. Common mode input current should be kept to less than ±160uA to avoid performance degradation: $|(I_{ip}+I_{in})/2| < 160uA$. This corresponds to ±1.6V for R_i=10 kΩ in the differential case.
8. This number was measured using perfectly matched external resistors (R_i). Mismatch in the external resistors typically reduces CMRR by 20 log ($|\Delta R_i|/R_i + 0.001$).
9. C_L represents the parasitic load capacitance between R_i on the input circuit and the input pin of the CS47048 package.
10. This measurement is not applicable to the CS47028 and CS47024 devices.

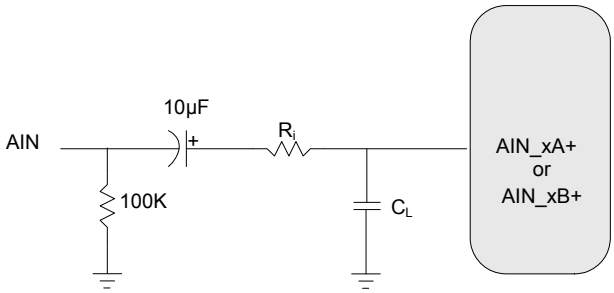


Figure 5-13. ADC Single-ended Input Test Circuit

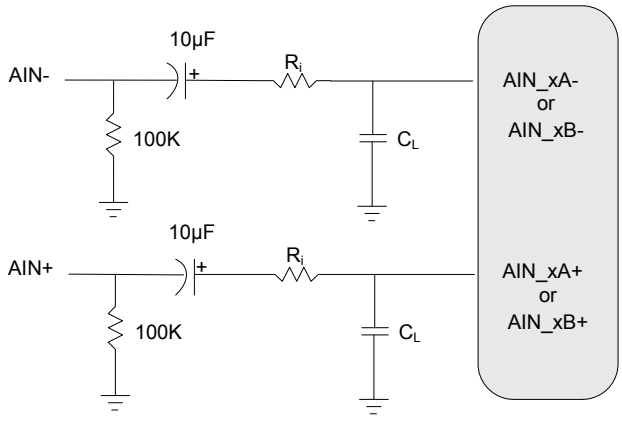


Figure 5-14. ADC Differential Input Test Circuit

5.16.3 ADC Digital Filter Characteristics

Parameter[1,2]	Min	Typ	Max	Unit
Fs = 96 kHz				
Passband (Frequency Response) to –0.1 dB corner	0	—	0.4896	Fs
Passband Ripple	—	—	0.08	dB
Stopband	0.5688	—	—	Fs
Stopband Attenuation	70	—	—	dB
Total Group Delay	—	12/Fs	—	s
High-pass Filter Characteristics				
Frequency Response: –3.0 dB –0.13 dB	 — —	 1 20	 — —	 Hz Hz
Phase Deviation @ 20 Hz	—	10	—	Deg
Passband Ripple	—	—	0	dB
Filter Settling Time	—	10^5/Fs	0	s

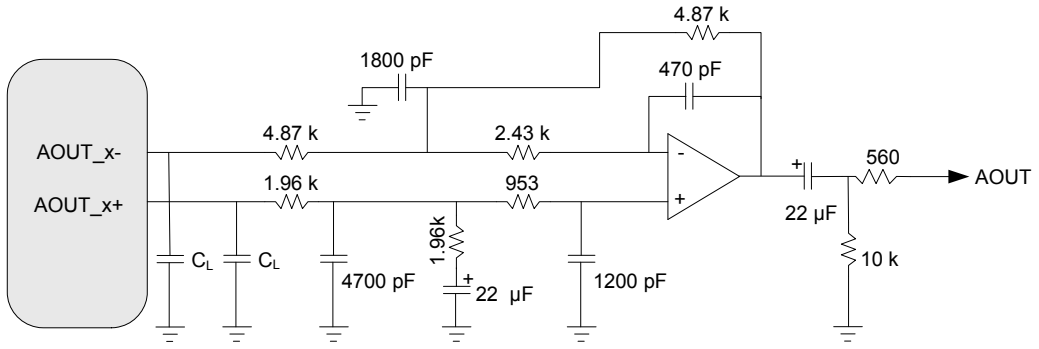
1. Filter response is guaranteed by design.
2. Response is clock-dependent and scales with Fs.

5.17 DAC Characteristics

5.17.1 Analog Output Characteristics (Commercial)

Test Conditions (unless otherwise specified): TA = 0–+70°C; VDD = 1.8V±5%, VDDA(VA) = 3.3V±5%; 1 kHz sine wave driven through a filter shown in Fig. 5-15 or Fig. 5-16; DSP running test application; Measurement Bandwidth is 20 Hz–20 kHz.

	Differential			Single-ended			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Fs = 96 kHz							
Dynamic Range A-weighted Unweighted	 102 99	 108 105	 — —	 99 96	 105 102	 — —	 dB dB
Total Harmonic Distortion + Noise 0 dB –20 dB –60 dB	 — — —	 –98 –88 –48	 –90 — —	 — — —	 –95 –85 –45	 –87 — —	 dB dB dB
Interchannel Isolation (1 kHz)	—	95	—	—	95	—	dB



P output: $R_L = 1.96k + ([2\pi F*4700pF]^{-1} || (1.96k + [2\pi F*22\mu F^{-}]^{-1}) || (953 + [2\pi F*1200pF]^{-1}))$

N output: $R_L = 4.87k + ([2\pi F*1800pF]^{-1} || ((2.43k + [2\pi F*470pF]^{-1}) || 4.87k))$

Figure 5-16. DAC Differential Output Test Circuit

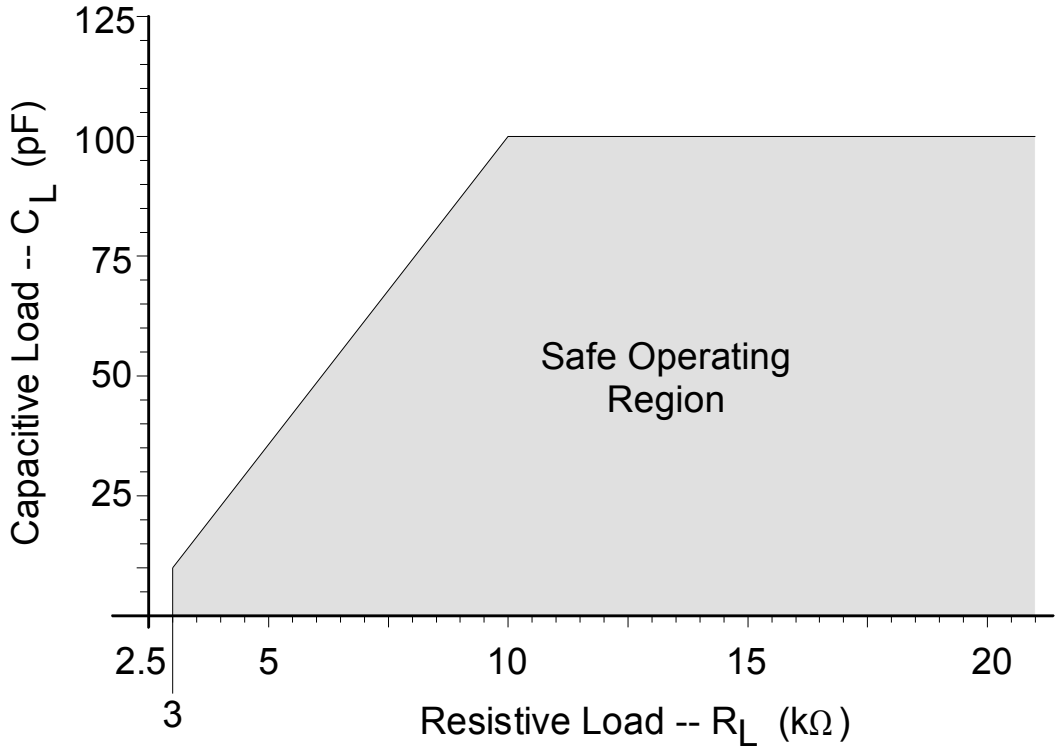


Figure 5-17. Maximum Loading

5.17.3 Combined DAC Interpolation and On-chip Analog Filter Response

Parameter	Min	Typ	Max	Unit
Passband (Frequency Response) to 0.22 dB corner to –3 dB corner	 0 0	 — —	 0.4125 0.4979	 Fs Fs
Frequency Response 10 Hz–20 kHz	–0.02	—	+0.02	dB
StopBand	0.5465	—	—	Fs
StopBand Attenuation	100	—	—	dB
Group Delay	—	10/Fs	—	s

6 Ordering Information

The CS470xx DSP part numbers are described as follows:

Example:
CS47048I-XYZR
where
I–ROM ID Letter
X–Product Grade
Y–Package Type
Z–Lead (Pb) Free
R–Tape and Reel Packaging

Table 6-1. Ordering Information

Part No.	Grade	Temp. Range	Package
CS47048C-CQZ	Commercial	0–+70°C	100-pin LQFP
CS47048C-DQZ	Automotive	–40–+85°C	
CS47048C-EQZ	Extended Automotive	–40–+105°C	
CS47028C-CQZ	Commercial	0–+70°C	
CS47028C-DQZ	Automotive	–40–+85°C	
CS47028C-EQZ	Extended Automotive	–40–+105°C	
CS47024C-CQZ	Commercial	0–+70°C	
CS47024C-DQZ	Automotive	–40–+85°C	
CS47024C-EQZ	Extended Automotive	–40–+105°C	

Note: Contact the factory for availability of the –D (automotive grade) package.

7 Environmental, Manufacturing, and Handling Information

Table 7-1. Environmental, Manufacturing, and Handling Information

Model Number	Peak Reflow Temp.	MSL[1] Rating	Max Floor Life
CS47048C-CQZ	260° C	3	7 days
CS47048C-DQZ			
CS47048C-EQZ			
CS47028C-CQZ	260° C	3	7 days
CS47028C-DQZ			
CS47028C-EQZ			
CS47024C-CQZ	260° C	3	7 days
CS47024C-DQZ			
CS47024C-EQZ			

1. Moisture Sensitivity Level as specified by IPC/JEDEC J-STD-020.

8.2 CS47028, 100-pin LQFP Pinout Diagram

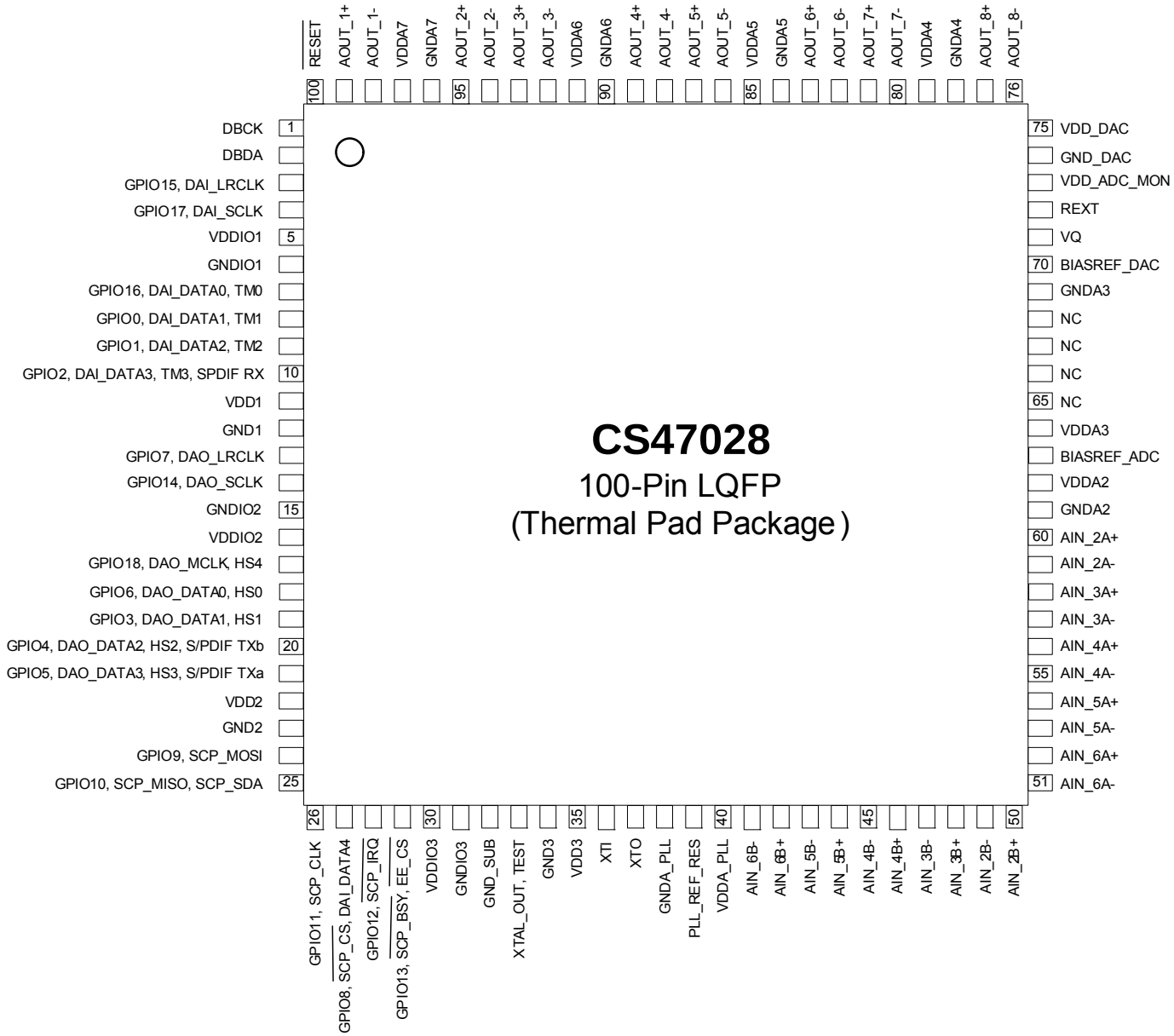


Figure 8-2. CS47028 Pinout Diagram

8.3 CS47024, 100-pin LQFP Pinout Diagram

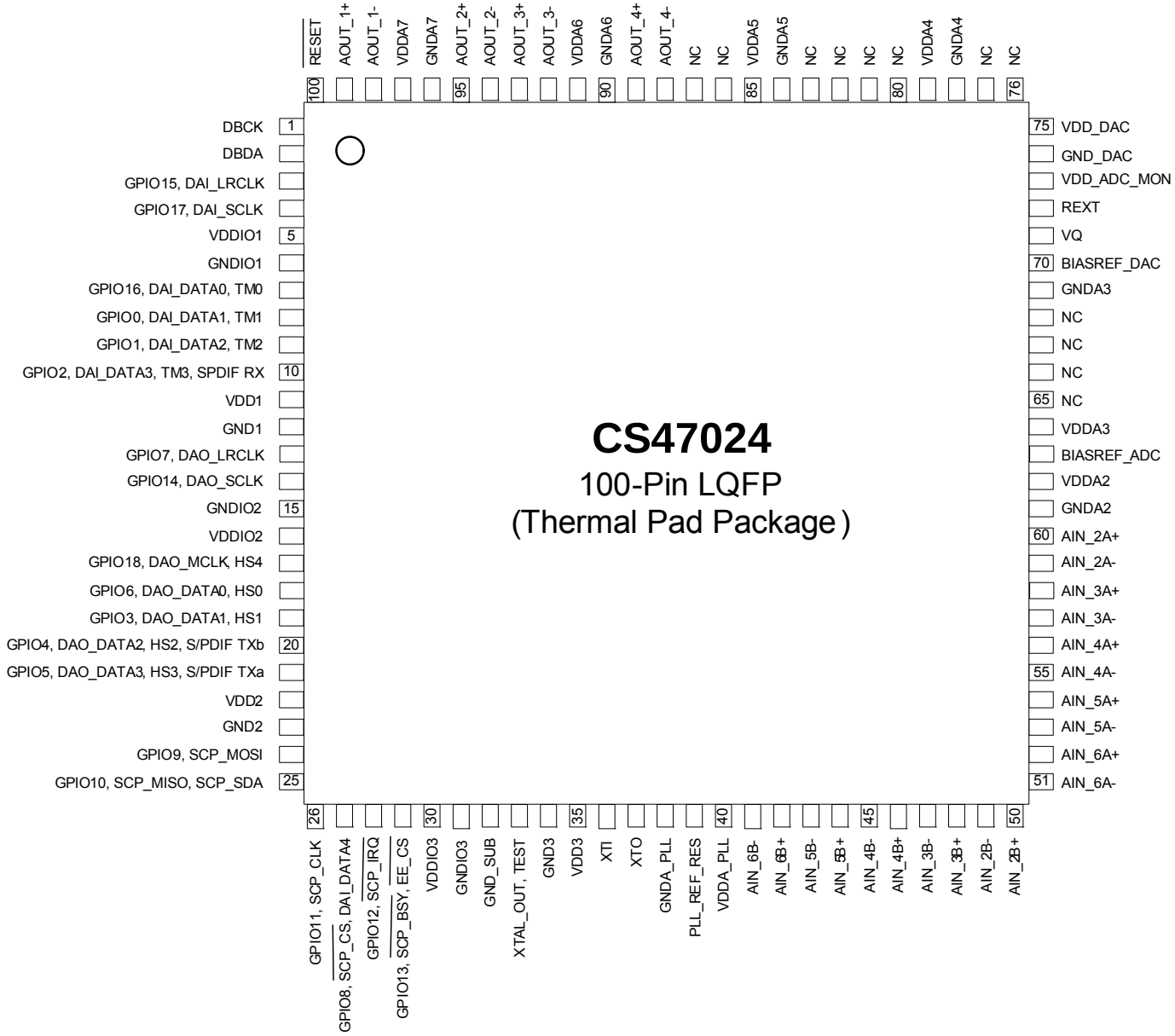
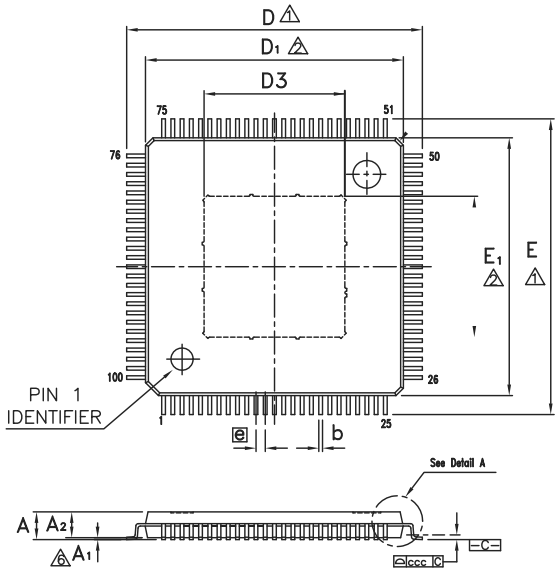
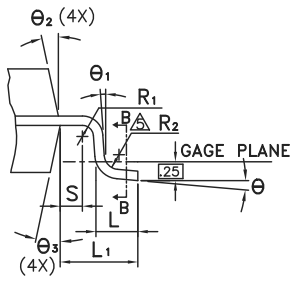


Figure 8-3. CS47024 Pinout Diagram

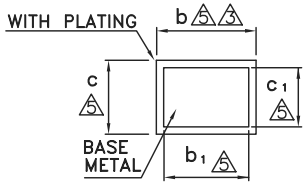
9 100-pin LQFP with Exposed Pad Package Drawing

Fig. 9-1 shows the 100-pin LQFP package with exposed pad for the CS47048, CS47028, and CS47024.





DETAIL A



SECTION B–B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP					
θ3						
ccc	0.08			0.003		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026.
9. **SPECIAL CHARACTERISTICS C CLASS: ccc**

Exposed Pad Size		
L/F	Dimension in mm	Dimension in inch
D3/E3	7.62 REF	0.300 REF

100LD E–PAD LQFP (14x14x1.4mm) PACKAGE OUTLINE
–Cu L/F,FOOTPRINT 2.0mm

Figure 9-1. 100-pin LQFP Package Drawing

10 Parameter Definitions

10.1 Dynamic Range

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

10.2 Total Harmonic Distortion + Noise

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth (typically 10 Hz–20 kHz), including distortion components. Expressed in decibels. Measured at –1 and –20 dBFS as suggested in AES17-1991 Annex A.

10.3 Frequency Response

A measure of the amplitude response variation from 10 Hz–20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

10.4 Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

10.5 Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

10.6 Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

10.7 Gain Drift

The change in gain value with temperature. Units in ppm/°C.

11 Revision History

Revision	Date	Changes
PP1	August, 2009	Updated Characterization data in Section 5.4, Section 5.7, Section 5.9, Section 5.11, Section 5.12, Section 5.16.1, Section 5.16.2, Section 5.16.3, Section 5.17.1, and Section 5.17.2. Modified Footnote 3 in both Section 5.16.1 and Section 5.16.2. Added Footnote 5 to Section 5.14. Updated Section 2.1. Modified Section 4.3.6 and Section 4.3.8. Modified references to TDM in various sections of the data sheet.
PP2	January, 2010	Updated TDM Feature description on page 1. Modified note at the bottom of the feature list on page 1. Updated table in Section 5.8, specifying performance data for 2- and 4-layer boards. Updated Table 3-1 and Table 3-2 Updated block diagrams in Fig. 4-1, Fig. 4-2, and Fig. 4-3.
PP3	June, 2010	Table 3-1: Straddled all three columns in the “Supports Different Fs Sample Rates” row to indicate that CS47024 devices have the same features as the CS47048 and CS47028. Added “The CS47024 has the 8-channel SRC block” to Section 4.3.7. Added text in the following places to indicate that the CS47024 implements the S/PDIF Rx functionality: • Removed dagger from the S/PDIF Rx bullet on p. 1. • Updated bullet in “Configurable Serial Audio Inputs/Outputs” row in Table 2 Integrated 192 kHz S/PDIF Rx, 2 Integrated 192 kHz S/PDIF Tx. • Changed entry in “S/PDIF In (Stereo Pairs)” column in Table 3-2. • Updated I2S block in Table 3-2. • Removed text “On the CS47048 and CS47028...” from Section 4.3.4. • Removed “(Not available on CS47024)” from the heading to Section 5.15. • Described additional support for TDM 8-channel output mode on CS47024. • Removed dagger from the TDM I/O bullet on p. 1. • Straddled “Configurable Serial Audio Inputs/Outputs” row in Table 3-1. • Changed cell in “TDM Out” column in Table 3-2. • Removed text “On the CS47048 and CS47028...” from Section 4.3.5.
PP4	February, 2011	Added “Decoder” information to Section 3. Changed the name of the core to “Cirrus Logic 32-bit core”.
PP5	February, 2011	Added “SPDIF RX” to Fig. 5-17.
PP6	June, 2011	In Section 4.3.1 and Section 4.3.7, removed mention of 192 kHz sampling frequency. Updated temperature operating conditions in Section 5.2. Updated pin 33 to XTAL_OUT, TEST in Fig. 8-1, Fig. 8-2, and Fig. 8-3.
PP7	April, 2012	Corrected peak reflow temperature in Table 7-1.
PP8	June, 2012	Added number of bits to Integrated DAC and ADC Functionality on the cover page.
PP9	July, 2012	Updated frequencies in Section 5.2. Added extended automotive grade information to Section 6 and Section 7.