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Understanding Embedded - DSP (Digital Signal Processors)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details

Product Status	Active
Type	Fixed Point
Interface	I ² C, SPI
Clock Rate	150MHz
Non-Volatile Memory	-
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/cs47024c-dqzr

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest you, go to www.cirrus.com.

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1 Documentation Strategy

The CS470xx Data Sheet describes the CS47048, CS47028, and CS47024 audio processors. This document should be used in conjunction with the following documents when evaluating or designing a system around the CS470xx processors.

Table 1-1. CS470xx Related Documentation

Document Name	Description
CS470xx Data Sheet	This document
CS470xx Hardware User's Manual Guide	Includes detailed system design information such as typical connection diagrams, boot-procedures, and pin descriptions
AN333 - CS470xx Firmware User's Manual	Includes a list of firmware modules available on the CS470xx family platform and detailed firmware design information including signal processing flow diagrams and control API information
DSP Composer User's Manual	Includes detailed configuration and usage information for the GUI development tool
CDB470xx User's Manual	Includes detailed instructions on the use of the CDB470xx development board

The scope of the CS470xx Data Sheet is primarily the hardware specifications of the CS470xx family of devices. This includes hardware functionality, characteristic data, pinout, and packaging information.

The intended audience for the CS470xx Data Sheet is the system PCB designer, MCU programmer, and the quality control engineer.

2 Overview

The CS470xx DSP is designed to provide high-performance post-processing and mixing of analog and digital audio. Dual clock domains are supported when the DAI and SPDIF RX inputs are used together. Integrated sample rate converters (SRCs) allow audio streams with different sample rates to be mixed. The low-power standby preserves battery life for applications that are always on, but not necessarily processing audio, such as automotive audio systems.

The CS470xx uses voltage-out DACs and is capable of supporting dual input clock domains through the use of the internal SRCs. The CS470xx is available in a 100-pin LQFP package. Refer to Table 3-1 and Table 3-2 for the input, output, and firmware configurations for the CS470xx DSP.

2.1 Licensing

Licenses are required for any third-party audio processing algorithms provided for the CS470xx. Contact your local Cirrus Logic Sales representative for more information.

Table 3-1. CS470xx Device Selection Guide

Features	CS47048-CQZ CS47048-DQZ	CS47028-CQZ CS47028-DQZ	CS47024-CQZ CS47024-DQZ
Primary Applications	<ul style="list-style-type: none"> 4-In/8-Out Car Audio High-end Digital TV Dual Source/Dual Zone 	<ul style="list-style-type: none"> 2-In/8-Out Car Audio Sound Bar DVD Receiver 	<ul style="list-style-type: none"> 2-In/4-Out Car Audio Digital TV Portable Audio Docking Station Portable DVD DVD Mini / Receiver Multimedia PC Speakers
Package	100-pin LQFP with Exposed Pad		
DSP Core	Cirrus Logic 32-bit Core		
SRAM	32K x 32-bit SRAM with three 2K blocks x 32-bit SRAM, assignable to either Y data or program memory		
Integrated DAC and ADC	<ul style="list-style-type: none"> 2 Channels of ADC input: with integrated 5:1 analog mux 2 additional channels of ADC input: without mux 8 channels of DAC output 	<ul style="list-style-type: none"> 2 channels of ADC input: with integrated 5:1 analog mux 8 channels of DAC output 	<ul style="list-style-type: none"> 2 channels of ADC input: with integrated 5:1 analog mux 4 channels of DAC output
Configurable Serial Audio Inputs/Outputs	<ul style="list-style-type: none"> Integrated 192 kHz S/PDIF Rx, 2 Integrated 192 kHz S/PDIF Tx I2S support for 32-bit Samples @ 192 kHz TDM Input modes (Up to 8 channels) TDM Output modes (Up to 8 channels) 		
Supports Different Fs Sample Rates	<ul style="list-style-type: none"> Integrated hardware SRC blocks for all ADC and DAC channels Additional 8-channel hardware SRC block Dual-domain Fs on inputs (I2S and S/PDIF Rx) Output can be master or slave 		
Other Features	<ul style="list-style-type: none"> Integrated Clock Manager/PLL with flexibility to operate from internal PLL, external crystal, external oscillator Host Control and Boot via SPI/I²C Serial Interface DSP Tool Set w/ Private Keys Protect Customer IP Configurable GPIOs and External Interrupts Hardware Watchdog Timer 		

Table 3-2. CS470xx Channel Count

Product	PCM/TDM In ¹	TDM Out ¹	PCM Out	ADC with 5:1 Input Mux	ADC without Mux	DAC Out	S/PDIF In (Stereo Pairs)	S/PDIF Out (Stereo Pairs)
CS47048	<ul style="list-style-type: none"> Up to 5 I2S lines, 2 channels per line or 1 TDM line, up to 8 channels per line. 	Up to 8 channels	8	2	2	8	1	2
CS47028	<ul style="list-style-type: none"> Up to 5 I2S lines, 2 channels per line or 1 TDM line, up to 8 channels per line. 	Up to 8 channels	8	2	0	8	1	2
CS47024	<ul style="list-style-type: none"> Up to 5 I2S lines, 2 channels per line or 1 TDM line, up to 8 channels per line. 	Up to 8 channels	8	2	0	4	1	2

1. Contact your Cirrus Logic representative to determine the TDM modes that are supported. The CS470xx can support up to 8 channels per line, but the DSP software provided for the IC can restrict this capability.

4 Hardware Functional Description

The CS470xx family, which includes the CS47048, CS47028, and CS47024 DSPs, is a true system-on-a-chip that combines a powerful 32-bit DSP engine with analog/digital audio inputs and analog/digital audio outputs. It can be integrated into a complex multi-DSP processing system, or stand alone in an audio product that requires analog-in and analog-out. A top level block diagram for the CS47048, CS47028, and CS47024 products are shown in Fig. 4-1, Fig. 4-2, and Fig. 4-3 respectively.

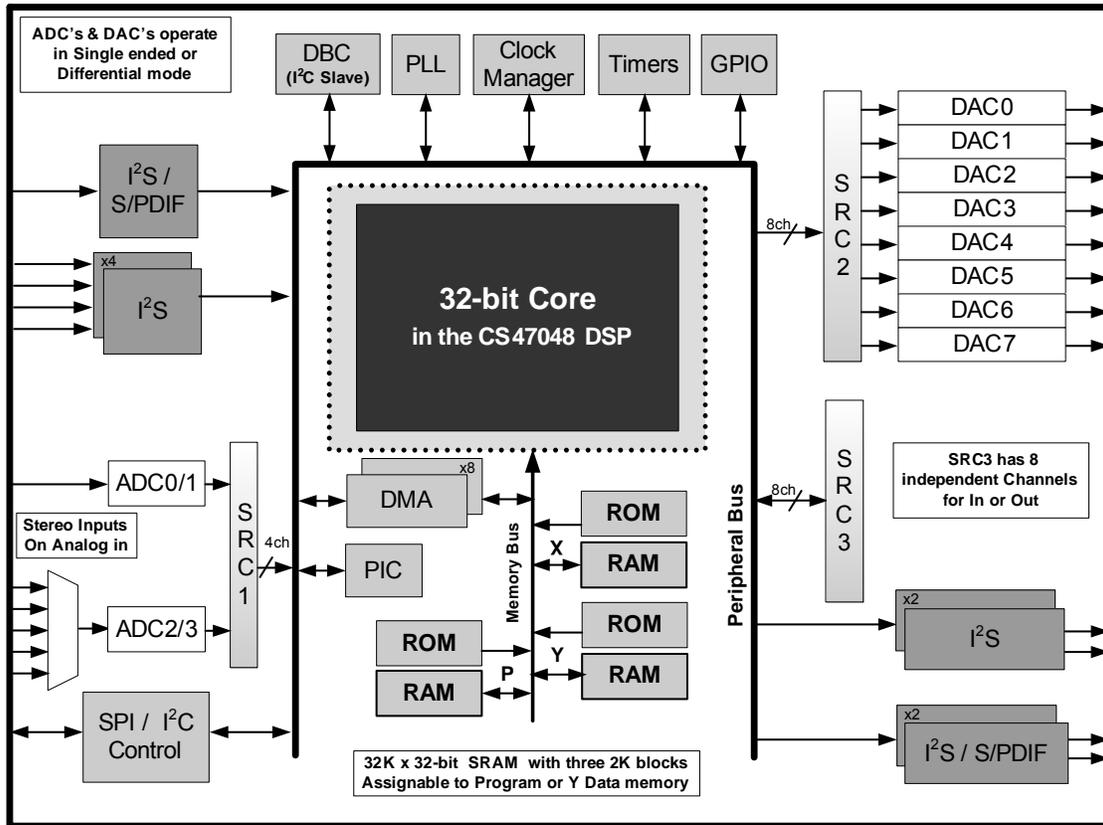


Figure 4-1. CS47048 Top-level Block Diagram

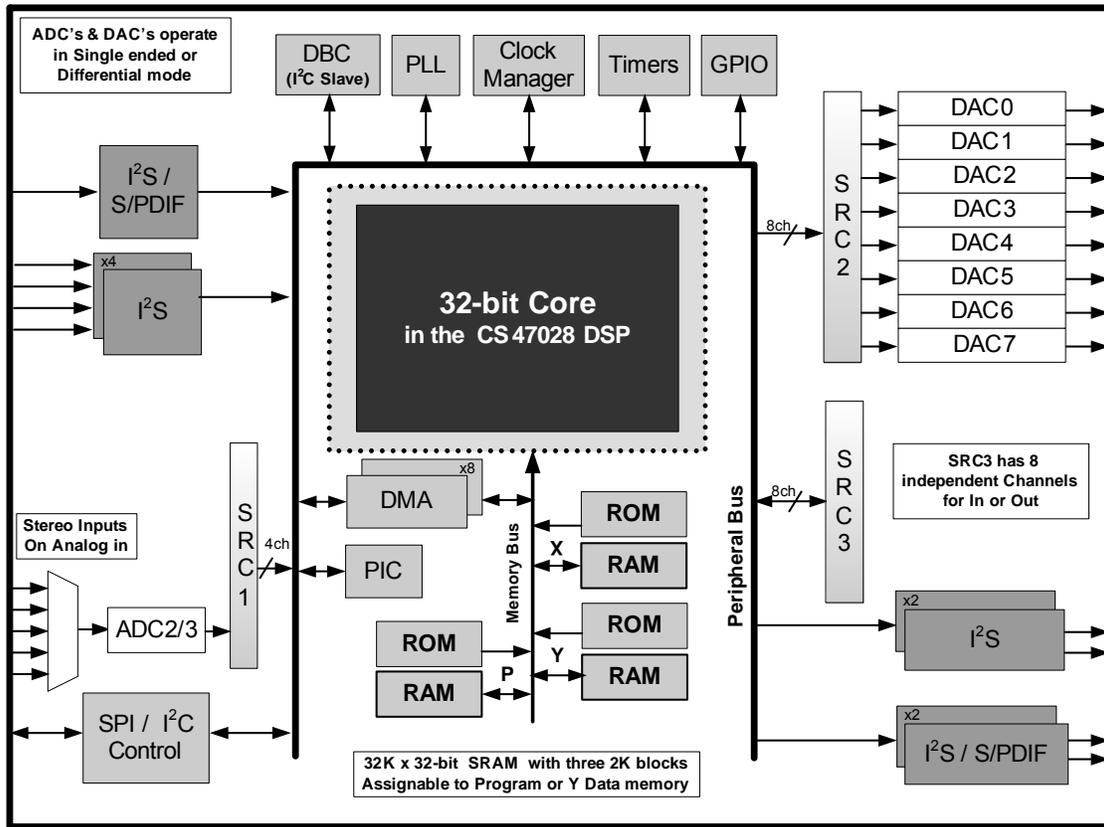


Figure 4-2. CS47028 Top-level Block Diagram

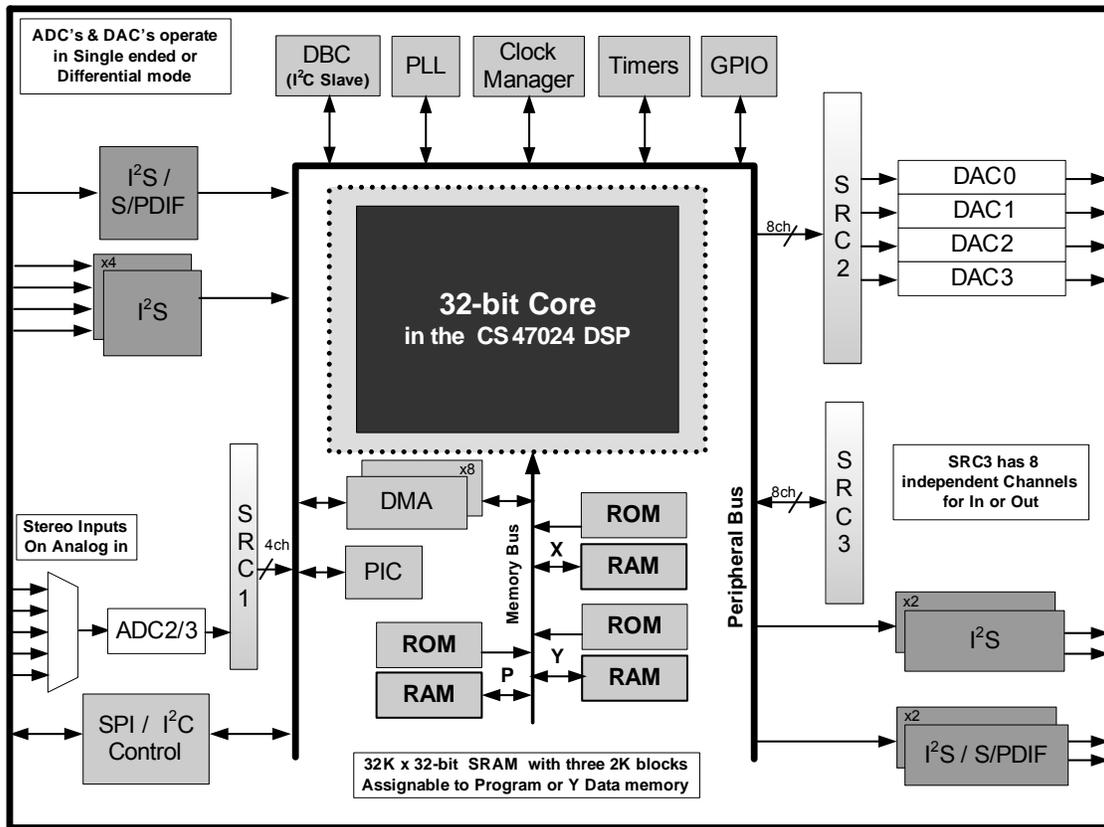


Figure 4-3. CS47024 Top-level Block Diagram

4.3.2 Digital to Analog Converter Port (DAC)

The DACs in the CS470xx devices feature dynamic range performance in excess of 100 dB. See Section 5.17 for more details on CS470xx DAC performance. The CS47024 device supports four simultaneous channels of digital-to-analog conversion. The CS47028 and CS47048 devices provide eight simultaneous channels of digital-to-analog conversion. The DACs have voltage mode outputs that can be connected either as single-ended or differential signals. The conversions are performed with $F_s=96$ kHz.

4.3.3 Digital Audio Input Port (DAI)

The input capabilities for each version of the CS470xx are summarized in Table 3-1 and Table 3-2.

Up to five DAI ports are available. Two of the DAI ports can be programmed to implement other functions. If the SPI mode is used, the DAI_DATA4 pin becomes the SCP_CS input. The integrated S/PDIF receiver can be used to take over the DAI_DATA3 pin.

The DAI port PCM inputs have a single slave-only clock domain. The S/PDIF receiver, if used, is a separate clock domain. The output of the S/PDIF Rx can then be converted through one of the internal SRC blocks to synchronize with the PCM input. The sample rate of the input clock domains can be determined automatically by the DSP, off-loading the task of monitoring the S/PDIF Rx from the host. A time-stamping feature provides the ability to also sample-rate convert the input data via software. The DAI port supports PCM format with word lengths up to 32 bits and sample rates as high as 192 kHz.

The DAI also supports a time division multiplexed (TDM) mode that packs up to 10 PCM audio channels on a single data line.

4.3.4 S/PDIF RX Input Port (DAI)

One of the PCM pins of the DAI can also be used as a DC-coupled, TTL-level S/PDIF Rx input capable of receiving and demodulating bi-phase encoded S/PDIF signals with $F_s \leq 192$ kHz.

4.3.5 Digital Audio Output Port (DAO)

DAO port supports PCM resolutions of up to 32-bits. The port supports sample rates (F_s) as high as 192 kHz. The port can be configured as an independent clock domain mastered by the DSP, or as a clock slave if an external MCLK or SCLK/LRCLK source is available.

The DAO also supports a time division multiplexed (TDM) mode, that packs up to 8 channels of PCM audio on a single data line.

4.3.6 S/PDIF TX Output Port (DAO)

Two of the serial audio pins can be re-configured as S/PDIF TX pins that drive a bi-phase encoded S/PDIF signal (data with embedded clock on a single line).

4.3.7 Sample Rate Converters (SRC)

All CS470xx devices have at least two internal hardware SRC modules. One is directly associated with the ADCs and normally serves to convert data from the 96 kHz sampling rate of the ADCs to another F_s appropriate for mixing with other audio in the system.

The other SRC module is directly associated with the DACs and normally serves to convert data from the DSP into the 96 kHz sample rate needed by the DACs.

The CS47024, CS47028, and CS47048 devices have an additional stand-alone 8-channel SRC module. This SRC module can be used to make independent input clock domains synchronous (different F_s on PCM input and S/PDIF Rx).

4.3.8 Serial Control Port (I²C or SPI)

The on-chip serial control port is capable of operating as master or slave in either SPI or I²C modes. Master/Slave operation is chosen by mode select pins when the CS470xx comes out of reset. The serial clock pin can support frequencies as high as 25 MHz in SPI mode (SPI clock speed must always be \leq (DSP Core Frequency/2)). The CS470xx serial control port also includes a pin for flow control of the communications interface (SCP_BSY) and a pin to indicate when the DSP has a message for the host (SCP_IRQ).

4.3.9 GPIO

Many of the CS470xx peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.3.10 PLL-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency, which is used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS470xx defaults to running from the external reference frequency and is switched to use the PLL output after overlays have been loaded and configured, either through master boot from an external flash or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

4.3.11 Hardware Watchdog Timer

The CS470xx has an integrated watchdog timer that acts as a “health” monitor for the DSP. The watchdog timer must be reset by the DSP before the counter expires, or the entire chip is reset. This peripheral ensures that the CS470xx resets itself in the event of a temporary system failure. In stand-alone mode (where there is no host MCU), the DSP reboots from external flash. In slave mode (where the host MCU is present), a GPIO is used to signal the host that the watchdog has expired and the DSP should be rebooted and re-configured.

4.4 DSP I/O Description

4.4.1 Multiplexed Pins

Many of the CS470xx pins are multifunctional. For details on pin functionality, see Section 10.5, “Pin Assignments”, in the *CS470xx Hardware User's Manual*.

4.4.2 Termination Requirements

Open-drain pins on the CS470xx must be pulled high for proper operation. See the *CS470xx Hardware User's Manual* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

Mode select pins on CS470xx are used to select the boot mode on the rising edge from reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS470xx Hardware User's Manual*.

4.4.3 Pads

The CS470xx Digital I/Os operate from the 3.3 V supply and are 5 V tolerant.

4.5 Application Code Security

The external program code can be encrypted by the programmer to protect any intellectual property it contains. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device. Contact your local Cirrus representative for details.

5 Characteristics and Specifications

Note: All data sheet minimum and maximum timing parameters are guaranteed over the rated voltage and temperature. All data sheet typical parameters are measured under the following conditions: T = 25°C, VDD = 1.8 V, VDDIO = VDDA = 3.3 V, GND = GNDIO = GNDA = 0 V.

5.1 Absolute Maximum Ratings

(GND = GNDIO = GNDA = 0V; all voltages with respect to 0V)

Parameter	Symbol	Min	Max	Unit
DC power supplies:				
Core supply	VDD	-0.3	2.0	V
Analog supply	VDDA	-0.3	3.6	V
I/O supply	VDDIO	-0.3	3.6	V
VDDA-VDDIO	—	—	0.3	V
Input pin current, any pin except supplies	I _{in}	—	±10	mA
Input voltage on PLL_REF_RES	V _{filt}	-0.3	3.6	V
Input voltage on digital I/O pins	V _{inio}	-0.3	5.0	V
Analog Input Voltage	V _{in}	AGND-0.7	VA+0.7	V
Storage temperature	T _{stg}	-65	150	°C

WARNING: Operation at or beyond these limits can result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5.2 Recommended Operating Conditions

(GND = GNDIO = GNDA = 0V; all voltages with respect to 0V)

Parameter	Symbol	Min	Typ	Max	Unit
DC power supplies:					
Core supply	VDD	1.71	1.8	1.89	V
Analog supply	VDDA	3.13	3.3	3.46	V
I/O supply	VDDIO	3.13	3.3	3.46	V
VDDA - VDDIO	—	—	0	—	V
Ambient operating temperature					
Commercial—CQZ (147 MHz)	T _A	0	—	+70	°C
Automotive—DQZ (131 MHz)	—	-40	—	+85	—
Automotive—DQZ (113 MHz)	—	-40	—	+105	—

Note: It is recommended that the 3.3 V IO supply come up ahead of or simultaneously with the 1.8 V core supply.

5.3 Digital DC Characteristics

(Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V _{IH}	2.0	—	—	V
Low-level input voltage, except XTI	V _{IL}	—	—	0.8	V
Low-level input voltage, XTI	V _{ILKXTI}	—	—	0.6	V
Input Hysteresis	V _{hys}	—	0.4	—	V
High-level output voltage (I _O = -2mA), except XTO	V _{OH}	VDDIO*0.9	—	—	V
Low-level output voltage (I _O = 2mA), except XTO	V _{OL}	—	—	VDDIO*0.1	V
Input leakage XTI	I _{LXTI}	—	—	5	µA
Input leakage current (all digital pins with internal pull-up resistors enabled)	I _{LEAK}	—	—	70	µA

5.4 Power Supply Characteristics

Note: Measurements performed under operating conditions

Parameter	Min	Typ	Max	Unit
Operational Power Supply Current:				
VDD: Core and I/O operating ¹	—	325	—	mA
VDDA: PLL operating current	—	16	—	mA
VDDA: DAC operating current (all 8 channels enabled)	—	56	—	mA
VDDA: ADC operating current (all 4 channels enabled)	—	34	—	mA
VDDIO: With most ports operating	—	27	—	mA
Total Operational Power Dissipation:		1025		mW
Standby Power Supply Current:				
VDD: Core and I/O not clocked	—	410	—	μA
VDDA: PLLs halted	—	26	—	μA
VDDA: DAC disabled	—	40	—	μA
VDDA: ADC disabled	—	24	—	μA
VDDIO: All connected I/O pins 3-stated by other ICs in system	—	215	—	μA
Total Standby Power Dissipation:		1745		μW

1. Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (100-pin LQFP with Exposed Pad)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C/Watt
Two-layer Board ¹		—	34	—	
Four-layer Board ²		—	18	—	
Thermal Resistance (Junction to Top of Package)	ψ_{jt}				°C/Watt
Two-layer Board ¹		—	0.54	—	
Four-layer Board ²		—	.28	—	

- To calculate the die temperature for a given power dissipation:

$$T_j = \text{Ambient temperature} + [(\text{Power Dissipation in Watts}) * \theta_{ja}]$$

- To calculate the case temperature for a given power dissipation:

$$T_c = T_j - [(\text{Power Dissipation in Watts}) * \psi_{jt}]$$

Note: Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20% of the top and bottom layers.

Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20% of the top and bottom layers and 0.5-oz. copper covering 90% of the internal power plane and ground plane layers.

5.6 Digital Switching Characteristics—RESET

Parameter	Symbol	Min	Max	Unit
RESET minimum pulse width low ¹	T_{rstl}	1	—	μs
All bidirectional pins high-Z after RESET low	T_{rst2z}	—	200	ns
Configuration pins setup before RESET high	T_{rstsu}	50	—	ns
Configuration pins hold after RESET high	T_{rsthd}	20	—	ns

1. The rising edge of $\overline{\text{RESET}}$ must not occur before the power supplies are stable at the recommended operating values as described in Section 5.2. In addition, for the configuration pins to be read correctly, the RESET T_{rstl} requirement must be met.

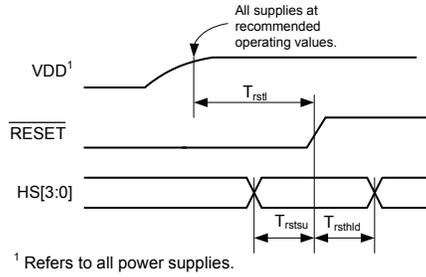


Figure 5-1. RESET Timing at Power-on

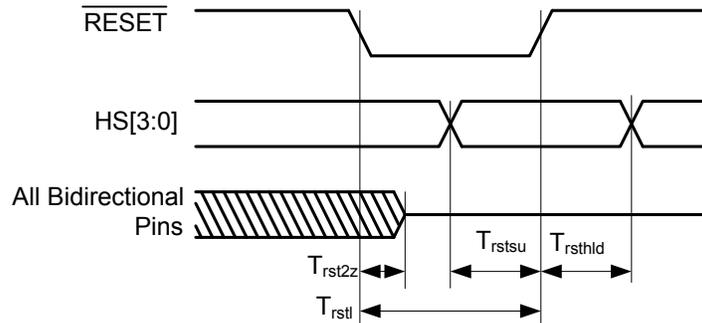


Figure 5-2. RESET Timing after Power is Stable

5.7 Digital Switching Characteristics–XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency ¹	F_{xtal}	12.288	24.576	MHz
XTI period	T_{clki}	41	81	ns
XTI high time	T_{clkih}	13.3	—	ns
XTI low time	T_{clkil}	13.3	—	ns
External Crystal Load Capacitance (parallel resonant) ²	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR	—	50	Ω

- Part characterized with the following crystal frequency values: 12.288 and 24.576 MHz.
- C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals that require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

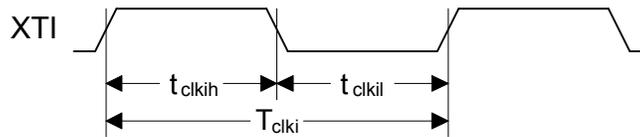


Figure 5-3. XTI Timing

5.8 Digital Switching Characteristics—Internal Clock

Parameter	Symbol	Min (2-layer Boards)	Min (4-layer Boards)	Max (2-layer Boards)	Max (4-layer Boards)	Unit
Internal DSP_CLK frequency ¹	F_{dclk}	(See Footnote 2)				MHz
CS47048-CQZ			F_{xtal}	147	147	
CS47048-DQZ			F_{xtal}	131	147	
CS47028-CQZ			F_{xtal}	147	147	
CS47028-DQZ			F_{xtal}	131	147	
CS47024-CQZ			F_{xtal}	147	147	
CS47024-DQZ			F_{xtal}	131	147	
Internal DSP_CLK period ¹	DCLKP					ns
CS47048-CQZ		6.8	6.8	$1/F_{xtal}$		
CS47048-DQZ		7.6	6.8	$1/F_{xtal}$		
CS47028-CQZ		6.8	6.8	$1/F_{xtal}$		
CS47028-DQZ		7.6	6.8	$1/F_{xtal}$		
CS47024-CQZ		6.8	6.8	$1/F_{xtal}$		
CS47024-DQZ		7.6	6.8	$1/F_{xtal}$		

1. After initial power-on reset, $F_{dclk} = F_{xtal}$. After initial kick-start commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

2. See Section 5.7. for all references to F_{xtal} .

5.9 Digital Switching Characteristics—Serial Control Port—SPI Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
SCP_CLK frequency ¹	f_{spisck}	—	—	25	MHz
SCP_CS falling to SCP_CLK rising	t_{spicss}	24	—	—	ns
SCP_CLK low time	t_{spickl}	20	—	—	ns
SCP_CLK high time	t_{spickh}	20	—	—	ns
Setup time SCP_MOSI input	t_{spidsu}	5	—	—	ns
Hold time SCP_MOSI input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MISO output valid	t_{spidov}	—	—	11	ns
SCP_CLK falling to SCP_IRQ rising	$t_{spiirqh}$	—	—	27	ns
SCP_CS rising to SCP_IRQ falling	$t_{spiirql}$	0	—	—	ns
SCP_CLK low to SCP_CS rising	t_{spicsh}	24	—	—	ns
SCP_CS rising to SCP_MISO output high-Z	$t_{spicsdz}$	—	20	—	ns
SCP_CLK rising to SCP_BSY falling	$t_{spicbsyl}$	—	$3 \cdot \text{DCLKP} + 20$	—	ns

1. f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port can be limited by the firmware application. Flow control using the SCP_BSY pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is $F_{xtal}/3$.

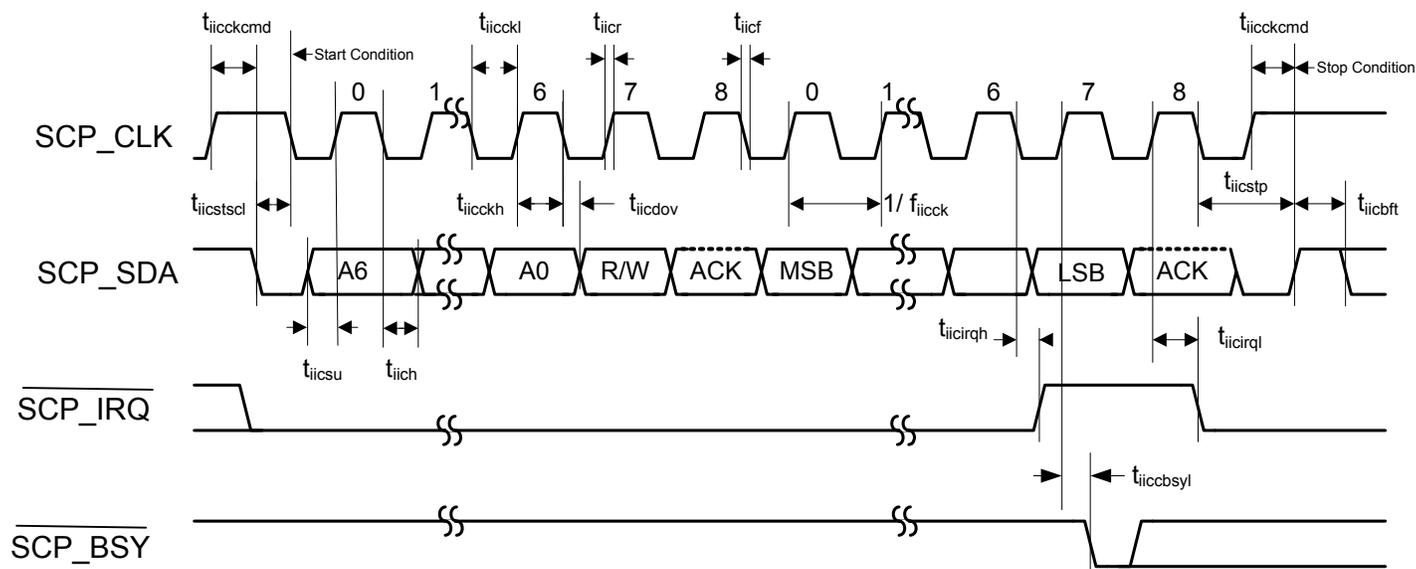


Figure 5-6. Serial Control Port—I2C Slave Mode Timing

5.12 Digital Switching Characteristics—Serial Control Port—I2C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency ¹	f_{iicck}	—	400	kHz
SCP_CLK rise time	t_{iicr}	—	150	ns
SCP_CLK fall time	t_{iicf}	—	150	ns
SCP_CLK low time	t_{iicckl}	1.25	—	μ s
SCP_CLK high time	t_{iicckh}	1.25	—	μ s
SCP_CLK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25	—	μ s
START condition to SCP_CLK falling	$t_{iicstsc}$	1.25	—	μ s
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	—	μ s
Bus free time between STOP and START conditions	t_{iicbft}	3	—	μ s
Setup time SCP_SDA input valid to SCP_CLK rising	$t_{iicstsu}$	110	—	ns
Hold time SCP_SDA input after SCP_CLK falling	$t_{iicstch}$	100	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	—	36	ns

1. f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port can be limited by the firmware application.

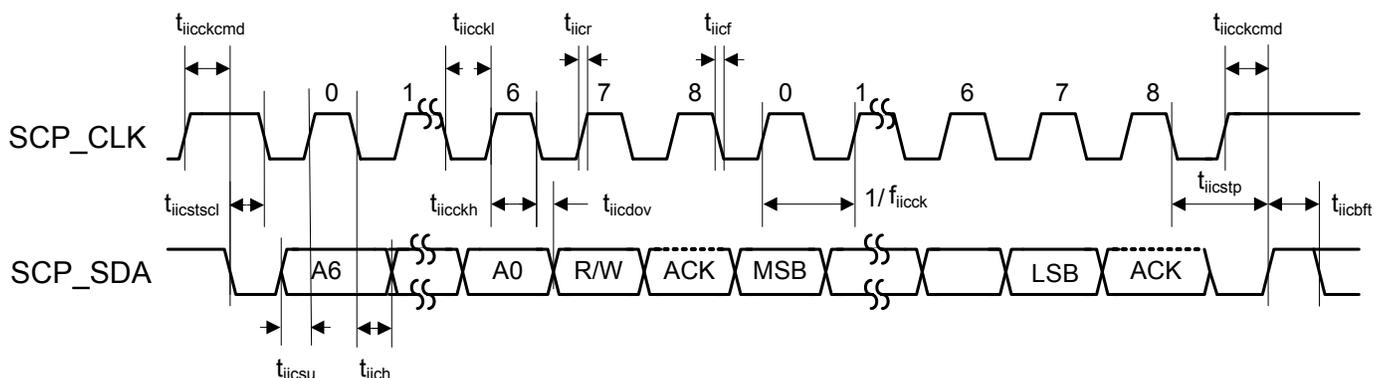


Figure 5-7. Serial Control Port—I2C Master Mode Timing

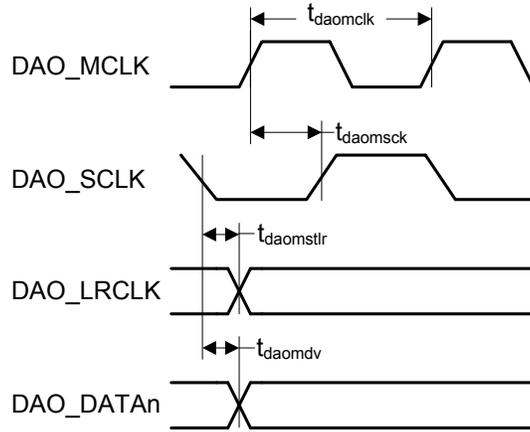


Figure 5-10. DAO_LRCLK Transition after DAO_SCLK Inactive Edge

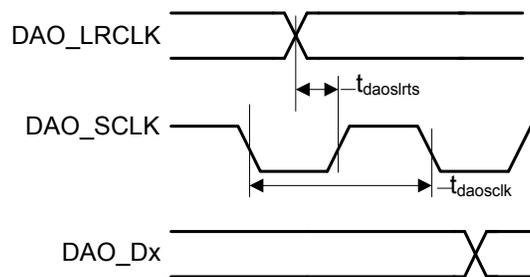


Figure 5-11. DAO_LRCLK Transition before DAO_SCLK Inactive Edge

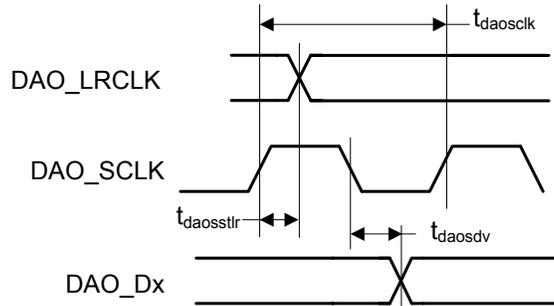


Figure 5-12. DAO_LRCLK Transition after DAO_SCLK Inactive Edge

5.15 Digital Switching Characteristics—S/PDIF RX Port

(Inputs: Logic 0 = V_{IL} , Logic 1 = V_{IH} , $C_L = 20$ pF)

Parameter	Symbol	Min	Typ	Max	Units
PLL Clock Recovery Sample Rate Range	—	30	—	200	kHz

5.16 ADC Characteristics

5.16.1 Analog Input Characteristics (Commercial)

Test Conditions (unless otherwise specified): $T_A = 0$ – $+70^\circ\text{C}$; $V_{DD} = 1.8\text{V} \pm 5\%$, $V_{DDA} (V_A) = 3.3\text{V} \pm 5\%$, 1kHz sine wave driven through the passive input filter ($R_i = 10$ k Ω) in Fig. 5-13 or Fig. 5-14; DSP running test application; Measurement Bandwidth is 10–20kHz.

Parameter	Differential			Single-ended			Unit
	Min	Typ	Max	Min	Typ	Max	
Fs = 96 kHz							
Dynamic Range ^{1,6,7}							
A-weighted	99	105	—	96	102	—	dB
Unweighted	96	102	—	93	99	—	dB
40 kHz bandwidth unweighted	—	99	—	—	96	—	dB
Total Harmonic Distortion + Noise ^{6,7}							
–1 dB	—	–98	–92	—	–95	–89	dB
–20 dB	—	–82	—	—	–79	—	dB
–60 dB	—	–42	—	—	–39	—	dB
40 kHz bandwidth –1 dB	—	–90	—	—	–90	—	dB
AIN_1A/B Interchannel Isolation ¹⁰	—	95	—	—	95	—	dB
AID_[2.6]A/B MUX Interchannel Isolation	—	95	—	—	95	—	dB
DC Accuracy							
Interchannel Gain Mismatch	—	0.1	—	—	0.1	—	dB
Gain Drift	—	± 120	—	—	± 120	—	ppm/ $^\circ\text{C}$
Analog Input							
Full-scale Input Voltage ^{2,3}	3.3	$3.7 \cdot V_A$	3.9	1.65	$1.85 \cdot V_A$	1.95	V_{PP}
Differential Input Impedance ⁴	—	400	—	—	—	—	Ω
Single-ended Input Impedance ⁵	—	—	—	—	200	—	Ω
Common Mode Rejection Ratio (CMRR) ⁸	—	60	—	—	—	—	dB
Parasitic Load Capacitance (C_L) ⁹	—	—	20	—	—	20	pF

1. dB units referred to the typical full-scale voltage.

2. These full-scale values were measured with $R_i = 10$ k for both the single-ended and differential mode input circuits.

3. The full-scale voltage can be changed by scaling R_i .

$$\text{Differential Full-Scale } (V_{pp}) = 3.7 \cdot V_{DDA} \cdot (R_i + 200) / (10k + 200)$$

$$\text{Single-Ended Full-Scale } (V_{pp}) = 1.85 \cdot V_{DDA} \cdot (R_i + 200) / (10k + 200)$$

4. Measured between AIN_xx+ and AN_xx–.

5. Measured between AIN_xx+ and AGND.

6. Decreasing full-scale voltage by reducing R_i causes the noise floor to increase.

7. Common mode input current should be kept to less than ± 160 μA to avoid performance degradation: $|(I_{ip} + I_{in})/2| < 160$ μA . This corresponds to ± 1.6 V for $R_i = 10$ k Ω in the differential case.

8. This number was measured using perfectly matched external resistors (R_i). Mismatch in the external resistors typically reduces CMRR by 20 log $(|\Delta R_i|/R_i + 0.001)$.

9. C_L represents the parasitic load capacitance between R_i on the input circuit and the input pin of the CS47048 package.

10. This measurement is not applicable to the CS47028 and CS47024 devices.

5.16.2 Analog Input Characteristics (Automotive)

Test Conditions (unless otherwise specified): TA = –40–85°C; VDD = 1.8V±5%, VDDA (VA) = 3.3V±5%; kHz sine wave driven through the passive input filter (R_i = 10 kΩ) in Fig. 5-13 or Fig. 5-14; DSP running test application; Measurement Bandwidth is 10 Hz–20 kHz.

Parameter	Differential			Single-ended			Unit
	Min	Typ	Max	Min	Typ	Max	
Fs = 96 kHz							
Dynamic Range ^{1,6,7}							
A-weighted	97	105	—	94	102	—	dB
Unweighted	94	102	—	91	99	—	dB
40 kHz bandwidth unweighted	—	99	—	—	96	—	dB
Total Harmonic Distortion + Noise ^{6,7}							
–1 dB	—	–98	–90	—	–95	–87	dB
–20 dB	—	–82	—	—	–79	—	dB
–60 dB	—	–42	—	—	–39	—	dB
40 kHz bandwidth –1 dB	—	–90	—	—	–90	—	dB
AIN_1A/B Interchannel Isolation ¹⁰	—	95	—	—	95	—	dB
AID_[2.6]A/B MUX Interchannel Isolation	—	95	—	—	95	—	dB
DC Accuracy							
Interchannel Gain Mismatch	—	0.1	—	—	0.1	—	dB
Gain Drift	—	±120	—	—	±120	—	ppm/°C
Analog Input							
Full-scale Input Voltage ^{2,3}	3.3	3.7•VA	3.9	1.65	1.85•VA	1.95	V _{PP}
Differential Input Impedance ⁴	—	400	—	—	—	—	Ω
Single-ended Input Impedance ⁵	—	—	—	—	200	—	Ω
Common Mode Rejection Ratio (CMRR) ⁸	—	60	—	—	—	—	dB
Parasitic Load Capacitance (C _L) ⁹	—	—	20	—	—	20	pF

1. dB units referred to the typical full-scale voltage.
2. These full-scale values were measured with R_i=10k for both the single-ended and differential mode input circuits.
3. The full-scale voltage can be changed by scaling R_i.
Differential Full-Scale (V_{pp}) = 3.7•VDDA•(R_i+200)/(10k+200)
Single-Ended Full-Scale (V_{pp}) = 1.85•VDDA•(R_i+200)/(10k+200)
4. Measured between AIN_xx+ and AN_xx–.
5. Measured between AIN_xx+ and AGND.
6. Decreasing full-scale voltage by reducing R_i causes the noise floor to increase.
7. Common mode input current should be kept to less than ±160uA to avoid performance degradation: $|(I_{ip}+I_{in})/2| < 160\mu A$. This corresponds to ±1.6V for R_i=10 kΩ in the differential case.
8. This number was measured using perfectly matched external resistors (R_i). Mismatch in the external resistors typically reduces CMRR by 20 log $(|\Delta R_i|/R_i + 0.001)$.
9. C_L represents the parasitic load capacitance between R_i on the input circuit and the input pin of the CS47048 package.
10. This measurement is not applicable to the CS47028 and CS47024 devices.

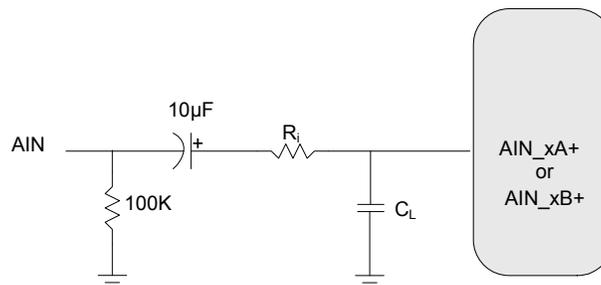


Figure 5-13. ADC Single-ended Input Test Circuit

Parameter	Differential			Single-ended			Unit
	Min	Typ	Max	Min	Typ	Max	
Analog Input							
Full-scale Output	1.20	1.40•VA	1.60	0.60	0.70•VA	0.80	V _{PP}
Interchannel Gain Mismatch	—	0.1	—	—	0.1	—	dB
Gain Drift	—	±120	—	—	±120	—	ppm/°C
Output Impedance	—	100	—	—	100	—	Ω
DC Current Draw from an AOUT Pin ¹	—	—	10	—	—	10	μA
AC-load Resistance (R _L) ²	3	—	—	3	—	—	kΩ
Load Capacitance (C _L) ²	—	—	100	—	—	100	pF

5.17.2 Analog Output Characteristics (Automotive)

Test Conditions (unless otherwise specified): T_A = –40 to +85°C; VDD = 1.8V±5%, VDDA(VA) = 3.3V±5%; 1 kHz sine wave driven through a filter shown in Fig. 5-15 or Fig. 5-16; DSP running test application; Measurement Bandwidth is 20 Hz–20 kHz.

Parameter	Differential			Single-ended			Unit
	Min	Typ	Max	Min	Typ	Max	
F_s = 96 kHz							
Dynamic Range							
A-weighted	100	108	—	97	105	—	dB
Unweighted	97	105	—	94	102	—	dB
Total Harmonic Distortion + Noise							
0 dB	—	–98	–90	—	–95	–87	dB
–20 dB	—	–88	—	—	–85	—	dB
–60 dB	—	–48	—	—	–45	—	dB
Interchannel Isolation (1 kHz)	—	95	—	—	95	—	dB
Analog Input							
Full-scale Output	1.20	1.40•VA	1.60	0.60	0.70•VA	0.80	V _{PP}
Interchannel Gain Mismatch	—	0.1	—	—	0.1	—	dB
Gain Drift	—	±120	—	—	±120	—	ppm/°C
Output Impedance	—	100	—	—	100	—	Ω
DC Current Draw from an AOUT Pin ¹	—	—	10	—	—	10	μA
AC-load Resistance (R _L) ²	3	—	—	3	—	—	kΩ
Load Capacitance (C _L) ²	—	—	100	—	—	100	pF

1. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC-blocking capacitors.
2. Guaranteed by design. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L represents any capacitive loading that appears *before* the 560 Ω series resistor (typically parasitic), and effectively moves the dominant pole of the two-pole amp in the output stage. Increasing this value beyond the recommended 100 pF can cause the internal op-amp to become unstable.

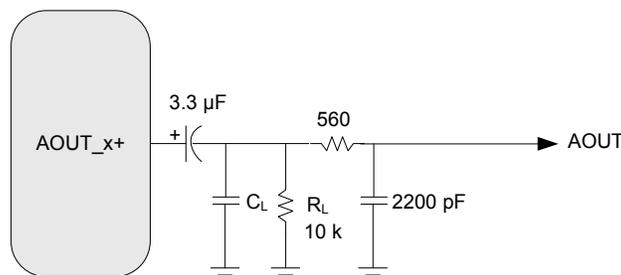


Figure 5-15. DAC Single-ended Output Test Circuit

6 Ordering Information

The CS470xx DSP part numbers are described as follows:

Example:

CS47048I-XYZR

where

I–ROM ID Letter

X–Product Grade

Y–Package Type

Z–Lead (Pb) Free

R–Tape and Reel Packaging

Table 6-1. Ordering Information

Part No.	Grade	Temp. Range	Package
CS47048C-CQZ	Commercial	0–+70°C	100-pin LQFP
CS47048C-DQZ	Automotive	–40–+85°C	
CS47048C-EQZ	Extended Automotive	–40–+105°C	
CS47028C-CQZ	Commercial	0–+70°C	
CS47028C-DQZ	Automotive	–40–+85°C	
CS47028C-EQZ	Extended Automotive	–40–+105°C	
CS47024C-CQZ	Commercial	0–+70°C	
CS47024C-DQZ	Automotive	–40–+85°C	
CS47024C-EQZ	Extended Automotive	–40–+105°C	

Note: Contact the factory for availability of the –D (automotive grade) package.

7 Environmental, Manufacturing, and Handling Information

Table 7-1. Environmental, Manufacturing, and Handling Information

Model Number	Peak Reflow Temp.	MSL ¹ Rating	Max Floor Life
CS47048C-CQZ	260° C	3	7 days
CS47048C-DQZ			
CS47048C-EQZ			
CS47028C-CQZ	260° C	3	7 days
CS47028C-DQZ			
CS47028C-EQZ			
CS47024C-CQZ	260° C	3	7 days
CS47024C-DQZ			
CS47024C-EQZ			

1. Moisture Sensitivity Level as specified by IPC/JEDEC J-STD-020.

8 Device Pinout Diagrams

8.1 CS47048, 100-pin LQFP Pinout Diagram

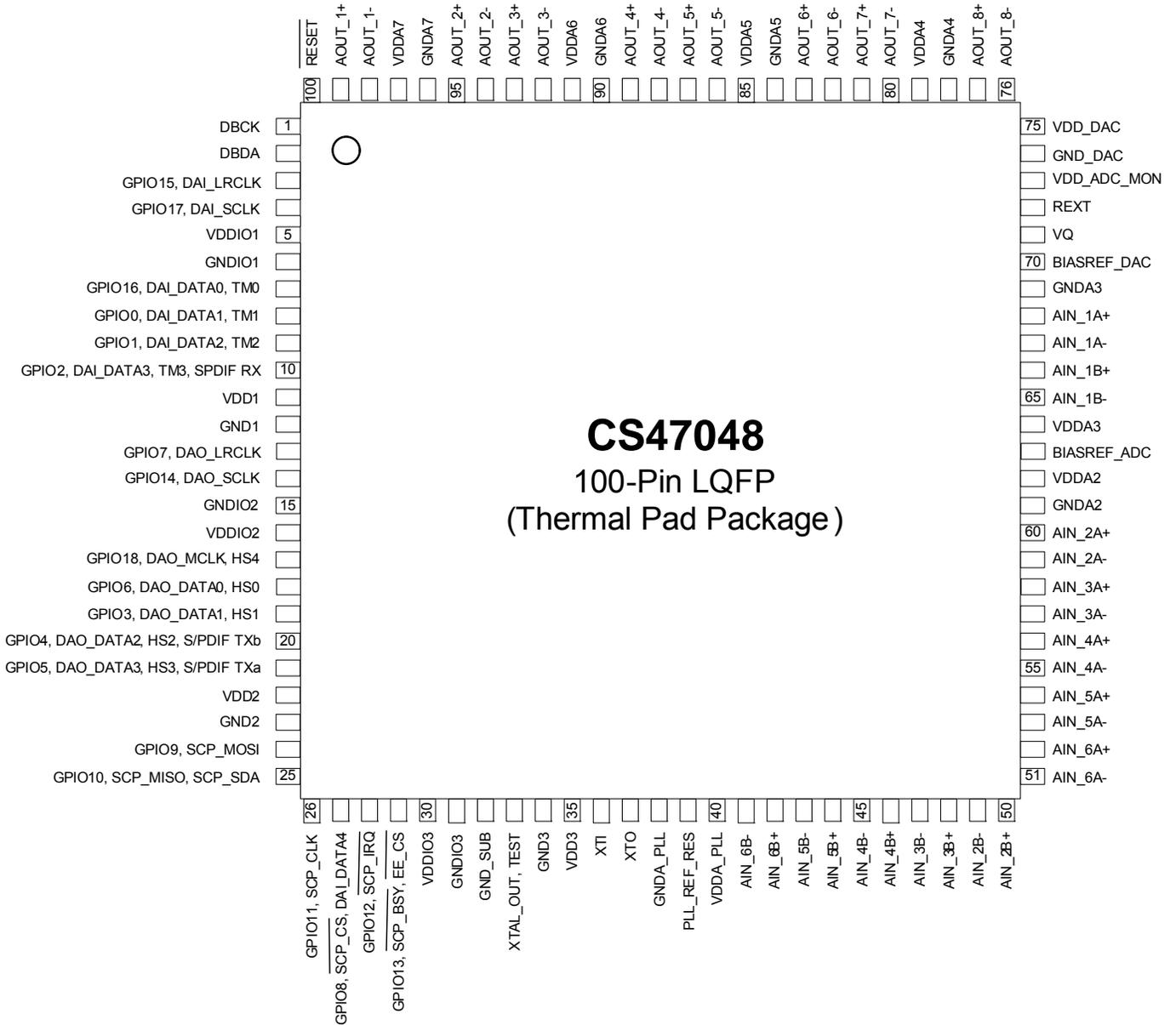


Figure 8-1. CS47048 Pinout Diagram

9 100-pin LQFP with Exposed Pad Package Drawing

Fig. 9-1 shows the 100-pin LQFP package with exposed pad for the CS47048, CS47028, and CS47024.

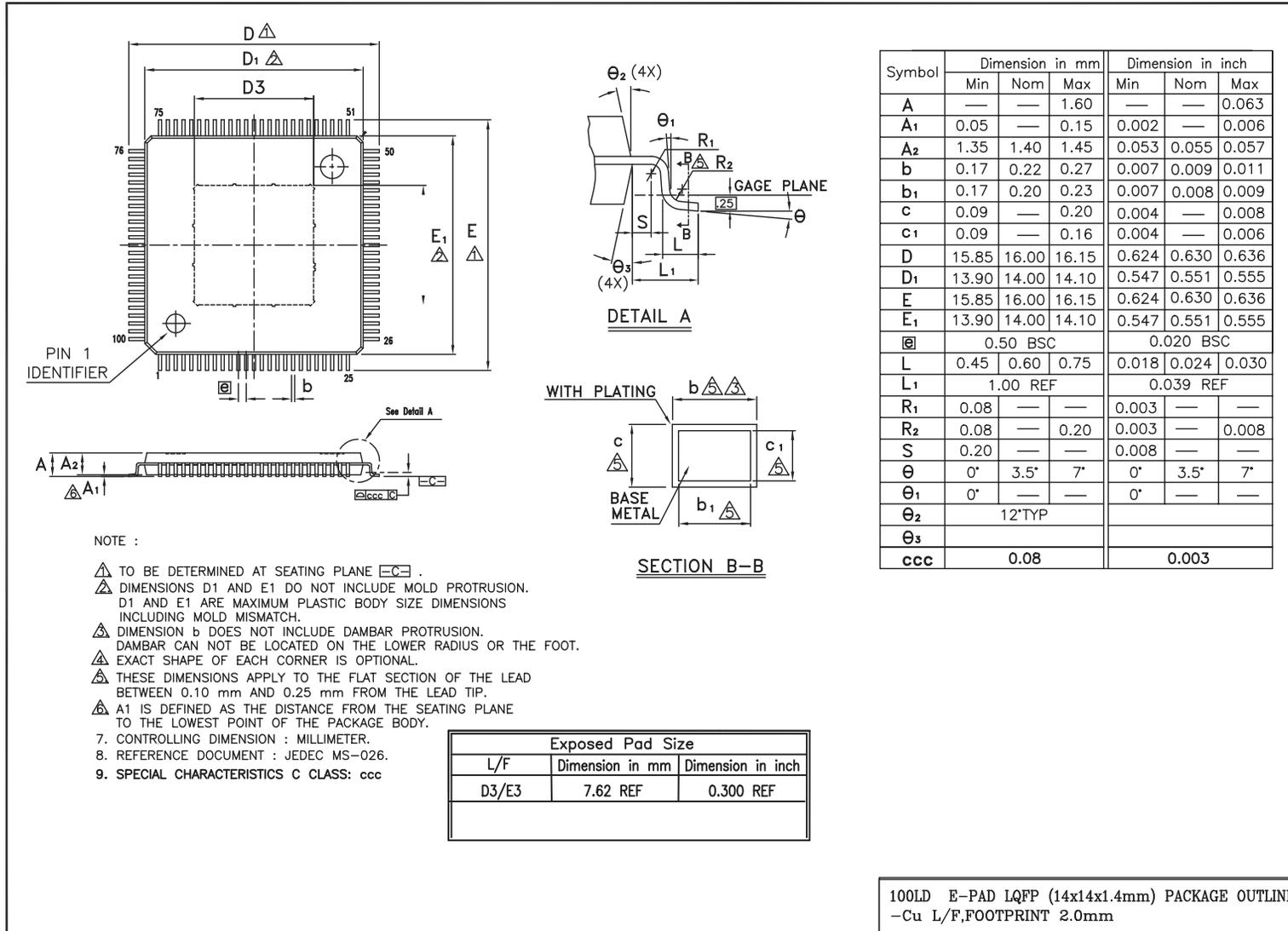


Figure 9-1. 100-pin LQFP Package Drawing

11 Revision History

Revision	Date	Changes
PP1	August, 2009	Updated Characterization data in Section 5.4, Section 5.7, Section 5.9, Section 5.11, Section 5.12, Section 5.16.1, Section 5.16.2, Section 5.16.3, Section 5.17.1, and Section 5.17.2. Modified Footnote 3 in both Section 5.16.1 and Section 5.16.2. Added Footnote 5 to Section 5.14. Updated Section 2.1. Modified Section 4.3.6 and Section 4.3.8. Modified references to TDM in various sections of the data sheet.
PP2	January, 2010	Updated TDM Feature description on page 1. Modified note at the bottom of the feature list on page 1. Updated table in Section 5.8, specifying performance data for 2- and 4-layer boards. Updated Table 3-1 and Table 3-2 Updated block diagrams in Fig. 4-1, Fig. 4-2, and Fig. 4-3.
PP3	June, 2010	Table 3-1: Straddled all three columns in the "Supports Different Fs Sample Rates" row to indicate that CS47024 devices have the same features as the CS47048 and CS47028. Added "The CS47024 has the 8-channel SRC block" to Section 4.3.7. Added text in the following places to indicate that the CS47024 implements the S/PDIF Rx functionality: <ul style="list-style-type: none"> • Removed dagger from the S/PDIF Rx bullet on p. 1. • Updated bullet in "Configurable Serial Audio Inputs/Outputs" row in Table 2 Integrated 192 kHz S/PDIF Rx, 2 Integrated 192 kHz S/PDIF Tx. • Changed entry in "S/PDIF In (Stereo Pairs)" column in Table 3-2. • Updated I2S block in Table 3-2. • Removed text "On the CS47048 and CS47028..." from Section 4.3.4. • Removed "(Not available on CS47024)" from the heading to Section 5.15. • Described additional support for TDM 8-channel output mode on CS47024. • Removed dagger from the TDM I/O bullet on p. 1. • Straddled "Configurable Serial Audio Inputs/Outputs" row in Table 3-1. • Changed cell in "TDM Out" column in Table 3-2. • Removed text "On the CS47048 and CS47028..." from Section 4.3.5.
PP4	February, 2011	Added "Decoder" information to Section 3. Changed the name of the core to "Cirrus Logic 32-bit core".
PP5	February, 2011	Added "SPDIF RX" to Fig. 5-17.
PP6	June, 2011	In Section 4.3.1 and Section 4.3.7, removed mention of 192 kHz sampling frequency. Updated temperature operating conditions in Section 5.2. Updated pin 33 to XTAL_OUT, TEST in Fig. 8-1, Fig. 8-2, and Fig. 8-3.
PP7	April, 2012	Corrected peak reflow temperature in Table 7-1.
PP8	June, 2012	Added number of bits to Integrated DAC and ADC Functionality on the cover page.
PP9	July, 2012	Updated frequencies in Section 5.2. Added extended automotive grade information to Section 6 and Section 7.