Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	I²C, SPI
Clock Rate	150MHz
Non-Volatile Memory	-
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/cs47028c-cqzr

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.

Table 3-1. CS470xx Device Selection Guide

Features	CS47048-CQZ CS47048-DQZ	CS47028-CQZ CS47028-DQZ	CS47024-CQZ CS47024-DQZ
Primary Applications	• 4-In/8-Out Car Audio • High-end Digital TV • Dual Source/Dual Zone	• 2-In/8-Out Car Audio • Sound Bar • DVD Receiver	• 2-In/4-Out Car Audio • Digital TV • Portable Audio Docking Station • Portable DVD • DVD Mini / Receiver • Multimedia PC Speakers
Package	100-pin LQFP with Exposed Pad		
DSP Core	Cirrus Logic 32-bit Core		
SRAM	32K x 32-bit SRAM with three 2K blocks x 32-bit SRAM, assignable to either Y data or program memory		
Integrated DAC and ADC	• 2 Channels of ADC input: with integrated 5:1 analog mux • 2 additional channels of ADC input: without mux • 8 channels of DAC output	• 2 channels of ADC input: with integrated 5:1 analog mux • 8 channels of DAC output	• 2 channels of ADC input: with integrated 5:1 analog mux • 4 channels of DAC output
Configurable Serial Audio Inputs/Outputs	• Integrated 192 kHz S/PDIF Rx, 2 Integrated 192 kHz S/PDIF Tx • I2S support for 32-bit Samples @ 192 kHz • TDM Input modes (Up to 8 channels) • TDM Output modes (Up to 8 channels)		
Supports Different Fs Sample Rates	• Integrated hardware SRC blocks for all ADC and DAC channels • Additional 8-channel hardware SRC block • Dual-domain Fs on inputs (I2S and S/PDIF Rx) • Output can be master or slave		
Other Features	• Integrated Clock Manager/PLL with flexibility to operate from internal PLL, external crystal, external oscillator • Host Control and Boot via SPI/I²C Serial Interface • DSP Tool Set w/ Private Keys Protect Customer IP • Configurable GPIOs and External Interrupts • Hardware Watchdog Timer		

Table 3-2. CS470xx Channel Count

Product	PCM/TDM In[1]	TDM Out[1]	PCM Out	ADC with 5:1 Input Mux	ADC without Mux	DAC Out	S/PDIF In (Stereo Pairs)	S/PDIF Out (Stereo Pairs)
CS47048	• Up to 5 I2S lines, 2 channels per line or • 1 TDM line, up to 8 channels per line.	Up to 8 channels	**8**	**2**	**2**	**8**	**1**	**2**
CS47028	• Up to 5 I2S lines, 2 channels per line or • 1 TDM line, up to 8 channels per line.	Up to 8 channels	**8**	**2**	**0**	**8**	**1**	**2**
CS47024	• Up to 5 I2S lines, 2 channels per line or • 1 TDM line, up to 8 channels per line.	Up to 8 channels	**8**	**2**	**0**	**4**	**1**	**2**

1. Contact your Cirrus Logic representative to determine the TDM modes that are supported. The CS470xx can support up to 8 channels per line, but the DSP software provided for the IC can restrict this capability.

4 Hardware Functional Description

The CS470xx family, which includes the CS47048, CS47028, and CS47024 DSPs, is a true system-on-a-chip that combines a powerful 32-bit DSP engine with analog/digital audio inputs and analog/digital audio outputs. It can be integrated into a complex multi-DSP processing system, or stand alone in an audio product that requires analog-in and analog-out. A top level block diagram for the CS47048, CS47028, and CS47024 products are shown in Fig. 4-1, Fig. 4-2, and Fig. 4-3 respectively.

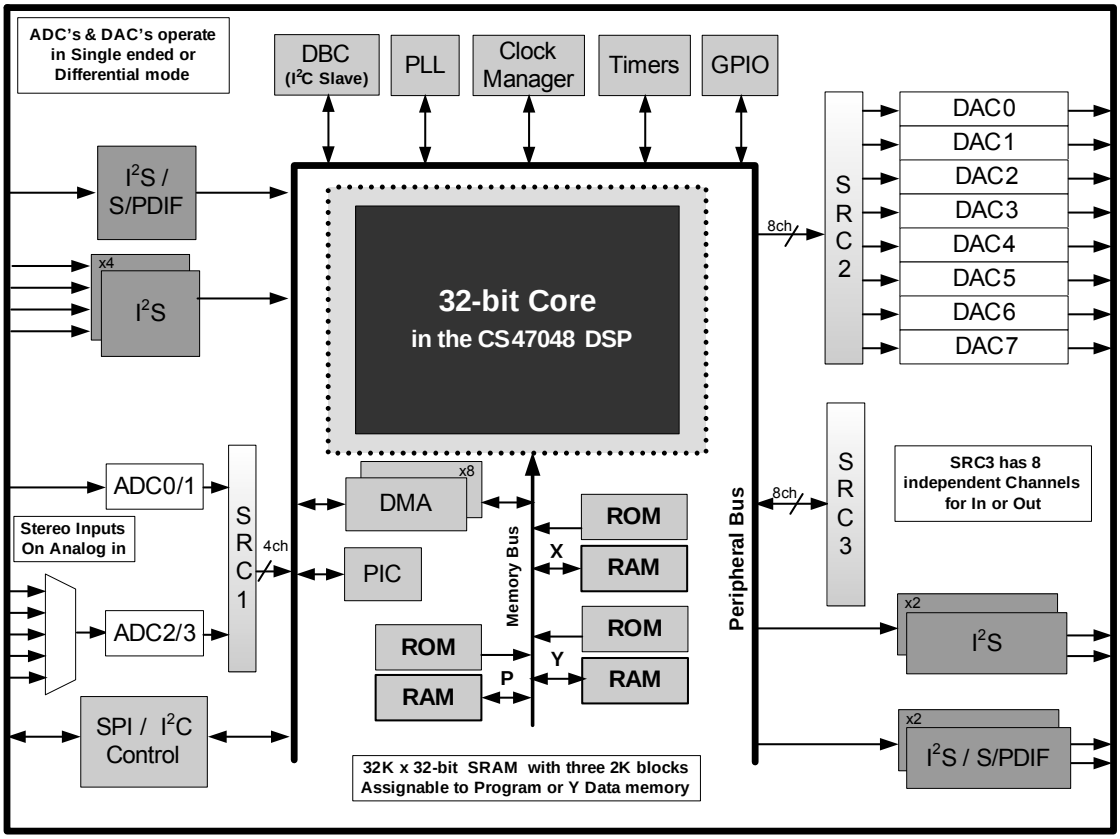


Figure 4-1. CS47048 Top-level Block Diagram

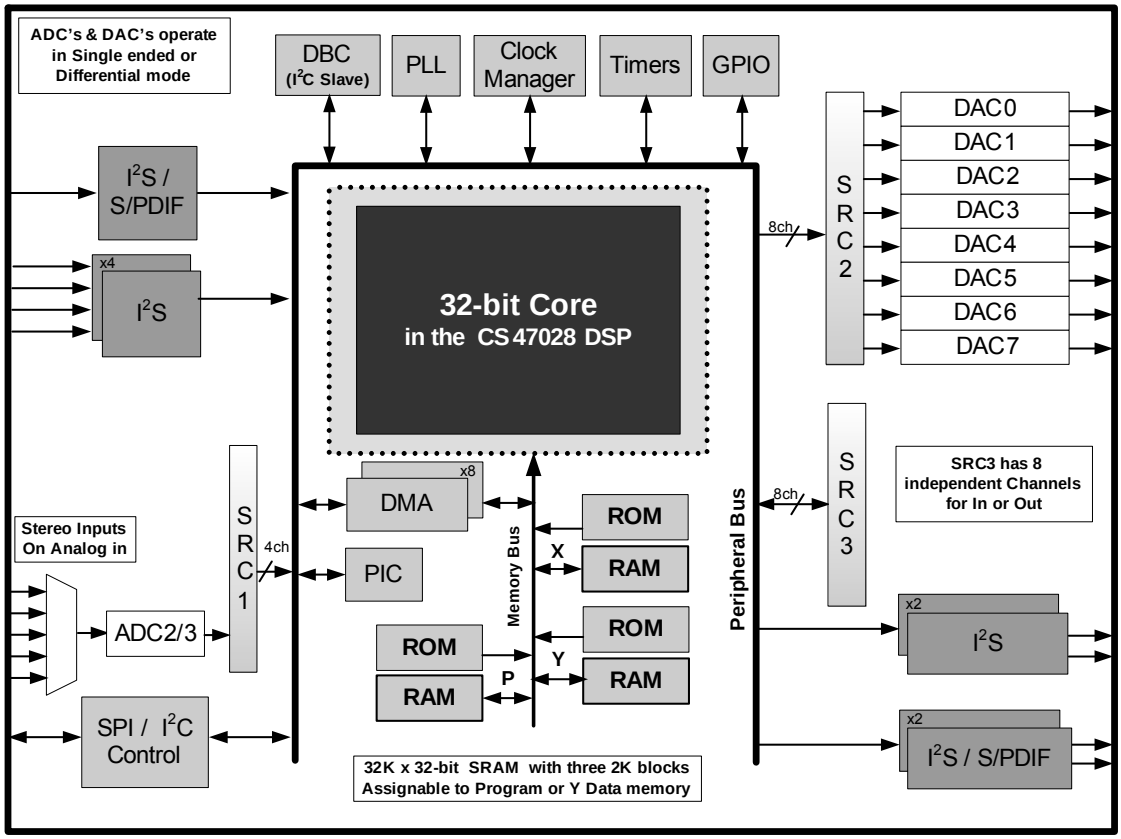


Figure 4-2. CS47028 Top-level Block Diagram

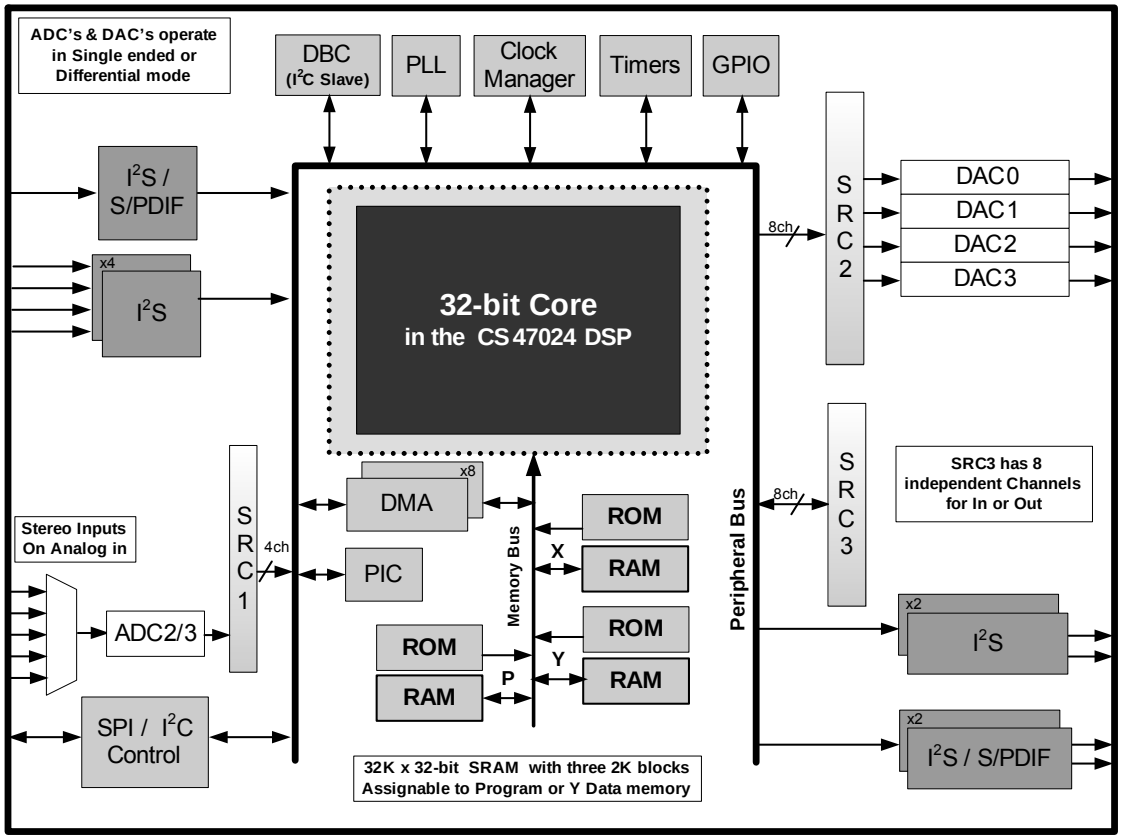


Figure 4-3. CS47024 Top-level Block Diagram

4.3.8 Serial Control Port (I²C or SPI)

The on-chip serial control port is capable of operating as master or slave in either SPI or I2C modes. Master/Slave operation is chosen by mode select pins when the CS470xx comes out of reset. The serial clock pin can support frequencies as high as 25 MHz in SPI mode (SPI clock speed must always be ≤ (DSP Core Frequency/2)). The CS470xx serial control port also includes a pin for flow control of the communications interface (SCP_BSY) and a pin to indicate when the DSP has a message for the host (SCP_IRQ).

4.3.9 GPIO

Many of the CS470xx peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.3.10 PLL-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency, which is used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS470xx defaults to running from the external reference frequency and is switched to use the PLL output after overlays have been loaded and configured, either through master boot from an external flash or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

4.3.11 Hardware Watchdog Timer

The CS470xx has an integrated watchdog timer that acts as a “health” monitor for the DSP. The watchdog timer must be reset by the DSP before the counter expires, or the entire chip is reset. This peripheral ensures that the CS470xx resets itself in the event of a temporary system failure. In stand-alone mode (where there is no host MCU), the DSP reboots from external flash. In slave mode (where the host MCU is present), a GPIO is used to signal the host that the watchdog has expired and the DSP should be rebooted and re-configured.

4.4 DSP I/O Description

4.4.1 Multiplexed Pins

Many of the CS470xx pins are multifunctional. For details on pin functionality, see Section 10.5, “Pin Assignments”, in the *CS470xx Hardware User’s Manual*.

4.4.2 Termination Requirements

Open-drain pins on the CS470xx must be pulled high for proper operation. See the *CS470xx Hardware User’s Manual* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

Mode select pins on CS470xx are used to select the boot mode on the rising edge from reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS470xx Hardware User’s Manual*.

4.4.3 Pads

The CS470xx Digital I/Os operate from the 3.3 V supply and are 5 V tolerant.

4.5 Application Code Security

The external program code can be encrypted by the programmer to protect any intellectual property it contains. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device. Contact your local Cirrus representative for details.

5.4 Power Supply Characteristics

Note: Measurements performed under operating conditions

Parameter	Min	Typ	Max	Unit
Operational Power Supply Current:				
VDD: Core and I/O operating[1]	—	325	—	mA
VDDA: PLL operating current	—	16	—	mA
VDDA: DAC operating current (all 8 channels enabled)	—	56	—	mA
VDDA: ADC operating current (all 4 channels enabled)	—	34	—	mA
VDDIO: With most ports operating	—	27	—	mA
Total Operational Power Dissipation:		1025		mW
Standby Power Supply Current:				
VDD: Core and I/O not clocked	—	410	—	µA
VDDA: PLLs halted	—	26	—	µA
VDDA: DAC disabled	—	40	—	µA
VDDA: ADC disabled	—	24	—	µA
VDDIO: All connected I/O pins 3-stated by other ICs in system	—	215	—	µA
Total Standby Power Dissipation:		1745		µW

1. Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (100-pin LQFP with Exposed Pad)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient) Two-layer Board[1] Four-layer Board[2]	θ_{ja}	 — —	 34 18	 — —	°C/Watt
Thermal Resistance (Junction to Top of Package) Two-layer Board[1] Four-layer Board[2]	ψ_{jt}	 — —	 0.54 .28	 — —	°C/Watt

1. To calculate the die temperature for a given power dissipation:
   T_j = Ambient temperature + [(Power Dissipation in Watts) * θ_{ja}]
2. To calculate the case temperature for a given power dissipation:
   $T_c = T_j$ - [(Power Dissipation in Watts) * ψ_{jt}]

Note: Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20% of the top and bottom layers.

Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20% of the top and bottom layers and 0.5-oz. copper covering 90% of the internal power plane and ground plane layers.

5.6 Digital Switching Characteristics–RESET

Parameter	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ minimum pulse width low[1]	T_{rstl}	1	—	µs
All bidirectional pins high-Z after $\overline{\text{RESET}}$ low	T_{rst2z}	—	200	ns
Configuration pins setup before $\overline{\text{RESET}}$ high	T_{rstsu}	50	—	ns
Configuration pins hold after $\overline{\text{RESET}}$ high	T_{rsthld}	20	—	ns

1. The rising edge of $\overline{\text{RESET}}$ must not occur before the power supplies are stable at the recommended operating values as described in Section 5.2. In addition, for the configuration pins to be read correctly, the $\overline{\text{RESET}}$ T_{rstl} requirement must be met.

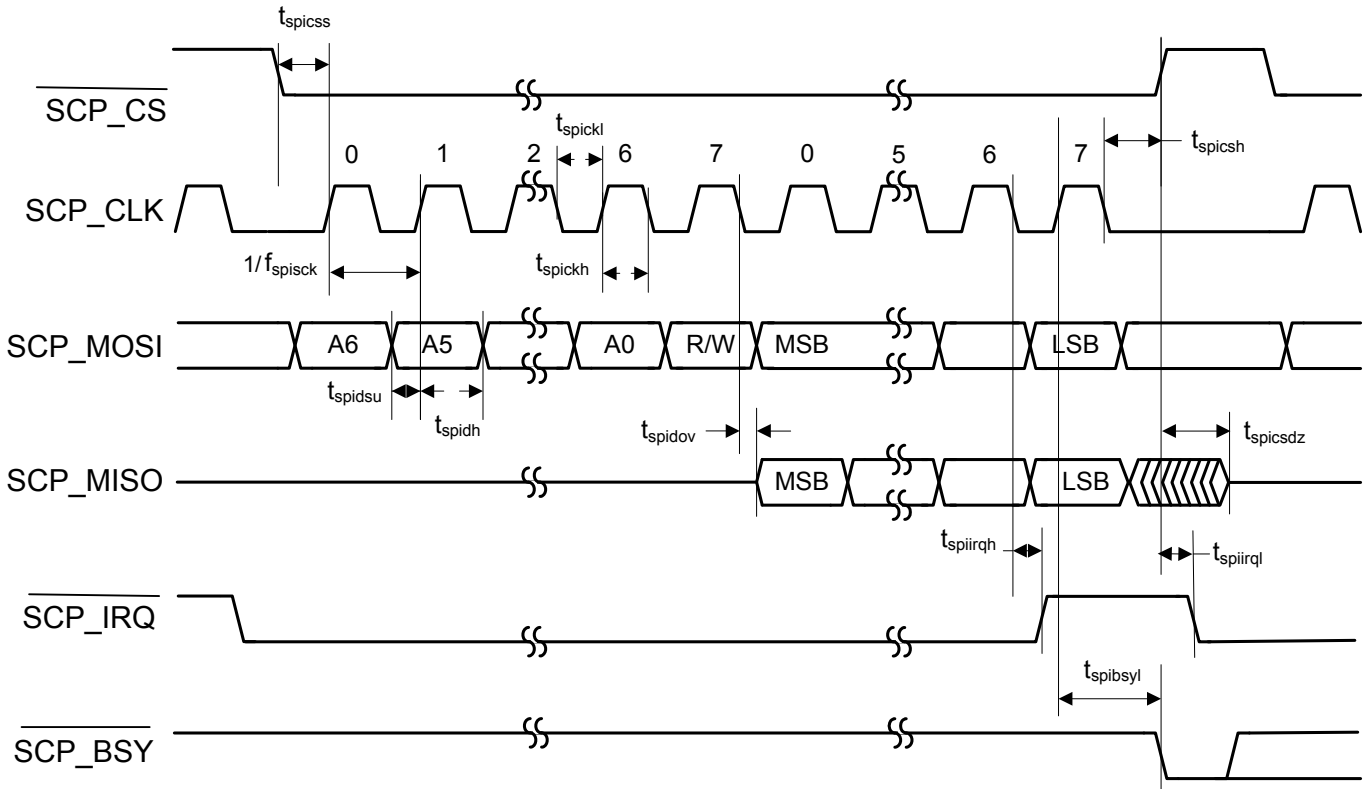


Figure 5-4. Serial Control Port–SPI Slave Mode Timing

5.10 Digital Switching Characteristics–Serial Control Port–SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1,2]	f_{spisck}	—	—	$F_{xtal}/2$	MHz
$\overline{EE\_CS}$ falling to SCP_CLK rising[3]	t_{spicss}	—	11*DCLKP+(SCP_CLK PERIOD)/2	—	ns
SCP_CLK low time	t_{spickl}	18	—	—	ns
SCP_CLK high time	t_{spickh}	18	—	—	ns
Setup time SCP_MISO input	t_{spidsu}	9	—	—	ns
Hold time SCP_MISO input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	—	—	8	ns
SCP_CLK low to $\overline{EE\_CS}$ falling	t_{spicsl}	7	—	—	ns
SCP_CLK low to $\overline{EE\_CS}$ rising	t_{spicsh}	—	11*DCLKP+(SCP_CLK PERIOD)/2	—	ns
Bus free time between active $\overline{EE\_CS}$	t_{spicsx}	—	3*DCLKP	—	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	—	—	20	ns

1. f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port can be limited by the firmware application.
2. See Section 5.7.
3. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter.

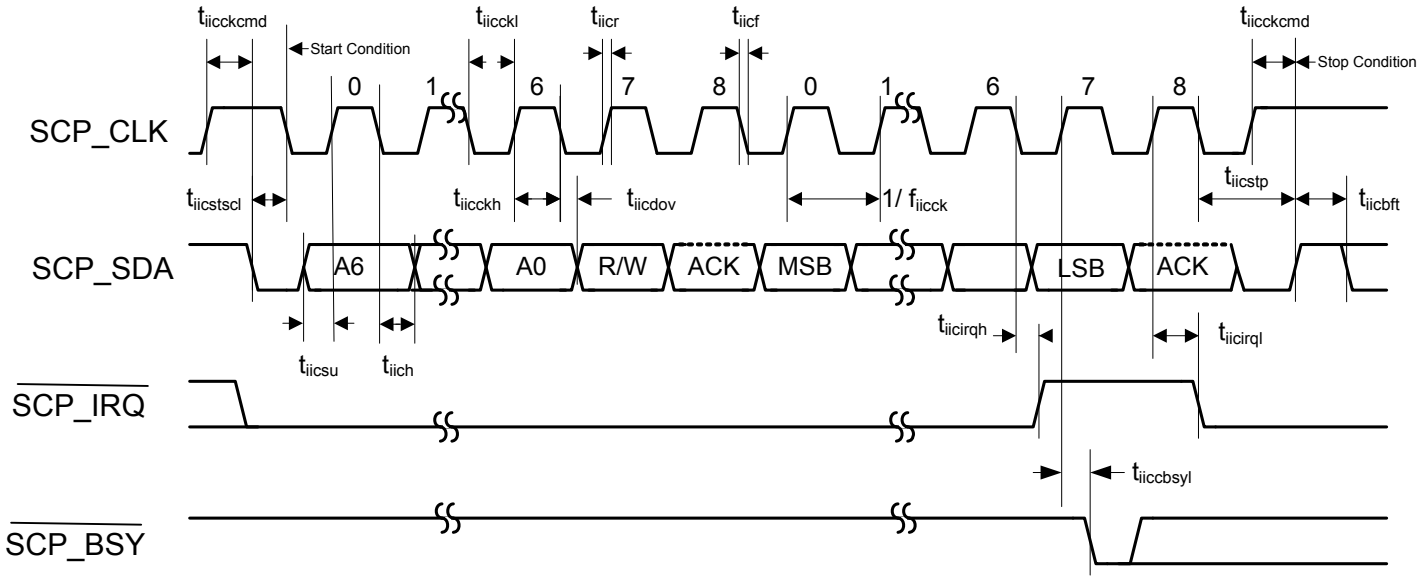


Figure 5-6. Serial Control Port–I2C Slave Mode Timing

5.12 Digital Switching Characteristics–Serial Control Port–I2C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency[1]	f_{iicck}	—	400	kHz
SCP_CLK rise time	t_{iicr}	—	150	ns
SCP_CLK fall time	t_{iicf}	—	150	ns
SCP_CLK low time	t_{iicckl}	1.25	—	µs
SCP_CLK high time	t_{iicckh}	1.25	—	µs
SCP_CLK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25	—	µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	—	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	—	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	—	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	110	—	ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	100	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	—	36	ns

1. f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port can be limited by the firmware application.

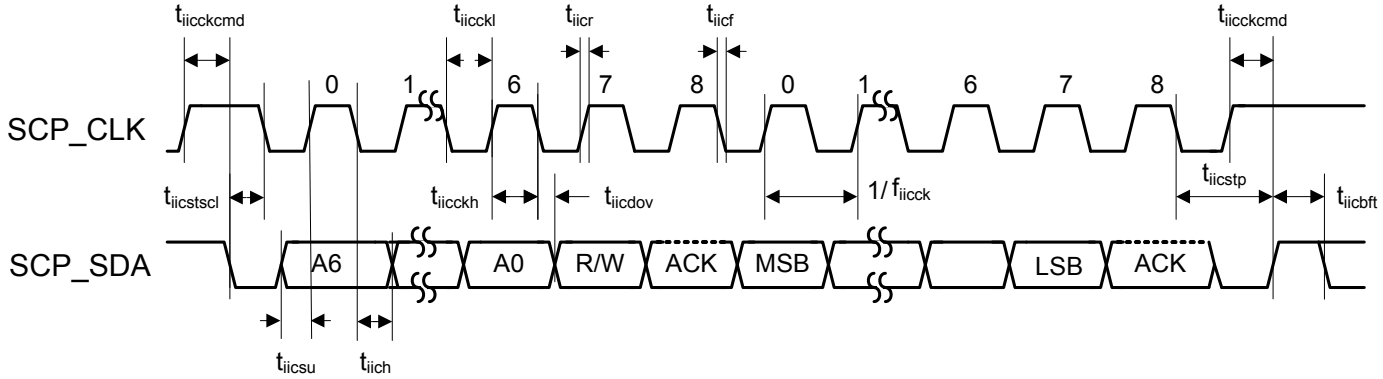


Figure 5-7. Serial Control Port–I2C Master Mode Timing

5.13 Digital Switching Characteristics–Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	20	—	ns
DAI_SCLK duty cycle	—	45	55	%
Setup time DAI_DATAn	t_{daidsu}	8	—	ns
Hold time DAI_DATAn	t_{daidh}	5	—	ns

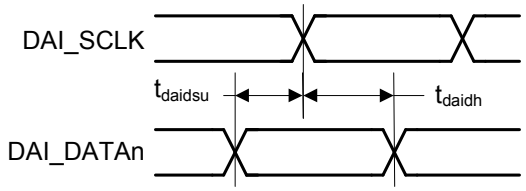


Figure 5-8. Digital Audio Input (DAI) Port Timing Diagram

5.14 Digital Switching Characteristics–Digital Audio Output Port

Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	20	—	ns
DAO_MCLK duty cycle	—	45	55	%
DAO_SCLK period for Master or Slave mode[1]	$T_{daosclk}$	20	—	ns
DAO_SCLK duty cycle for Master or Slave mode[1]	—	40	60	%
Master Mode (Output A1 Mode)[1,2]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO MCLK as an input	$t_{daomsck}$	—	19	ns
DAO_LRCLK to DAO_SCLK inactive edge[3]. See Fig. 5-9.	$t_{daomlrts}$	—	8	ns
DAO_SCLK inactive edge[3] to DAO_LRCLK. See Fig. 5-10.	$t_{daomstlr}$	—	8	ns
DAO_DATA[3:0] delay from DAO_SCLK inactive edge[3]	t_{daomdy}	—	8	ns
Slave Mode (Output A0 Mode)[4]				
DAO_SCLK active edge to DAO_LRCLK transition. See Fig. 5-11.	$t_{daosstlr}$	10	—	ns
DAO_LRCLK transition to DAO_SCLK active edge. See Fig. 5-12.	$t_{daoslrts}$	10	—	ns
DAO_Dx delay from DAO_SCLK inactive edge	t_{daosdv}	—	11	ns

1. Master mode timing specifications are characterized, not production tested.
2. Master mode is defined as the CS47048 driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.
3. The DAO_LRCLK transition can occur on either side of the edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.
4. Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.

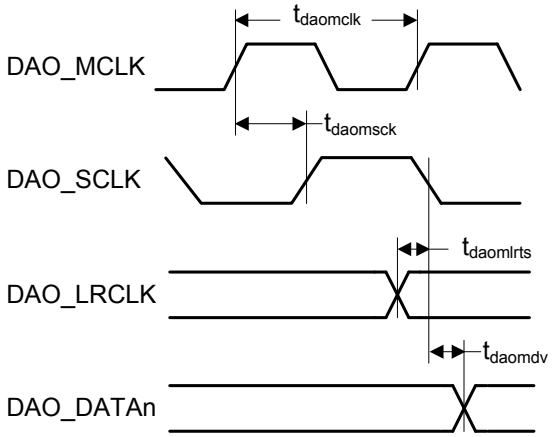


Figure 5-9. DAO_LRCLK Transition before DAO_SCLK Inactive Edge

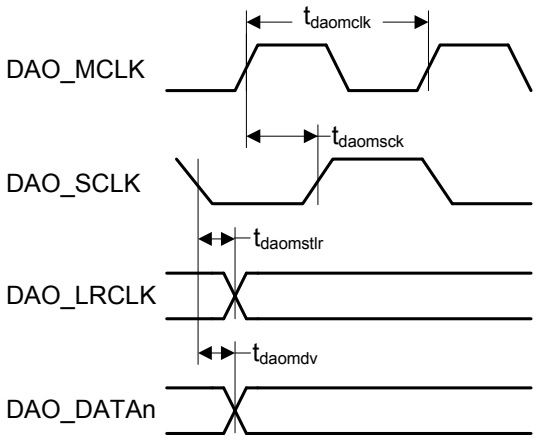


Figure 5-10. DAO_LRCLK Transition after DAO_SCLK Inactive Edge

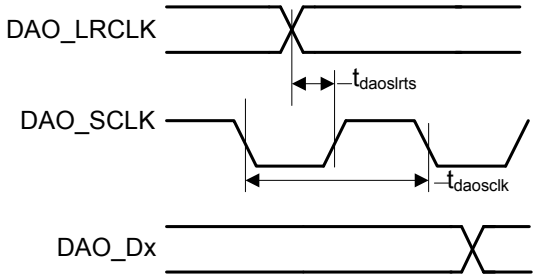


Figure 5-11. DAO_LRCLK Transition before DAO_SCLK Inactive Edge

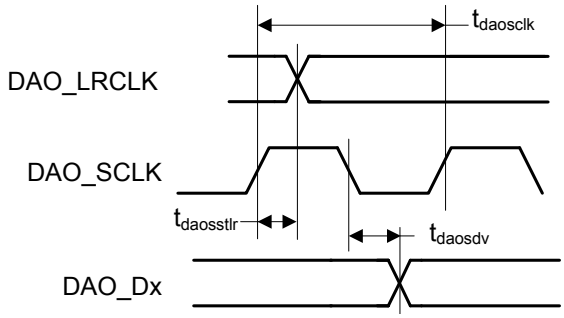


Figure 5-12. DAO_LRCLK Transition after DAO_SCLK Inactive Edge

5.15 Digital Switching Characteristics–S/PDIF RX Port

(Inputs: Logic 0 = V_{IL}, Logic 1 = V_{IH}, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
PLL Clock Recovery Sample Rate Range	—	30	—	200	kHz

5.16 ADC Characteristics

5.16.1 Analog Input Characteristics (Commercial)

Test Conditions (unless otherwise specified): T_A = 0–+70°C; VDD = 1.8V±5%, VDDA (VA) = 3.3V±5%, 1kHz sine wave driven through the passive input filter (R_i = 10 kΩ) in Fig. 5-13 or Fig. 5-14; DSP running test application; Measurement Bandwidth is 10–20kHz.

	Differential			Single-ended			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Fs = 96 kHz							
Dynamic Range[1,6,7]							
A-weighted	99	105	—	96	102	—	dB
Unweighted	96	102	—	93	99	—	dB
40 kHz bandwidth unweighted	—	99	—	—	96	—	dB
Total Harmonic Distortion + Noise[6,7]							
–1 dB	—	–98	–92	—	–95	–89	dB
–20 dB	—	–82	—	—	–79	—	dB
–60 dB	—	–42	—	—	–39	—	dB
40 kHz bandwidth –1 dB	—	–90	—	—	–90	—	dB
AIN_1A/B Interchannel Isolation[10]	—	95	—	—	95	—	dB
AID_[2.6]A/B MUX Interchannel Isolation	—	95	—	—	95	—	dB
DC Accuracy							
Interchannel Gain Mismatch	—	0.1	—	—	0.1	—	dB
Gain Drift	—	±120	—	—	±120	—	ppm/°C
Analog Input							
Full-scale Input Voltage[2,3]	3.3	3.7•VA	3.9	1.65	1.85•VA	1.95	V_{PP}
Differential Input Impedance[4]	—	400	—	—	—	—	Ω
Single-ended Input Impedance[5]	—	—	—	—	200	—	Ω
Common Mode Rejection Ratio (CMRR)[8]	—	60	—	—	—	—	dB
Parasitic Load Capacitance (C_L)[9]	—	—	20	—	—	20	pF

1. dB units referred to the typical full-scale voltage.
2. These full-scale values were measured with R_i=10k for both the single-ended and differential mode input circuits.
3. The full-scale voltage can be changed by scaling R_i.
   Differential Full-Scale (Vpp) = 3.7*VDDA*(Ri+200)/(10k+200)
   Single-Ended Full-Scale (Vpp) = 1.85*VDDA*(Ri+200)/(10k+200)
4. Measured between AIN_xx+ and AN_xx–.
5. Measured between AIN_xx+ and AGND.
6. Decreasing full-scale voltage by reducing R_i causes the noise floor to increase.
7. Common mode input current should be kept to less than ±160uA to avoid performance degradation: $|(I_{ip}+I_{in})/2| < 160uA$. This corresponds to ±1.6V for R_i=10 kΩ in the differential case.
8. This number was measured using perfectly matched external resistors (R_i). Mismatch in the external resistors typically reduces CMRR by 20 log ($|\Delta R_i|/R_i + 0.001$).
9. C_L represents the parasitic load capacitance between R_i on the input circuit and the input pin of the CS47048 package.
10. This measurement is not applicable to the CS47028 and CS47024 devices.

5.16.2 Analog Input Characteristics (Automotive)

Test Conditions (unless otherwise specified): TA = –40–85°C; VDD = 1.8V±5%, VDDA (VA) = 3.3V±5%; kHz sine wave driven through the passive input filter (R_i = 10 kΩ) in Fig. 5-13 or Fig. 5-14; DSP running test application; Measurement Bandwidth is 10 Hz–20 kHz.

	Differential			Single-ended			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Fs = 96 kHz							
Dynamic Range[1,6,7] A-weighted Unweighted 40 kHz bandwidth unweighted	 97 94 —	 105 102 99	 — — —	 94 91 —	 102 99 96	 — — —	 dB dB dB
Total Harmonic Distortion + Noise[6,7] –1 dB –20 dB –60 dB 40 kHz bandwidth –1 dB	 — — — —	 –98 –82 –42 –90	 –90 — — —	 — — — —	 –95 –79 –39 –90	 –87 — — —	 dB dB dB dB
AIN_1A/B Interchannel Isolation[10]	—	95	—	—	95	—	dB
AID_[2.6]A/B MUX Interchannel Isolation	—	95	—	—	95	—	dB
DC Accuracy							
Interchannel Gain Mismatch	—	0.1	—	—	0.1	—	dB
Gain Drift	—	±120	—	—	±120	—	ppm/°C
Analog Input							
Full-scale Input Voltage[2,3]	3.3	3.7•VA	3.9	1.65	1.85•VA	1.95	V_{PP}
Differential Input Impedance[4]	—	400	—	—	—	—	Ω
Single-ended Input Impedance[5]	—	—	—	—	200	—	Ω
Common Mode Rejection Ratio (CMRR)[8]	—	60	—	—	—	—	dB
Parasitic Load Capacitance (C_L)[9]	—	—	20	—	—	20	pF

1. dB units referred to the typical full-scale voltage.
2. These full-scale values were measured with R_i=10k for both the single-ended and differential mode input circuits.
3. The full-scale voltage can be changed by scaling R_i.
   Differential Full-Scale (Vpp) = 3.7*VDDA*(Ri+200)/(10k+200)
   Single-Ended Full-Scale (Vpp) = 1.85*VDDA*(Ri+200)/(10k+200)
4. Measured between AIN_xx+ and AN_xx–.
5. Measured between AIN_xx+ and AGND.
6. Decreasing full-scale voltage by reducing R_i causes the noise floor to increase.
7. Common mode input current should be kept to less than ±160uA to avoid performance degradation: $|(I_{ip}+I_{in})/2| < 160uA$. This corresponds to ±1.6V for R_i=10 kΩ in the differential case.
8. This number was measured using perfectly matched external resistors (R_i). Mismatch in the external resistors typically reduces CMRR by 20 log ($|\Delta R_i|/R_i + 0.001$).
9. C_L represents the parasitic load capacitance between R_i on the input circuit and the input pin of the CS47048 package.
10. This measurement is not applicable to the CS47028 and CS47024 devices.

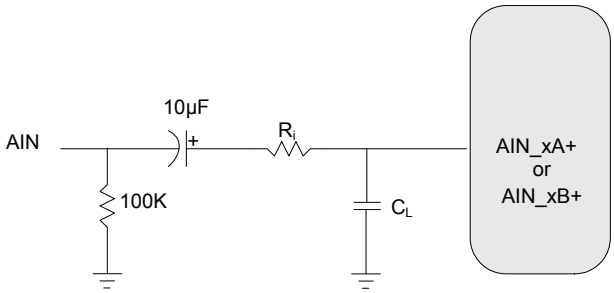


Figure 5-13. ADC Single-ended Input Test Circuit

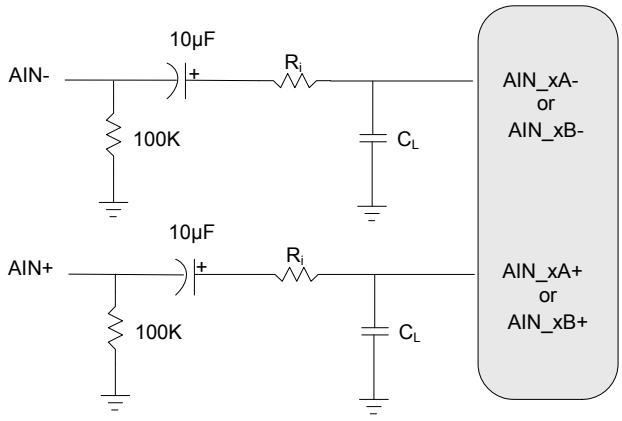


Figure 5-14. ADC Differential Input Test Circuit

5.16.3 ADC Digital Filter Characteristics

Parameter[1,2]	Min	Typ	Max	Unit
Fs = 96 kHz				
Passband (Frequency Response) to –0.1 dB corner	0	—	0.4896	Fs
Passband Ripple	—	—	0.08	dB
Stopband	0.5688	—	—	Fs
Stopband Attenuation	70	—	—	dB
Total Group Delay	—	12/Fs	—	s
High-pass Filter Characteristics				
Frequency Response: –3.0 dB –0.13 dB	 — —	 1 20	 — —	 Hz Hz
Phase Deviation @ 20 Hz	—	10	—	Deg
Passband Ripple	—	—	0	dB
Filter Settling Time	—	10^5/Fs	0	s

1. Filter response is guaranteed by design.
2. Response is clock-dependent and scales with Fs.

5.17 DAC Characteristics

5.17.1 Analog Output Characteristics (Commercial)

Test Conditions (unless otherwise specified): TA = 0–+70°C; VDD = 1.8V±5%, VDDA(VA) = 3.3V±5%; 1 kHz sine wave driven through a filter shown in Fig. 5-15 or Fig. 5-16; DSP running test application; Measurement Bandwidth is 20 Hz–20 kHz.

	Differential			Single-ended			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Fs = 96 kHz							
Dynamic Range A-weighted Unweighted	 102 99	 108 105	 — —	 99 96	 105 102	 — —	 dB dB
Total Harmonic Distortion + Noise 0 dB –20 dB –60 dB	 — — —	 –98 –88 –48	 –90 — —	 — — —	 –95 –85 –45	 –87 — —	 dB dB dB
Interchannel Isolation (1 kHz)	—	95	—	—	95	—	dB

	Differential			Single-ended			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Analog Input							
Full-scale Output	1.20	1.40•VA	1.60	0.60	0.70•VA	0.80	V_{PP}
Interchannel Gain Mismatch	—	0.1	—	—	0.1	—	dB
Gain Drift	—	±120	—	—	±120	—	ppm/°C
Output Impedance	—	100	—	—	100	—	Ω
DC Current Draw from an AOUT Pin[1]	—	—	10	—	—	10	µA
AC-load Resistance (R_L)[2]	3	—	—	3	—	—	kΩ
Load Capacitance (C_L)[2]	—	—	100	—	—	100	pF

5.17.2 Analog Output Characteristics (Automotive)

Test Conditions (unless otherwise specified): T_A = –40 to +85°C; VDD = 1.8V±5%, VDDA(VA) = 3.3V±5%; 1 kHz sine wave driven through a filter shown in Fig. 5-15 or Fig. 5-16; DSP running test application; Measurement Bandwidth is 20 Hz–20 kHz.

	Differential			Single-ended			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Fs = 96 kHz							
Dynamic Range A-weighted Unweighted	 100 97	 108 105	 — —	 97 94	 105 102	 — —	 dB dB
Total Harmonic Distortion + Noise 0 dB –20 dB –60 dB	 — — —	 –98 –88 –48	 –90 — —	 — — —	 –95 –85 –45	 –87 — —	 dB dB dB
Interchannel Isolation (1 kHz)	—	95	—	—	95	—	dB
Analog Input							
Full-scale Output	1.20	1.40•VA	1.60	0.60	0.70•VA	0.80	V_{PP}
Interchannel Gain Mismatch	—	0.1	—	—	0.1	—	dB
Gain Drift	—	±120	—	—	±120	—	ppm/°C
Output Impedance	—	100	—	—	100	—	Ω
DC Current Draw from an AOUT Pin[1]	—	—	10	—	—	10	µA
AC-load Resistance (R_L)[2]	3	—	—	3	—	—	kΩ
Load Capacitance (C_L)[2]	—	—	100	—	—	100	pF

1. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC-blocking capacitors.
2. Guaranteed by design. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L represents any capacitive loading that appears *before* the 560 Ω series resistor (typically parasitic), and effectively moves the dominant pole of the two-pole amp in the output stage. Increasing this value beyond the recommended 100 pF can cause the internal op-amp to become unstable.

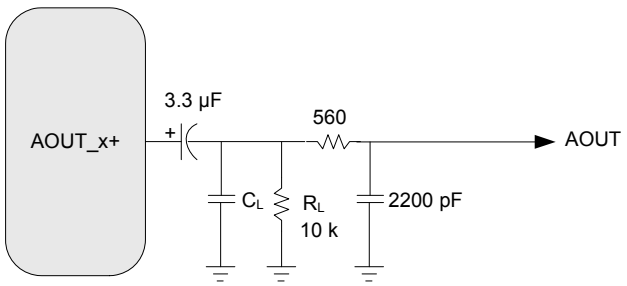
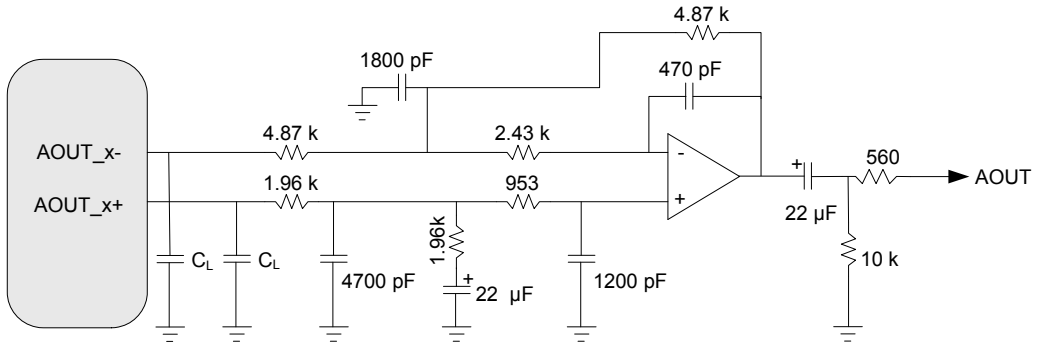


Figure 5-15. DAC Single-ended Output Test Circuit



P output: $R_L = 1.96k + ([2\pi F*4700pF]^{-1} || (1.96k + [2\pi F*22\mu F^{-}]^{-1}) || (953 + [2\pi F*1200pF]^{-1}))$

N output: $R_L = 4.87k + ([2\pi F*1800pF]^{-1} || ((2.43k + [2\pi F*470pF]^{-1}) || 4.87k))$

Figure 5-16. DAC Differential Output Test Circuit

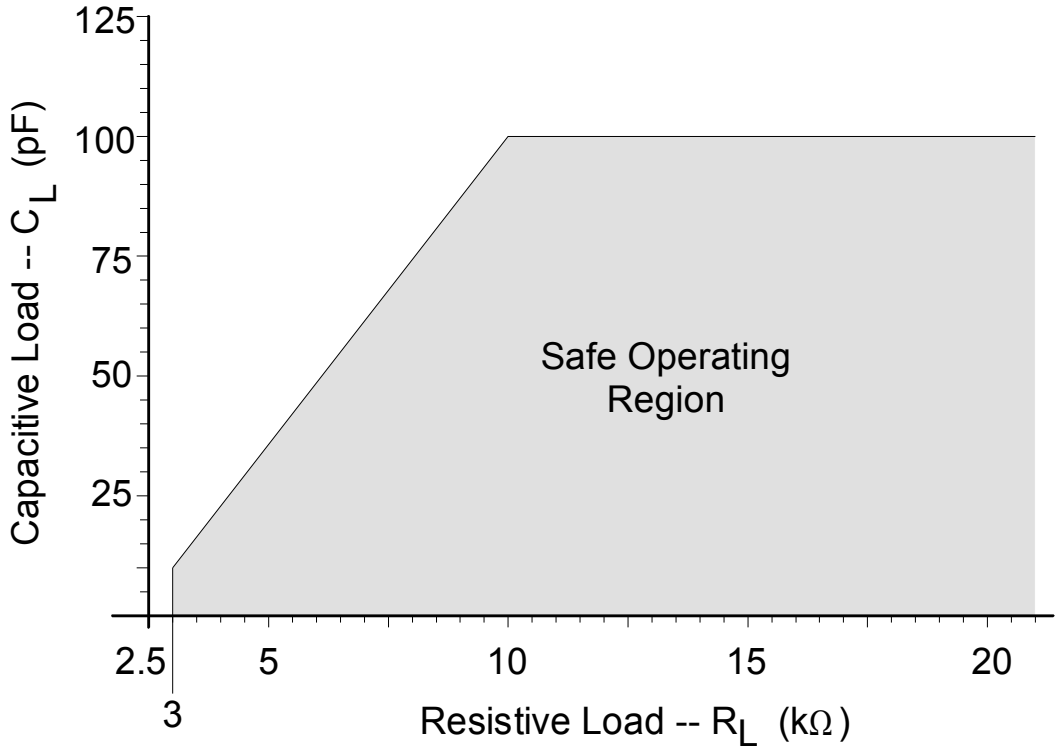


Figure 5-17. Maximum Loading

5.17.3 Combined DAC Interpolation and On-chip Analog Filter Response

Parameter	Min	Typ	Max	Unit
Passband (Frequency Response) to 0.22 dB corner to –3 dB corner	 0 0	 — —	 0.4125 0.4979	 Fs Fs
Frequency Response 10 Hz–20 kHz	–0.02	—	+0.02	dB
StopBand	0.5465	—	—	Fs
StopBand Attenuation	100	—	—	dB
Group Delay	—	10/Fs	—	s

6 Ordering Information

The CS470xx DSP part numbers are described as follows:

Example:
CS47048I-XYZR
where
I–ROM ID Letter
X–Product Grade
Y–Package Type
Z–Lead (Pb) Free
R–Tape and Reel Packaging

Table 6-1. Ordering Information

Part No.	Grade	Temp. Range	Package
CS47048C-CQZ	Commercial	0–+70°C	100-pin LQFP
CS47048C-DQZ	Automotive	–40–+85°C	
CS47048C-EQZ	Extended Automotive	–40–+105°C	
CS47028C-CQZ	Commercial	0–+70°C	
CS47028C-DQZ	Automotive	–40–+85°C	
CS47028C-EQZ	Extended Automotive	–40–+105°C	
CS47024C-CQZ	Commercial	0–+70°C	
CS47024C-DQZ	Automotive	–40–+85°C	
CS47024C-EQZ	Extended Automotive	–40–+105°C	

Note: Contact the factory for availability of the –D (automotive grade) package.

7 Environmental, Manufacturing, and Handling Information

Table 7-1. Environmental, Manufacturing, and Handling Information

Model Number	Peak Reflow Temp.	MSL[1] Rating	Max Floor Life
CS47048C-CQZ	260° C	3	7 days
CS47048C-DQZ			
CS47048C-EQZ			
CS47028C-CQZ	260° C	3	7 days
CS47028C-DQZ			
CS47028C-EQZ			
CS47024C-CQZ	260° C	3	7 days
CS47024C-DQZ			
CS47024C-EQZ			

1. Moisture Sensitivity Level as specified by IPC/JEDEC J-STD-020.

8.2 CS47028, 100-pin LQFP Pinout Diagram

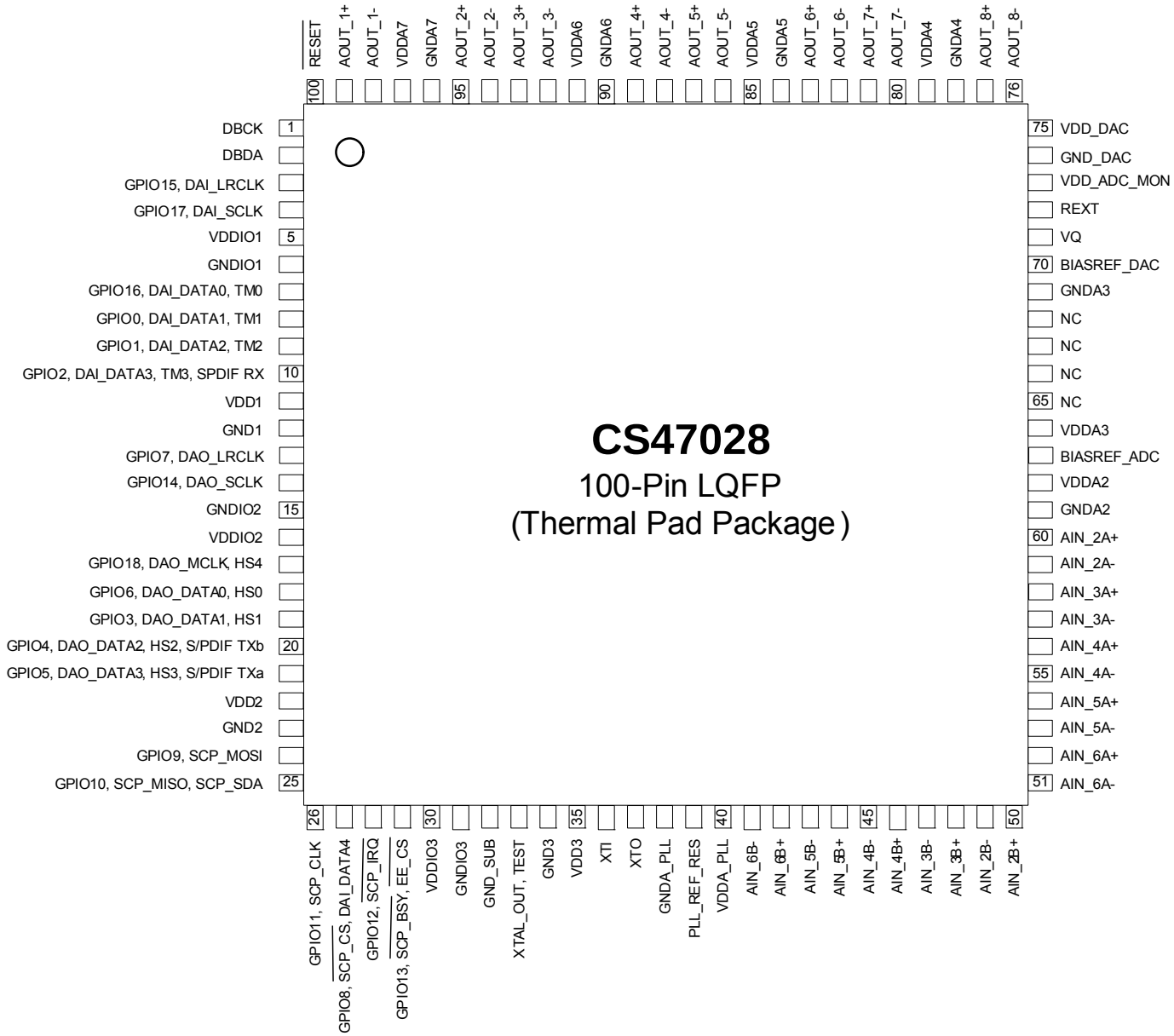
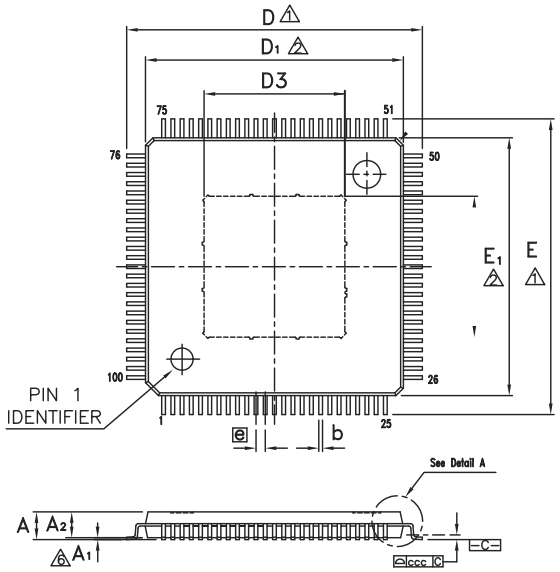
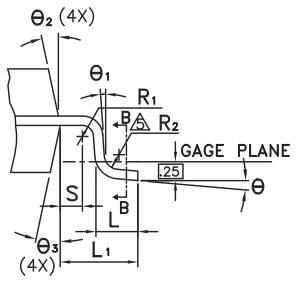


Figure 8-2. CS47028 Pinout Diagram

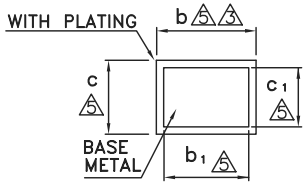
9 100-pin LQFP with Exposed Pad Package Drawing

Fig. 9-1 shows the 100-pin LQFP package with exposed pad for the CS47048, CS47028, and CS47024.





DETAIL A



SECTION B–B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP					
θ3						
ccc	0.08			0.003		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026.
9. **SPECIAL CHARACTERISTICS C CLASS: ccc**

Exposed Pad Size		
L/F	Dimension in mm	Dimension in inch
D3/E3	7.62 REF	0.300 REF

100LD E–PAD LQFP (14x14x1.4mm) PACKAGE OUTLINE
–Cu L/F,FOOTPRINT 2.0mm

Figure 9-1. 100-pin LQFP Package Drawing

10 Parameter Definitions

10.1 Dynamic Range

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

10.2 Total Harmonic Distortion + Noise

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth (typically 10 Hz–20 kHz), including distortion components. Expressed in decibels. Measured at –1 and –20 dBFS as suggested in AES17-1991 Annex A.

10.3 Frequency Response

A measure of the amplitude response variation from 10 Hz–20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

10.4 Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

10.5 Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

10.6 Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

10.7 Gain Drift

The change in gain value with temperature. Units in ppm/°C.

11 Revision History

Revision	Date	Changes
PP1	August, 2009	Updated Characterization data in Section 5.4, Section 5.7, Section 5.9, Section 5.11, Section 5.12, Section 5.16.1, Section 5.16.2, Section 5.16.3, Section 5.17.1, and Section 5.17.2. Modified Footnote 3 in both Section 5.16.1 and Section 5.16.2. Added Footnote 5 to Section 5.14. Updated Section 2.1. Modified Section 4.3.6 and Section 4.3.8. Modified references to TDM in various sections of the data sheet.
PP2	January, 2010	Updated TDM Feature description on page 1. Modified note at the bottom of the feature list on page 1. Updated table in Section 5.8, specifying performance data for 2- and 4-layer boards. Updated Table 3-1 and Table 3-2 Updated block diagrams in Fig. 4-1, Fig. 4-2, and Fig. 4-3.
PP3	June, 2010	Table 3-1: Straddled all three columns in the “Supports Different Fs Sample Rates” row to indicate that CS47024 devices have the same features as the CS47048 and CS47028. Added “The CS47024 has the 8-channel SRC block” to Section 4.3.7. Added text in the following places to indicate that the CS47024 implements the S/PDIF Rx functionality: • Removed dagger from the S/PDIF Rx bullet on p. 1. • Updated bullet in “Configurable Serial Audio Inputs/Outputs” row in Table 2 Integrated 192 kHz S/PDIF Rx, 2 Integrated 192 kHz S/PDIF Tx. • Changed entry in “S/PDIF In (Stereo Pairs)” column in Table 3-2. • Updated I2S block in Table 3-2. • Removed text “On the CS47048 and CS47028...” from Section 4.3.4. • Removed “(Not available on CS47024)” from the heading to Section 5.15. • Described additional support for TDM 8-channel output mode on CS47024. • Removed dagger from the TDM I/O bullet on p. 1. • Straddled “Configurable Serial Audio Inputs/Outputs” row in Table 3-1. • Changed cell in “TDM Out” column in Table 3-2. • Removed text “On the CS47048 and CS47028...” from Section 4.3.5.
PP4	February, 2011	Added “Decoder” information to Section 3. Changed the name of the core to “Cirrus Logic 32-bit core”.
PP5	February, 2011	Added “SPDIF RX” to Fig. 5-17.
PP6	June, 2011	In Section 4.3.1 and Section 4.3.7, removed mention of 192 kHz sampling frequency. Updated temperature operating conditions in Section 5.2. Updated pin 33 to XTAL_OUT, TEST in Fig. 8-1, Fig. 8-2, and Fig. 8-3.
PP7	April, 2012	Corrected peak reflow temperature in Table 7-1.
PP8	June, 2012	Added number of bits to Integrated DAC and ADC Functionality on the cover page.
PP9	July, 2012	Updated frequencies in Section 5.2. Added extended automotive grade information to Section 6 and Section 7.