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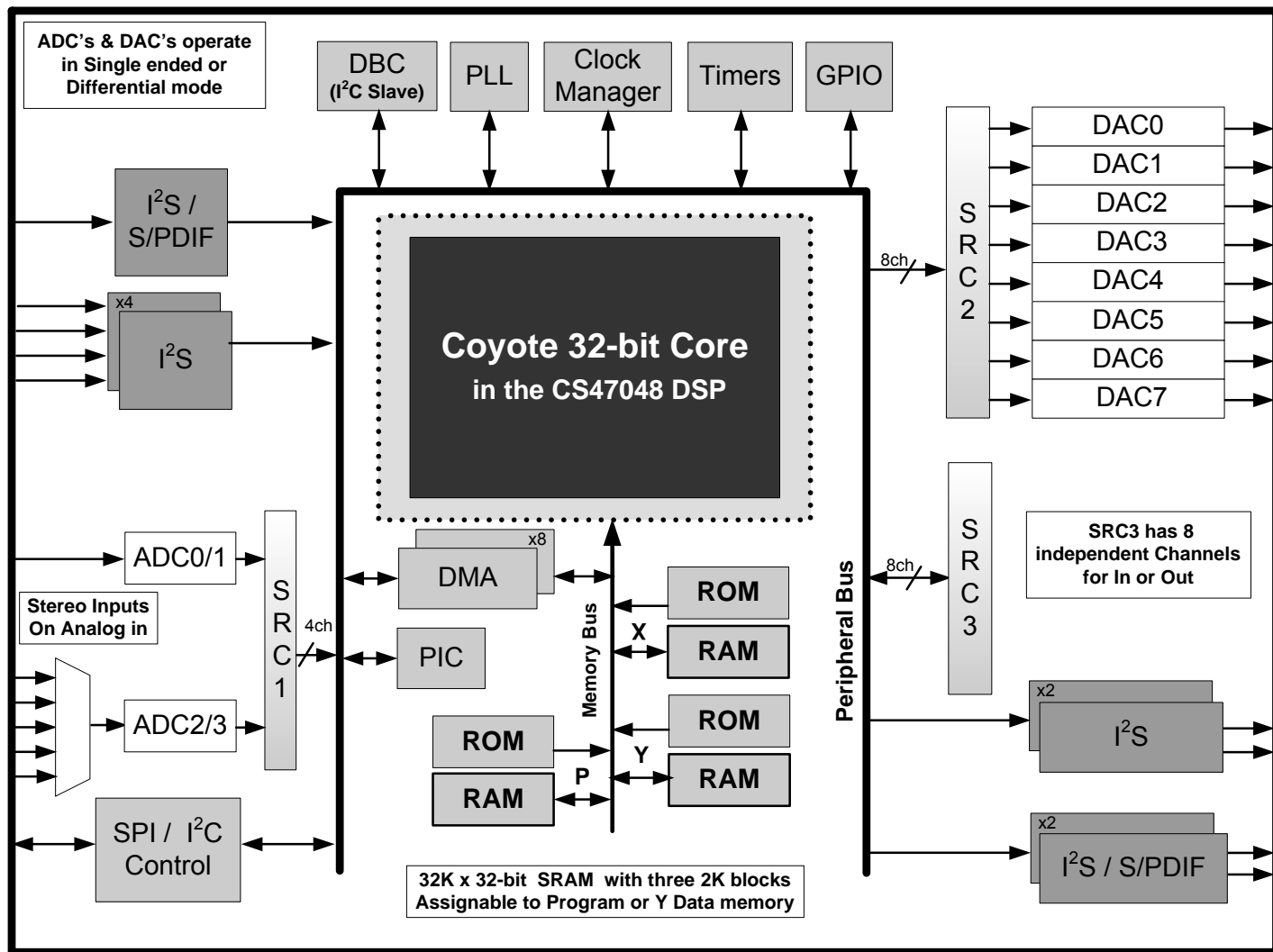
Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Active
Type	Fixed Point
Interface	I ² C, SPI
Clock Rate	150MHz
Non-Volatile Memory	-
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/cs47048c-cqz



CS47048 Block Diagram

1 Documentation Strategy

The CS470xx Data Sheet describes the CS47048, CS47028, and CS47024 audio processors. This document should be used in conjunction with the following documents when evaluating or designing a system around the CS470xx processors.

Table 1-1. CS470xx Related Documentation

Document Name	Description
CS470xx Data Sheet	This document
CS470xx Hardware User's Manual Guide	Includes detailed system design information such as typical connection diagrams, boot-procedures, and pin descriptions
AN333 - CS470xx Firmware User's Manual	Includes a list of firmware modules available on the CS470xx family platform and detailed firmware design information including signal processing flow diagrams and control API information
DSP Composer User's Manual	Includes detailed configuration and usage information for the GUI development tool
CDB470xx User's Manual	Includes detailed instructions on the use of the CDB470xx development board

The scope of the CS470xx Data Sheet is primarily the hardware specifications of the CS470xx family of devices. This includes hardware functionality, characteristic data, pinout, and packaging information.

The intended audience for the CS470xx Data Sheet is the system PCB designer, MCU programmer, and the quality control engineer.

2 Overview

The CS470xx DSP is designed to provide high-performance post-processing and mixing of analog and digital audio. Dual clock domains are supported when the DAI and SPDIF RX inputs are used together. Integrated sample rate converters (SRCs) allow audio streams with different sample rates to be mixed. The low-power standby preserves battery life for applications that are always on, but not necessarily processing audio, such as automotive audio systems.

The CS470xx uses voltage-out DACs and is capable of supporting dual input clock domains through the use of the internal SRCs. The CS470xx is available in a 100-pin LQFP package. Refer to Table 3-1 and Table 3-2 for the input, output, and firmware configurations for the CS470xx DSP.

2.1 Licensing

Licenses are required for any third-party audio processing algorithms provided for the CS470xx. Contact your local Cirrus Logic Sales representative for more information.

3 Code Overlays

The suite of software available for the CS470xx family consists of an operating system (OS) and a library of overlays. The software components for the CS470xx family include:

1. *OS/Kernel*—Encompasses all non-audio processing tasks, including loading data from external serial memory, processing host messages, calling audio-processing subroutines, error concealment, etc.
2. *Decoder*—Any module that performs a compressed audio decode on IEC61937-packed data delivered via S/PDIF Rx or I²S input, such as Dolby Digital (AC3).
3. *Matrix-processor*—Any Module that performs a matrix decode on PCM data to produce more output channels than input channels (2Æn channels). Examples are Dolby® Pro Logic® IIx and SRS Circle Surround II®. Generally speaking, these modules increase the number of valid channels in the audio I/O buffer.
4. *Virtualizer-processor*—Any module that encodes PCM data into fewer output channels than input channels (nÆ2 channels) with the effect of providing “phantom” speakers to represent the physical audio channels that were eliminated. Examples are Dolby Headphone® 2 and Dolby® Virtual Speaker® 2. Generally speaking, these modules reduce the number of valid channels in the audio I/O buffer.
5. *Post-processors*—Any module that processes audio I/O buffer PCM data. Examples are bass management, audio manager, tone control, EQ, delay, customer-specific effects, and any post-processing algorithms available for the CS470xx DSP.

The bulk of standard overlays are stored in ROM within the CS470xx, but a small image is required to configure the overlays and boot the DSP. This small image can either be stored in an external serial flash/EEPROM, or downloaded via a host controller through the SPI/I²C serial port.

The overlay structure reduces the time required to reconfigure the DSP when a processing change is requested. Each overlay can be reloaded independently without disturbing the other overlays. For example, when a different post-processor is selected, the OS, does not need to be reloaded—only the new post-processor.

Table 3-1 lists the different configuration options available. Refer to the CS470xx Firmware User’s Manual for the latest listing of application codes and Cirrus Framework™ modules available. See Table 3-2, which provides a summary of the available channels for each type of input and output communication mode for members of the CS470xx family of DSPs.

Table 3-1. CS470xx Device Selection Guide

Features	CS47048-CQZ CS47048-DQZ	CS47028-CQZ CS47028-DQZ	CS47024-CQZ CS47024-DQZ
Primary Applications	<ul style="list-style-type: none"> 4-In/8-Out Car Audio High-end Digital TV Dual Source/Dual Zone 	<ul style="list-style-type: none"> 2-In/8-Out Car Audio Sound Bar DVD Receiver 	<ul style="list-style-type: none"> 2-In/4-Out Car Audio Digital TV Portable Audio Docking Station Portable DVD DVD Mini / Receiver Multimedia PC Speakers
Package	100-pin LQFP with Exposed Pad		
DSP Core	Cirrus Logic 32-bit Core		
SRAM	32K x 32-bit SRAM with three 2K blocks x 32-bit SRAM, assignable to either Y data or program memory		
Integrated DAC and ADC	<ul style="list-style-type: none"> 2 Channels of ADC input: with integrated 5:1 analog mux 2 additional channels of ADC input: without mux 8 channels of DAC output 	<ul style="list-style-type: none"> 2 channels of ADC input: with integrated 5:1 analog mux 8 channels of DAC output 	<ul style="list-style-type: none"> 2 channels of ADC input: with integrated 5:1 analog mux 4 channels of DAC output
Configurable Serial Audio Inputs/Outputs	<ul style="list-style-type: none"> Integrated 192 kHz S/PDIF Rx, 2 Integrated 192 kHz S/PDIF Tx I2S support for 32-bit Samples @ 192 kHz TDM Input modes (Up to 8 channels) TDM Output modes (Up to 8 channels) 		
Supports Different Fs Sample Rates	<ul style="list-style-type: none"> Integrated hardware SRC blocks for all ADC and DAC channels Additional 8-channel hardware SRC block Dual-domain Fs on inputs (I2S and S/PDIF Rx) Output can be master or slave 		
Other Features	<ul style="list-style-type: none"> Integrated Clock Manager/PLL with flexibility to operate from internal PLL, external crystal, external oscillator Host Control and Boot via SPI/I²C Serial Interface DSP Tool Set w/ Private Keys Protect Customer IP Configurable GPIOs and External Interrupts Hardware Watchdog Timer 		

Table 3-2. CS470xx Channel Count

Product	PCM/TDM In ¹	TDM Out ¹	PCM Out	ADC with 5:1 Input Mux	ADC without Mux	DAC Out	S/PDIF In (Stereo Pairs)	S/PDIF Out (Stereo Pairs)
CS47048	<ul style="list-style-type: none"> Up to 5 I2S lines, 2 channels per line or 1 TDM line, up to 8 channels per line. 	Up to 8 channels	8	2	2	8	1	2
CS47028	<ul style="list-style-type: none"> Up to 5 I2S lines, 2 channels per line or 1 TDM line, up to 8 channels per line. 	Up to 8 channels	8	2	0	8	1	2
CS47024	<ul style="list-style-type: none"> Up to 5 I2S lines, 2 channels per line or 1 TDM line, up to 8 channels per line. 	Up to 8 channels	8	2	0	4	1	2

1. Contact your Cirrus Logic representative to determine the TDM modes that are supported. The CS470xx can support up to 8 channels per line, but the DSP software provided for the IC can restrict this capability.

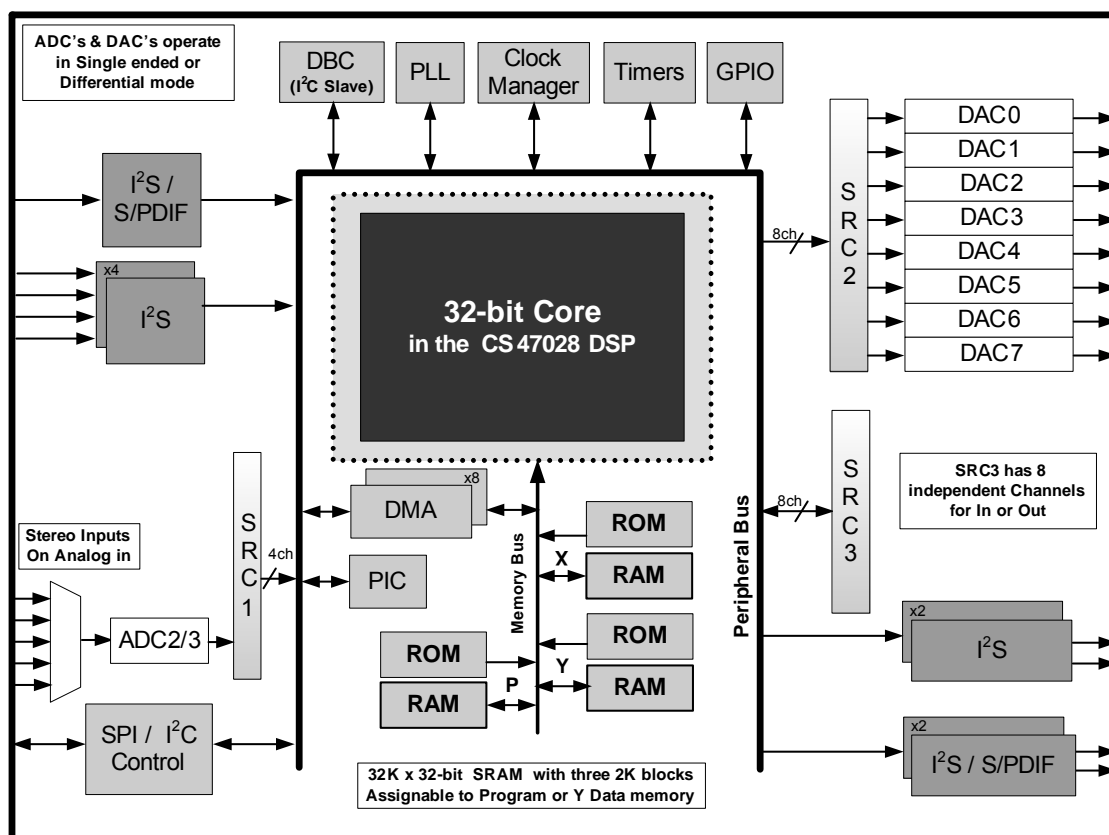


Figure 4-2. CS47028 Top-level Block Diagram

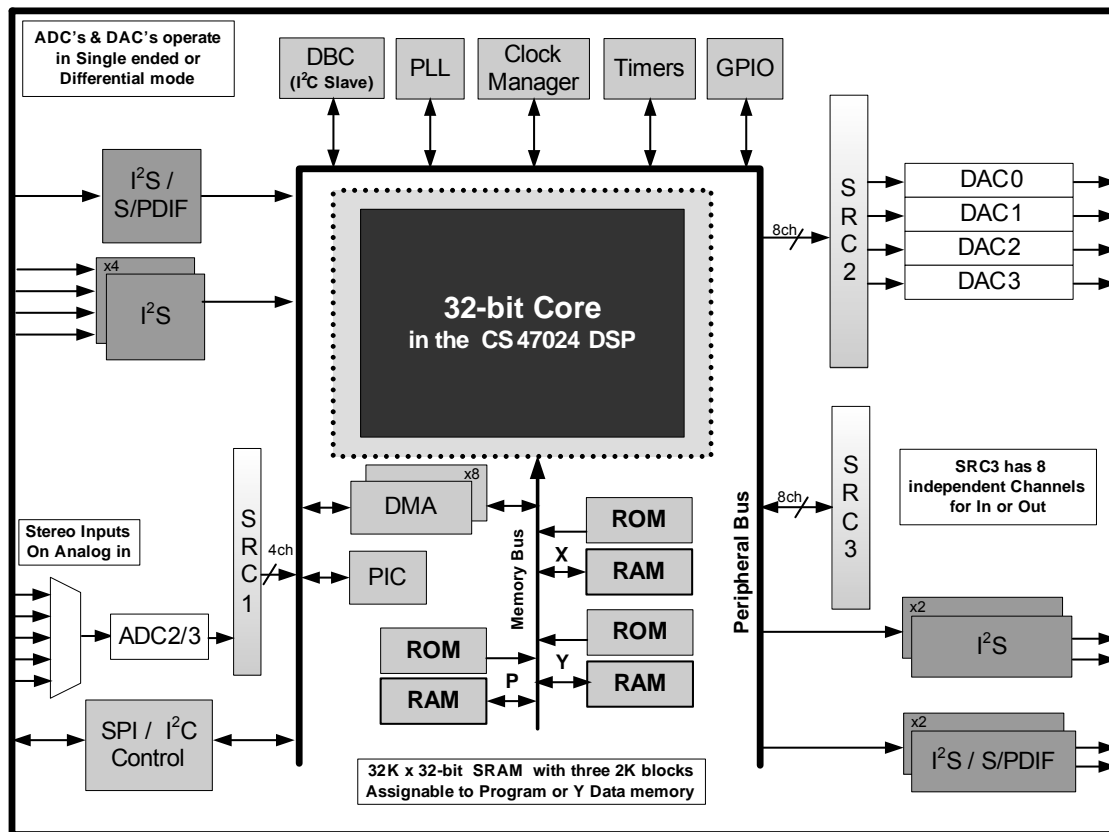


Figure 4-3. CS47024 Top-level Block Diagram

4.3.8 Serial Control Port (I²C or SPI)

The on-chip serial control port is capable of operating as master or slave in either SPI or I²C modes. Master/Slave operation is chosen by mode select pins when the CS470xx comes out of reset. The serial clock pin can support frequencies as high as 25 MHz in SPI mode (SPI clock speed must always be \leq (DSP Core Frequency/2)). The CS470xx serial control port also includes a pin for flow control of the communications interface (SCP_BSY) and a pin to indicate when the DSP has a message for the host (SCP_IRQ).

4.3.9 GPIO

Many of the CS470xx peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.3.10 PLL-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency, which is used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS470xx defaults to running from the external reference frequency and is switched to use the PLL output after overlays have been loaded and configured, either through master boot from an external flash or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

4.3.11 Hardware Watchdog Timer

The CS470xx has an integrated watchdog timer that acts as a “health” monitor for the DSP. The watchdog timer must be reset by the DSP before the counter expires, or the entire chip is reset. This peripheral ensures that the CS470xx resets itself in the event of a temporary system failure. In stand-alone mode (where there is no host MCU), the DSP reboots from external flash. In slave mode (where the host MCU is present), a GPIO is used to signal the host that the watchdog has expired and the DSP should be rebooted and re-configured.

4.4 DSP I/O Description

4.4.1 Multiplexed Pins

Many of the CS470xx pins are multifunctional. For details on pin functionality, see Section 10.5, “Pin Assignments”, in the *CS470xx Hardware User’s Manual*.

4.4.2 Termination Requirements

Open-drain pins on the CS470xx must be pulled high for proper operation. See the *CS470xx Hardware User’s Manual* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

Mode select pins on CS470xx are used to select the boot mode on the rising edge from reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS470xx Hardware User’s Manual*.

4.4.3 Pads

The CS470xx Digital I/Os operate from the 3.3 V supply and are 5 V tolerant.

4.5 Application Code Security

The external program code can be encrypted by the programmer to protect any intellectual property it contains. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device. Contact your local Cirrus representative for details.

5 Characteristics and Specifications

Note: All data sheet minimum and maximum timing parameters are guaranteed over the rated voltage and temperature. All data sheet typical parameters are measured under the following conditions: $T = 25^{\circ}\text{C}$, $V_{\text{DD}} = 1.8\text{ V}$, $V_{\text{DDIO}} = V_{\text{DDA}} = 3.3\text{ V}$, $\text{GND} = \text{GNDIO} = \text{GNDA} = 0\text{ V}$.

5.1 Absolute Maximum Ratings

($\text{GND} = \text{GNDIO} = \text{GNDA} = 0\text{V}$; all voltages with respect to 0V)

Parameter	Symbol	Min	Max	Unit
DC power supplies:				
Core supply	V_{DD}	-0.3	2.0	V
Analog supply	V_{DDA}	-0.3	3.6	V
I/O supply	V_{DDIO}	-0.3	3.6	V
$ V_{\text{DDA}} - V_{\text{DDIO}} $		—	0.3	V
Input pin current, any pin except supplies	I_{in}	—	± 10	mA
Input voltage on PLL_REF_RES	V_{filt}	-0.3	3.6	V
Input voltage on digital I/O pins	V_{inio}	-0.3	5.0	V
Analog Input Voltage	V_{in}	$\text{AGND} - 0.7$	$\text{VA} + 0.7$	V
Storage temperature	T_{stg}	-65	150	$^{\circ}\text{C}$

WARNING: Operation at or beyond these limits can result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5.2 Recommended Operating Conditions

($\text{GND} = \text{GNDIO} = \text{GNDA} = 0\text{V}$; all voltages with respect to 0V)

Parameter	Symbol	Min	Typ	Max	Unit
DC power supplies:					
Core supply	V_{DD}	1.71	1.8	1.89	V
Analog supply	V_{DDA}	3.13	3.3	3.46	V
I/O supply	V_{DDIO}	3.13	3.3	3.46	V
$ V_{\text{DDA}} - V_{\text{DDIO}} $			0		V
Ambient operating temperature	T_{A}				$^{\circ}\text{C}$
Commercial—CQZ (147 MHz)		0	—	+70	
Automotive—DQZ (131 MHz)		-40		+85	
Automotive—DQZ (113 MHz)		-40		+105	

Note: It is recommended that the 3.3 V IO supply come up ahead of or simultaneously with the 1.8 V core supply.

5.3 Digital DC Characteristics

(Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.0	—	—	V
Low-level input voltage, except XTI	V_{IL}	—	—	0.8	V
Low-level input voltage, XTI	V_{ILKXTI}	—	—	0.6	V
Input Hysteresis	V_{hys}	—	0.4	—	V
High-level output voltage ($I_{\text{O}} = -2\text{mA}$), except XTO	V_{OH}	$V_{\text{DDIO}} \cdot 0.9$	—	—	V
Low-level output voltage ($I_{\text{O}} = 2\text{mA}$), except XTO	V_{OL}	—	—	$V_{\text{DDIO}} \cdot 0.1$	V
Input leakage XTI	I_{LXTI}	—	—	5	μA
Input leakage current (all digital pins with internal pull-up resistors enabled)	I_{LEAK}	—	—	70	μA

5.4 Power Supply Characteristics

Note: Measurements performed under operating conditions

Parameter	Min	Typ	Max	Unit
Operational Power Supply Current:				
VDD: Core and I/O operating ¹	—	325	—	mA
VDDA: PLL operating current	—	16	—	mA
VDDA: DAC operating current (all 8 channels enabled)	—	56	—	mA
VDDA: ADC operating current (all 4 channels enabled)	—	34	—	mA
VDDIO: With most ports operating	—	27	—	mA
Total Operational Power Dissipation:		1025		mW
Standby Power Supply Current:				
VDD: Core and I/O not clocked	—	410	—	μA
VDDA: PLLs halted	—	26	—	μA
VDDA: DAC disabled	—	40	—	μA
VDDA: ADC disabled	—	24	—	μA
VDDIO: All connected I/O pins 3-stated by other ICs in system	—	215	—	μA
Total Standby Power Dissipation:		1745		μW

1. Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (100-pin LQFP with Exposed Pad)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C/Watt
Two-layer Board ¹		—	34	—	
Four-layer Board ²		—	18	—	
Thermal Resistance (Junction to Top of Package)	ψ_{jt}				°C/Watt
Two-layer Board ¹		—	0.54	—	
Four-layer Board ²		—	.28	—	

- To calculate the die temperature for a given power dissipation:

$$T_j = \text{Ambient temperature} + [(\text{Power Dissipation in Watts}) * \theta_{ja}]$$

- To calculate the case temperature for a given power dissipation:

$$T_c = T_j - [(\text{Power Dissipation in Watts}) * \psi_{jt}]$$

Note: Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20% of the top and bottom layers.

Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20% of the top and bottom layers and 0.5-oz. copper covering 90% of the internal power plane and ground plane layers.

5.6 Digital Switching Characteristics—RESET

Parameter	Symbol	Min	Max	Unit
RESET minimum pulse width low ¹	T_{rstl}	1	—	μs
All bidirectional pins high-Z after RESET low	T_{rst2z}	—	200	ns
Configuration pins setup before RESET high	T_{rstsu}	50	—	ns
Configuration pins hold after RESET high	T_{rsthd}	20	—	ns

1. The rising edge of $\overline{\text{RESET}}$ must not occur before the power supplies are stable at the recommended operating values as described in Section 5.2. In addition, for the configuration pins to be read correctly, the RESET T_{rstl} requirement must be met.

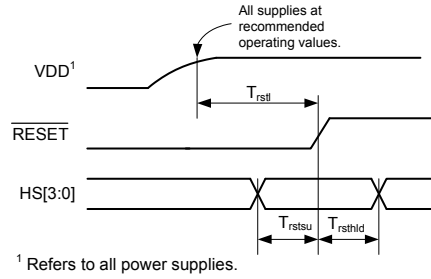


Figure 5-1. RESET Timing at Power-on

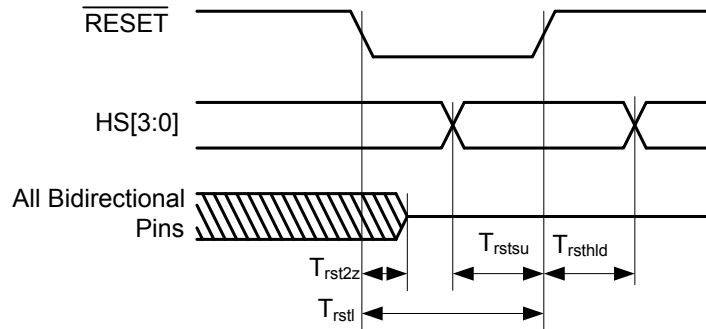


Figure 5-2. RESET Timing after Power is Stable

5.7 Digital Switching Characteristics–XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency ¹	F_{xtal}	12.288	24.576	MHz
XTI period	T_{clki}	41	81	ns
XTI high time	T_{clkih}	13.3	—	ns
XTI low time	T_{clkil}	13.3	—	ns
External Crystal Load Capacitance (parallel resonant) ²	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR	—	50	Ω

1. Part characterized with the following crystal frequency values: 12.288 and 24.576 MHz.

2. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals that require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

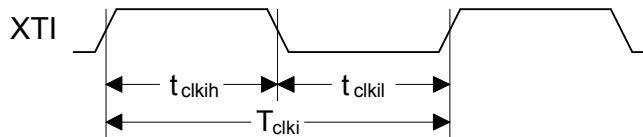


Figure 5-3. XTI Timing

5.8 Digital Switching Characteristics—Internal Clock

Parameter	Symbol	Min (2-layer Boards)	Min (4-layer Boards)	Max (2-layer Boards)	Max (4-layer Boards)	Unit
Internal DSP_CLK frequency ¹	F_{dclk}	(See Footnote 2)				MHz
CS47048-CQZ			F_{xtal}	147	147	
CS47048-DQZ			F_{xtal}	131	147	
CS47028-CQZ			F_{xtal}	147	147	
CS47028-DQZ			F_{xtal}	131	147	
CS47024-CQZ			F_{xtal}	147	147	
CS47024-DQZ			F_{xtal}	131	147	
Internal DSP_CLK period ¹	DCLKP					ns
CS47048-CQZ		6.8	6.8	$1/F_{\text{xtal}}$		
CS47048-DQZ		7.6	6.8	$1/F_{\text{xtal}}$		
CS47028-CQZ		6.8	6.8	$1/F_{\text{xtal}}$		
CS47028-DQZ		7.6	6.8	$1/F_{\text{xtal}}$		
CS47024-CQZ		6.8	6.8	$1/F_{\text{xtal}}$		
CS47024-DQZ		7.6	6.8	$1/F_{\text{xtal}}$		

1. After initial power-on reset, $F_{\text{dclk}} = F_{\text{xtal}}$. After initial kick-start commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

2. See Section 5.7. for all references to F_{xtal} .

5.9 Digital Switching Characteristics—Serial Control Port—SPI Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
SCP_CLK frequency ¹	f_{spisck}	—	—	25	MHz
SCP_CS falling to SCP_CLK rising	t_{spicss}	24	—	—	ns
SCP_CLK low time	t_{spickl}	20	—	—	ns
SCP_CLK high time	t_{spickh}	20	—	—	ns
Setup time SCP_MOSI input	t_{spidsu}	5	—	—	ns
Hold time SCP_MOSI input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MISO output valid	t_{spidov}	—	—	11	ns
SCP_CLK falling to SCP_IRQ rising	t_{spiirqh}	—	—	27	ns
SCP_CS rising to SCP_IRQ falling	t_{spiirql}	0	—	—	ns
SCP_CLK low to SCP_CS rising	t_{spicsh}	24	—	—	ns
SCP_CS rising to SCP_MISO output high-Z	t_{spicsdz}	—	20	—	ns
SCP_CLK rising to SCP_BSY falling	t_{spicbsyl}	—	$3 \cdot \text{DCLKP} + 20$	—	ns

1. f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port can be limited by the firmware application. Flow control using the SCP_BSY pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is $F_{\text{xtal}}/3$.

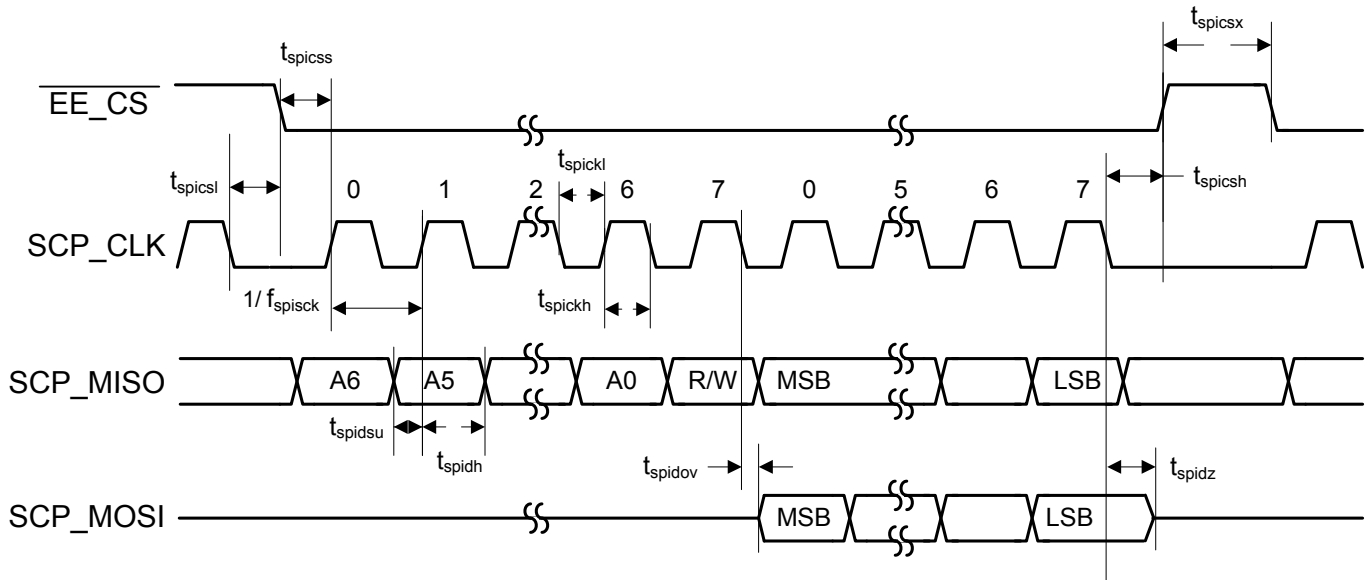


Figure 5-5. Serial Control Port–SPI Master Mode Timing

5.11 Digital Switching Characteristics–Serial Control Port I2C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency ¹	f_{icck}	—	—	400	kHz
SCP_CLK rise time	t_{icr}	—	—	150	ns
SCP_CLK fall time	t_{icf}	—	—	150	ns
SCP_CLK low time	t_{icckl}	1.25	—	—	μ s
SCP_CLK high time	t_{icckh}	1.25	—	—	μ s
SCP_CLK rising to SCP_SDA rising or falling for START or STOP condition	$t_{icckcmd}$	1.25	—	—	μ s
START condition to SCP_CLK falling	t_{icstsc}	1.25	—	—	μ s
SCP_CLK falling to STOP condition	t_{icstp}	2.5	—	—	μ s
Bus free time between STOP and START conditions	t_{icbft}	3	—	—	μ s
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iccsu}	110	—	—	ns
Hold time SCP_SDA input after SCP_CLK falling	t_{icich}	100	—	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iccdov}	—	—	18	ns
SCP_CLK falling to SCP_IRQ rising	t_{icirqh}	—	—	$3 \cdot DCLKP + 40$	ns
NAK condition to SCP_IRQ low	t_{icirql}	—	$3 \cdot DCLKP + 20$	—	ns
SCP_CLK rising to SCP_BSY low	t_{icbsyl}	—	$3 \cdot DCLKP + 20$	—	ns

1. f_{icck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port can be limited by the firmware application. Flow control using the $\overline{SCP_BSY}$ pin should be implemented to prevent overflow of the input data buffer.

I2C Slave Address = 0x82

5.13 Digital Switching Characteristics–Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	20	—	ns
DAI_SCLK duty cycle	—	45	55	%
Setup time DAI_DATAn	t_{daidsu}	8	—	ns
Hold time DAI_DATAn	t_{daidh}	5	—	ns

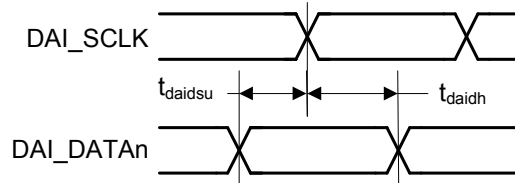


Figure 5-8. Digital Audio Input (DAI) Port Timing Diagram

5.14 Digital Switching Characteristics–Digital Audio Output Port

Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	20	—	ns
DAO_MCLK duty cycle	—	45	55	%
DAO_SCLK period for Master or Slave mode ¹	$T_{daosclk}$	20	—	ns
DAO_SCLK duty cycle for Master or Slave mode ¹	—	40	60	%
Master Mode (Output A1 Mode)^{1,2}				
DAO_SCLK delay from DAO_MCLK rising edge, DAO MCLK as an input	$t_{daomsck}$	—	19	ns
DAO_LRCLK to DAO_SCLK inactive edge ³ . See Fig. 5-9.	$t_{daomlrts}$	—	8	ns
DAO_SCLK inactive edge ³ to DAO_LRCLK. See Fig. 5-10.	$t_{daomstlr}$	—	8	ns
DAO_DATA[3:0] delay from DAO_SCLK inactive edge ³	t_{daomdy}	—	8	ns
Slave Mode (Output A0 Mode)⁴				
DAO_SCLK active edge to DAO_LRCLK transition. See Fig. 5-11.	$t_{daosstlr}$	10	—	ns
DAO_LRCLK transition to DAO_SCLK active edge. See Fig. 5-12.	$t_{daoslrts}$	10	—	ns
DAO_Dx delay from DAO_SCLK inactive edge	t_{daosdv}	—	11	ns

1. Master mode timing specifications are characterized, not production tested.

2. Master mode is defined as the CS47048 driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.

3. The DAO_LRCLK transition can occur on either side of the edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.

4. Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.

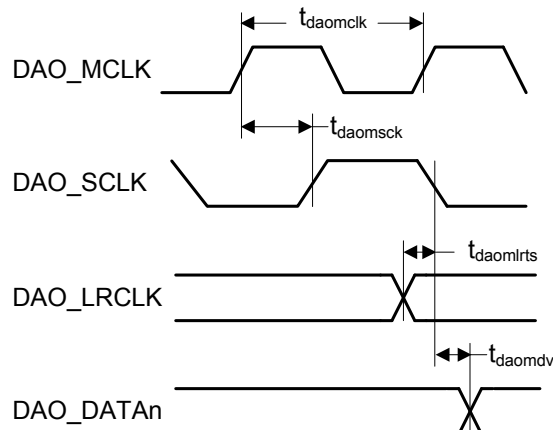


Figure 5-9. DAO_LRCLK Transition before DAO_SCLK Inactive Edge

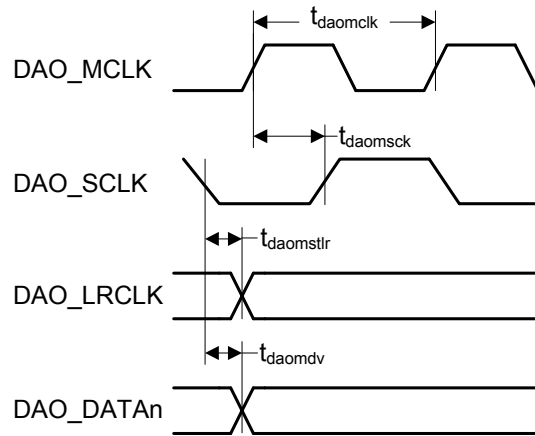


Figure 5-10. DAO_LRCLK Transition after DAO_SCLK Inactive Edge

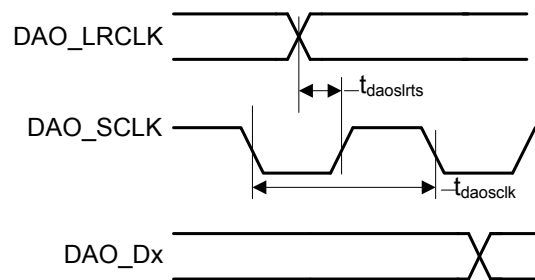


Figure 5-11. DAO_LRCLK Transition before DAO_SCLK Inactive Edge

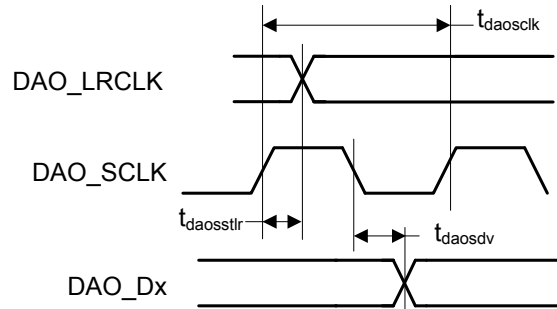


Figure 5-12. DAO_LRCLK Transition after DAO_SCLK Inactive Edge

5.16.2 Analog Input Characteristics (Automotive)

Test Conditions (unless otherwise specified): $T_A = -40$ – 85°C ; $V_{DD} = 1.8\text{V} \pm 5\%$, $V_{DDA} (V_A) = 3.3\text{V} \pm 5\%$; kHz sine wave driven through the passive input filter ($R_i = 10\text{ k}\Omega$) in Fig. 5-13 or Fig. 5-14; DSP running test application; Measurement Bandwidth is 10 Hz–20 kHz.

	Differential			Single-ended			
Parameter	Min	Typ	Max	Min	Typ	Max	Unit
Fs = 96 kHz							
Dynamic Range ^{1,6,7}							
A-weighted	97	105	—	94	102	—	dB
Unweighted	94	102	—	91	99	—	dB
40 kHz bandwidth unweighted	—	99	—	—	96	—	dB
Total Harmonic Distortion + Noise ^{6,7}							
–1 dB	—	–98	–90	—	–95	–87	dB
–20 dB	—	–82	—	—	–79	—	dB
–60 dB	—	–42	—	—	–39	—	dB
40 kHz bandwidth –1 dB	—	–90	—	—	–90	—	dB
AIN_1A/B Interchannel Isolation ¹⁰	—	95	—	—	95	—	dB
AID_[2.6]A/B MUX Interchannel Isolation	—	95	—	—	95	—	dB
DC Accuracy							
Interchannel Gain Mismatch	—	0.1	—	—	0.1	—	dB
Gain Drift	—	±120	—	—	±120	—	ppm/°C
Analog Input							
Full-scale Input Voltage ^{2,3}	3.3	3.7•VA	3.9	1.65	1.85•VA	1.95	V _{PP}
Differential Input Impedance ⁴	—	400	—	—	—	—	Ω
Single-ended Input Impedance ⁵	—	—	—	—	200	—	Ω
Common Mode Rejection Ratio (CMRR) ⁸	—	60	—	—	—	—	dB
Parasitic Load Capacitance (C _L) ⁹	—	—	20	—	—	20	pF

1. dB units referred to the typical full-scale voltage.
2. These full-scale values were measured with $R_i = 10\text{ k}\Omega$ for both the single-ended and differential mode input circuits.
3. The full-scale voltage can be changed by scaling R_i .
 Differential Full-Scale (V_{pp}) = $3.7 \cdot V_{DDA} \cdot (R_i + 200) / (10\text{ k} + 200)$
 Single-Ended Full-Scale (V_{pp}) = $1.85 \cdot V_{DDA} \cdot (R_i + 200) / (10\text{ k} + 200)$
4. Measured between AIN_xx+ and AN_xx–.
5. Measured between AIN_xx+ and AGND.
6. Decreasing full-scale voltage by reducing R_i causes the noise floor to increase.
7. Common mode input current should be kept to less than $\pm 160\text{ uA}$ to avoid performance degradation: $|I_{ip} + I_{in}|/2 < 160\text{ uA}$. This corresponds to $\pm 1.6\text{ V}$ for $R_i = 10\text{ k}\Omega$ in the differential case.
8. This number was measured using perfectly matched external resistors (R_i). Mismatch in the external resistors typically reduces CMRR by $20 \log(|\Delta R_i|/R_i + 0.001)$.
9. C_L represents the parasitic load capacitance between R_i on the input circuit and the input pin of the CS47048 package.
10. This measurement is not applicable to the CS47028 and CS47024 devices.

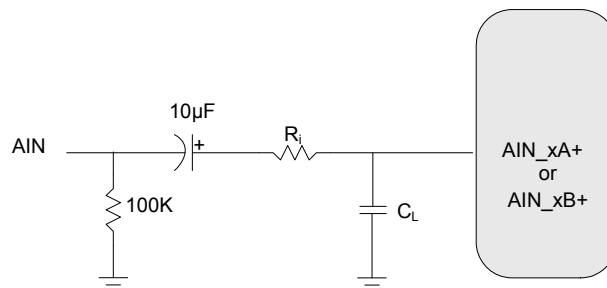


Figure 5-13. ADC Single-ended Input Test Circuit

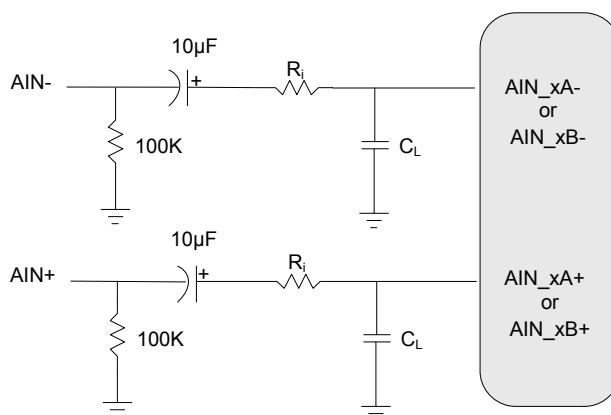


Figure 5-14. ADC Differential Input Test Circuit

5.16.3 ADC Digital Filter Characteristics

Parameter ^{1,2}	Min	Typ	Max	Unit
Fs = 96 kHz				
Passband (Frequency Response) to -0.1 dB corner	0	—	0.4896	Fs
Passband Ripple	—	—	0.08	dB
Stopband	0.5688	—	—	Fs
Stopband Attenuation	70	—	—	dB
Total Group Delay	—	12/Fs	—	s
High-pass Filter Characteristics				
Frequency Response:				
-3.0 dB	—	1	—	Hz
-0.13 dB	—	20	—	Hz
Phase Deviation @ 20 Hz	—	10	—	Deg
Passband Ripple	—	—	0	dB
Filter Settling Time	—	10 ⁵ /Fs	0	s

1. Filter response is guaranteed by design.

2. Response is clock-dependent and scales with Fs.

5.17 DAC Characteristics

5.17.1 Analog Output Characteristics (Commercial)

Test Conditions (unless otherwise specified): TA = 0–+70°C; VDD = 1.8V±5%, VDDA(VA) = 3.3V±5%; 1 kHz sine wave driven through a filter shown in Fig. 5-15 or Fig. 5-16; DSP running test application; Measurement Bandwidth is 20 Hz–20 kHz.

	Differential			Single-ended			
Parameter	Min	Typ	Max	Min	Typ	Max	Unit
Fs = 96 kHz							
Dynamic Range							
A-weighted	102	108	—	99	105	—	dB
Unweighted	99	105	—	96	102	—	dB
Total Harmonic Distortion + Noise							
0 dB	—	−98	−90	—	−95	−87	dB
−20 dB	—	−88	—	—	−85	—	dB
−60 dB	—	−48	—	—	−45	—	dB
Interchannel Isolation (1 kHz)	—	95	—	—	95	—	dB

8 Device Pinout Diagrams

8.1 CS47048, 100-pin LQFP Pinout Diagram

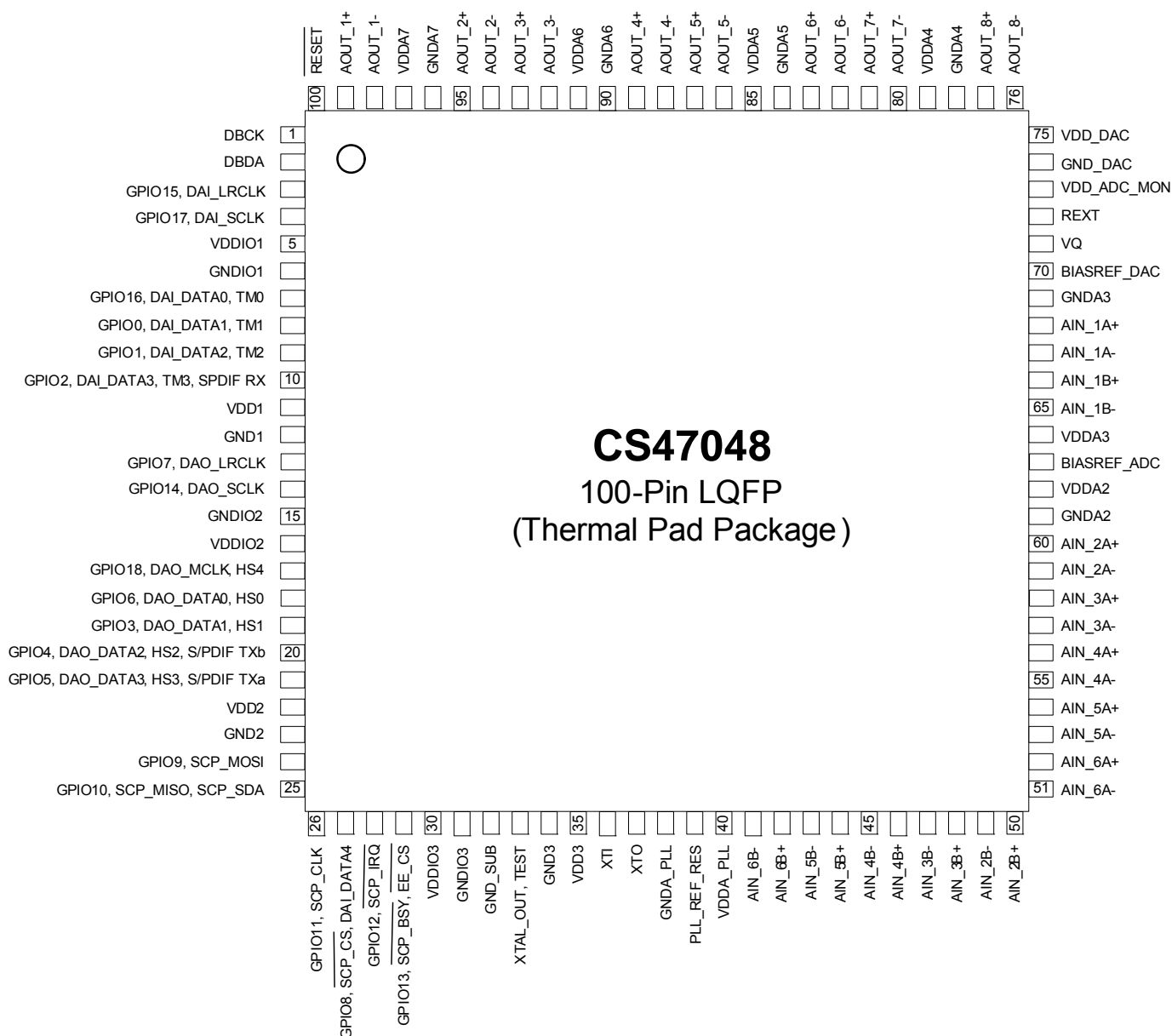


Figure 8-1. CS47048 Pinout Diagram

8.2 CS47028, 100-pin LQFP Pinout Diagram

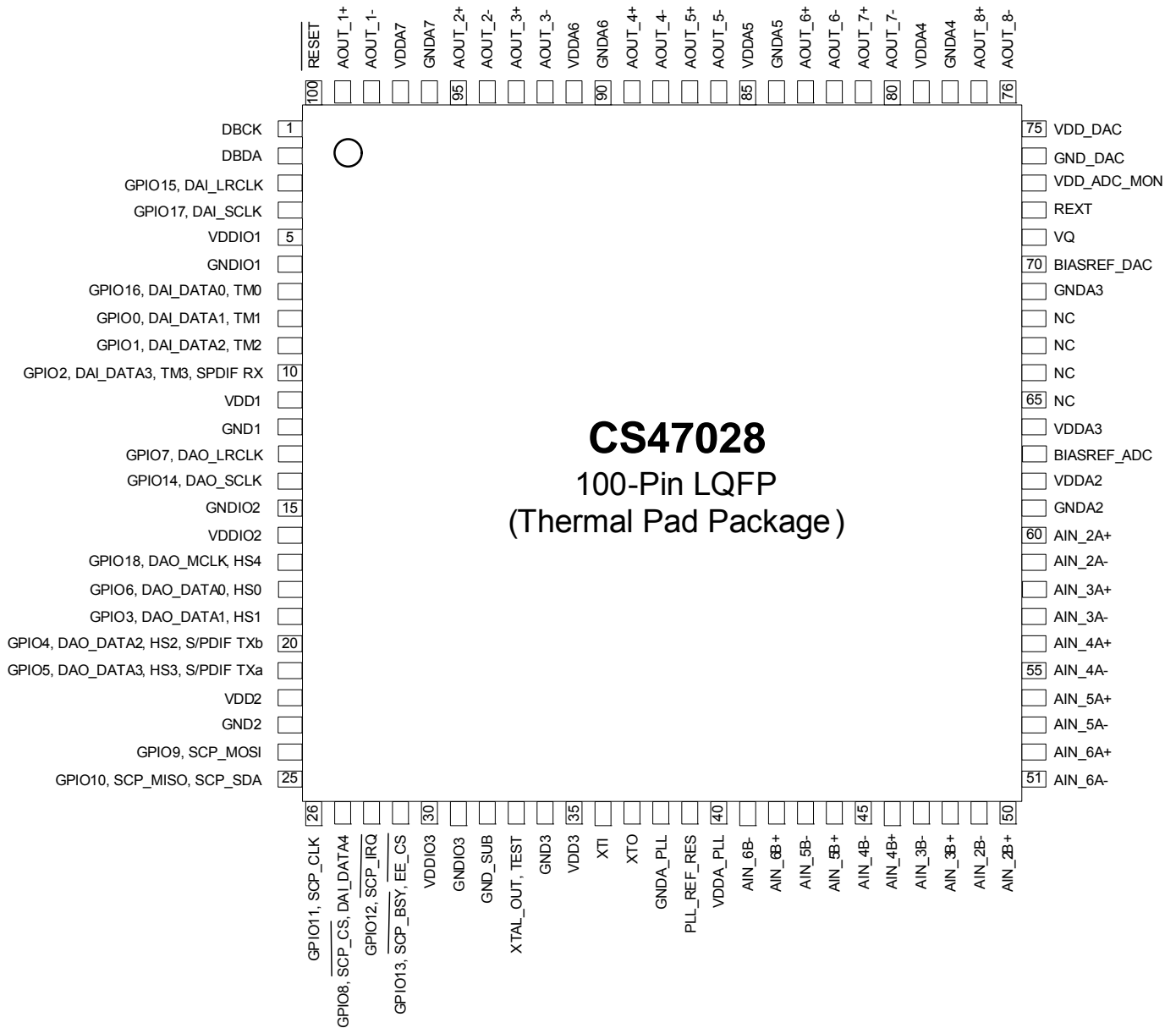


Figure 8-2. CS47028 Pinout Diagram

8.3 CS47024, 100-pin LQFP Pinout Diagram

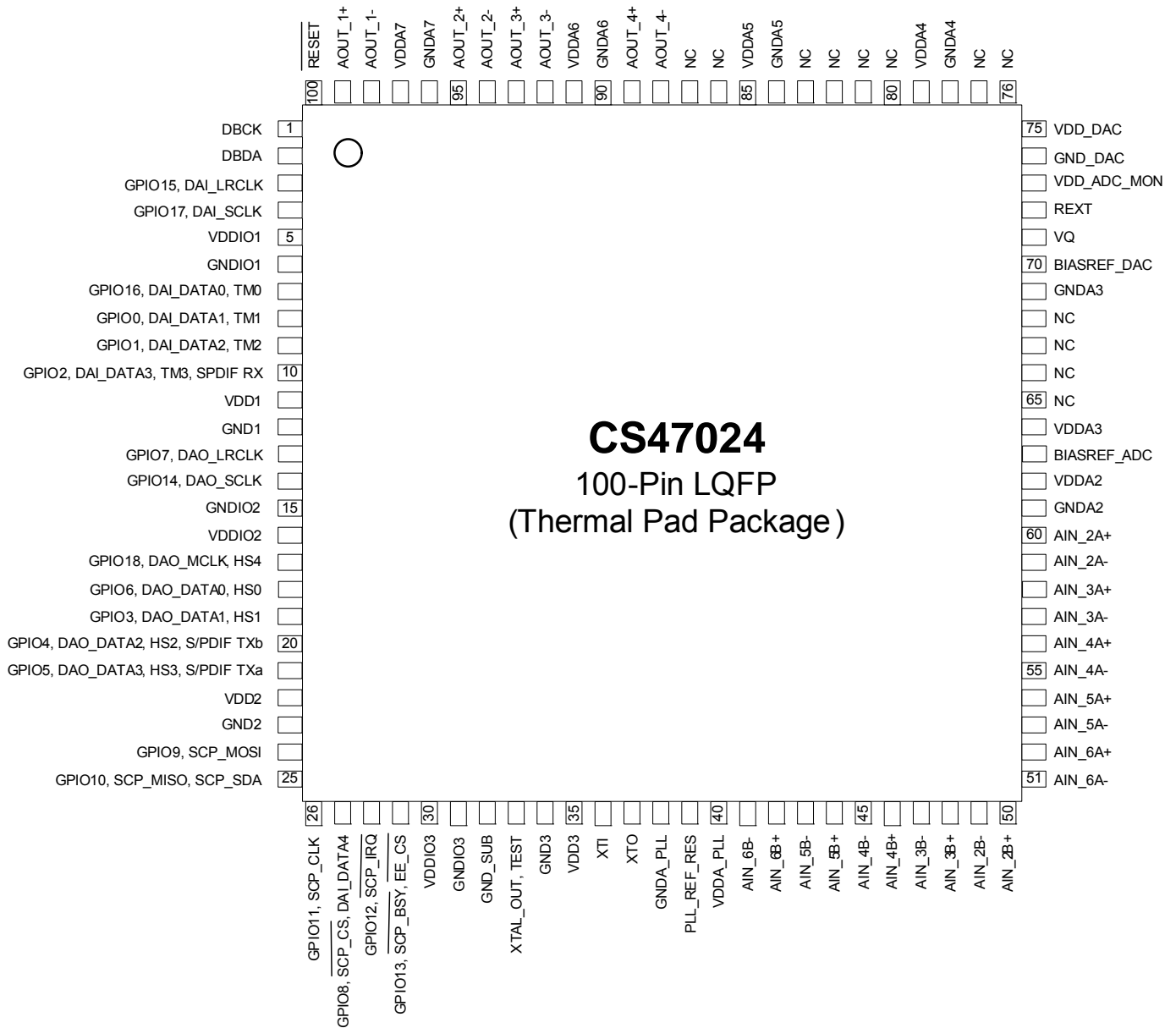


Figure 8-3. CS47024 Pinout Diagram

10 Parameter Definitions

10.1 Dynamic Range

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

10.2 Total Harmonic Distortion + Noise

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth (typically 10 Hz–20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

10.3 Frequency Response

A measure of the amplitude response variation from 10 Hz–20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

10.4 Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

10.5 Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

10.6 Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

10.7 Gain Drift

The change in gain value with temperature. Units in ppm/°C.

11 Revision History

Revision	Date	Changes
PP1	August, 2009	Updated Characterization data in Section 5.4, Section 5.7, Section 5.9, Section 5.11, Section 5.12, Section 5.16.1, Section 5.16.2, Section 5.16.3, Section 5.17.1, and Section 5.17.2. Modified Footnote 3 in both Section 5.16.1 and Section 5.16.2. Added Footnote 5 to Section 5.14. Updated Section 2.1. Modified Section 4.3.6 and Section 4.3.8. Modified references to TDM in various sections of the data sheet.
PP2	January, 2010	Updated TDM Feature description on page 1. Modified note at the bottom of the feature list on page 1. Updated table in Section 5.8, specifying performance data for 2- and 4-layer boards. Updated Table 3-1 and Table 3-2 Updated block diagrams in Fig. 4-1, Fig. 4-2, and Fig. 4-3.
PP3	June, 2010	Table 3-1: Straddled all three columns in the "Supports Different Fs Sample Rates" row to indicate that CS47024 devices have the same features as the CS47048 and CS47028. Added "The CS47024 has the 8-channel SRC block" to Section 4.3.7. Added text in the following places to indicate that the CS47024 implements the S/PDIF Rx functionality: <ul style="list-style-type: none"> • Removed dagger from the S/PDIF Rx bullet on p. 1. • Updated bullet in "Configurable Serial Audio Inputs/Outputs" row in Table 2 Integrated 192 kHz S/PDIF Rx, 2 Integrated 192 kHz S/PDIF Tx. • Changed entry in "S/PDIF In (Stereo Pairs)" column in Table 3-2. • Updated I2S block in Table 3-2. • Removed text "On the CS47048 and CS47028..." from Section 4.3.4. • Removed "(Not available on CS47024)" from the heading to Section 5.15. • Described additional support for TDM 8-channel output mode on CS47024. • Removed dagger from the TDM I/O bullet on p. 1. • Straddled "Configurable Serial Audio Inputs/Outputs" row in Table 3-1. • Changed cell in "TDM Out" column in Table 3-2. • Removed text "On the CS47048 and CS47028..." from Section 4.3.5.
PP4	February, 2011	Added "Decoder" information to Section 3. Changed the name of the core to "Cirrus Logic 32-bit core".
PP5	February, 2011	Added "SPDIF RX" to Fig. 5-17.
PP6	June, 2011	In Section 4.3.1 and Section 4.3.7, removed mention of 192 kHz sampling frequency. Updated temperature operating conditions in Section 5.2. Updated pin 33 to XTAL_OUT, TEST in Fig. 8-1, Fig. 8-2, and Fig. 8-3.
PP7	April, 2012	Corrected peak reflow temperature in Table 7-1.
PP8	June, 2012	Added number of bits to Integrated DAC and ADC Functionality on the cover page.
PP9	July, 2012	Updated frequencies in Section 5.2. Added extended automotive grade information to Section 6 and Section 7.