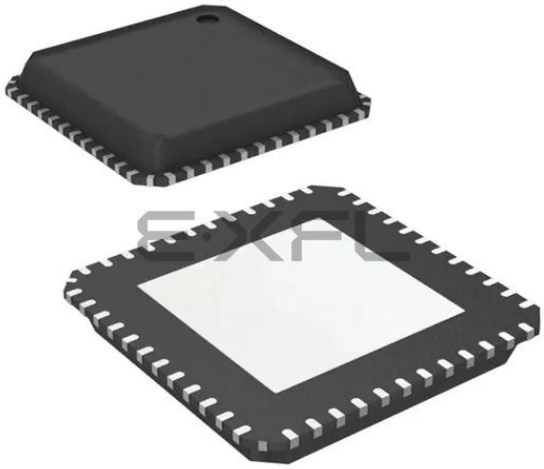
Infineon Technologies - XC2723X20F66VAAKXUMA1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-54
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2723x20f66vaakxuma1

As this document refers to all of these derivatives, some descriptions may not apply to a specific product, in particular to the special device types.

For simplicity the term **XC2723X** is used for all derivatives throughout this document.

1.2 Special Device Types

Special device types are only available for high-volume applications on request.

Table 2 Synopsis of XC2723X **Special Device Types**

Derivative[1]	Flash Memory[2]	PSRAM DSRAM[3]	Capt./Comp. Modules	ADC[4] Chan.	Interfaces[4]
None					

1) x is a placeholder for available speed grade in MHz. Can be 66 or 80.
2) Specific information about the on-chip Flash memory in **Table 3**.
3) All derivatives additionally provide 2 Kbytes DPRAM.
4) Specific information about the available channels in **Table 5**.

Key to Pin Definitions

- **Ctrl.**: The output signal for a port pin is selected by bit field PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bit field PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.
  Output signal OH is controlled by hardware.
- **Type**: Indicates the pad type and its power supply domain (B, M).
  - St: Standard pad
  - Sp: Special pad e.g. XTALx
  - DA: Digital IO and analog input
  - In: Input only pad
  - PS: Power supply pad

Table 6 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
1	$\overline{\text{TESTM}}$	I	In/B	**Testmode Enable** Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
2	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC2723X's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
3	P6.3	O0 / I	St/B	**Bit 3 of Port 6, General Purpose Input/Output**
	CCU63_COUT62	O1	St/B	**CCU63 Channel 2 Output**
	T3OUT	O2	St/B	**GPT12E Timer T3 Toggle Latch Output**
	U1C1_SELO0	O3	St/B	**USIC1 Channel 1 Select/Control 0 Output**
	U1C1_DX2D	I	St/B	**USIC1 Channel 1 Shift Control Input**
	ADC0_REQTRyF	I	St/B	**External Request Trigger Input for ADC0/1**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
47	XTAL1	I	Sp/M	**Crystal Oscillator Amplifier Input** To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDIM}.
	ESR2_9	I	St/B	**ESR2 Trigger Input 9**
48	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XC2723X completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pullup device will hold this pin high when nothing is driving it.
8	V_{AREF}	-	PS/B	**Reference Voltage for A/D Converters ADC0**
9	V_{AGND}	-	PS/B	**Reference Ground for A/D Converters ADC0**
18, 43	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDIM} pins must be connected to each other.
7, 20, 41	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins.
6, 19, 42	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane.

Table 8 XC2723X **Memory Map** (cont'd)[1] (cont'd)

Address Area	Start Loc.	End Loc.	Area Size[2]	Notes
ESFR area	$00'F000_H$	$00'F1FF_H$	0.5 Kbytes	
XSFR area	$00'E000_H$	$00'EFFF_H$	4 Kbytes	
Data SRAM (DSRAM)	$00'C800_H$	$00'DFFF_H$	6 Kbytes	
Reserved for DSRAM	$00'8000_H$	$00'C7FF_H$	18 Kbytes	
External memory area	$00'0000_H$	$00'7FFF_H$	32 Kbytes	

1) Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.

2) The areas marked with "<" are slightly smaller than indicated, see column "Notes".

3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

4) Several pipeline optimizations are not active within the external IO area.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

4 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

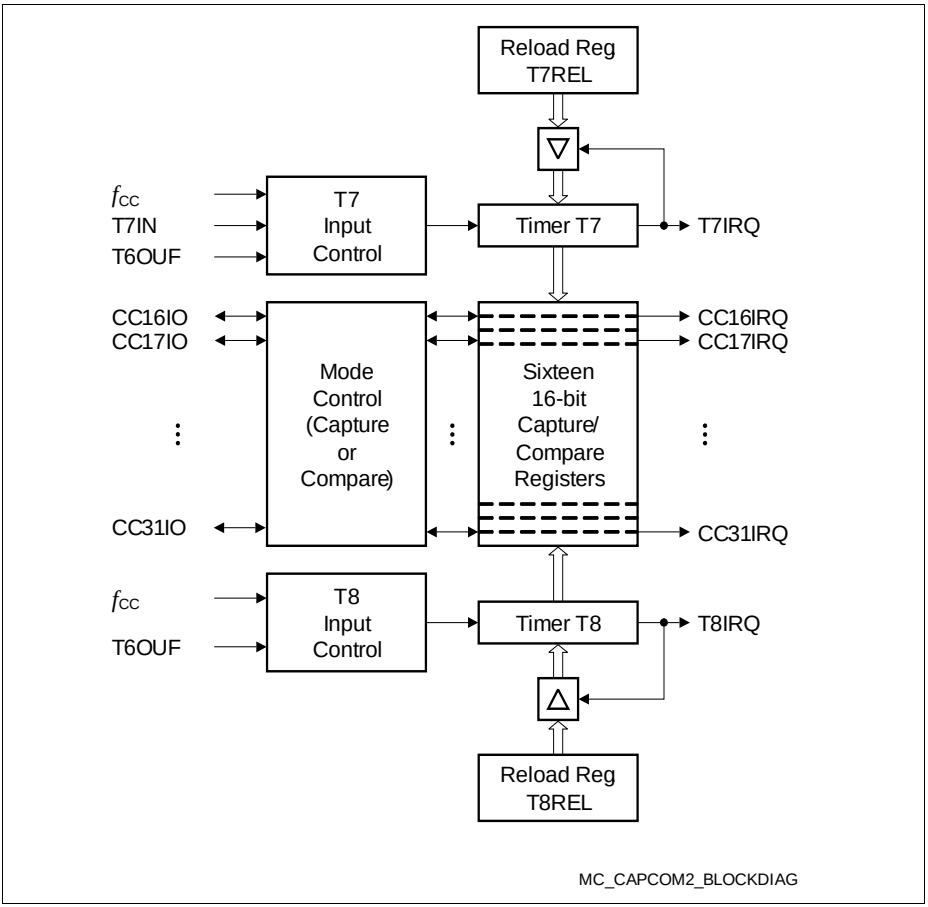


Figure 5 CAPCOM Unit Block Diagram

3.11 A/D Converters

For analog signal measurement, a 12-bit A/D converters (ADC0) with 10 multiplexed input channels and a sample and hold circuit have been integrated on-chip. Conversions use the successive approximation method. The sample time (to charge the capacitors) and the conversion time are programmable so that they can be adjusted to the external circuit. The A/D converters can also operate in 8-bit and 10-bit conversion mode, further reducing the conversion time.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to meet the application requirements.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically. For applications that require fewer analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XC2723X support two types of request sources which can be triggered by several internal and external events.

- Parallel requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing that sequence. All requests are arbitrated according to the priority level assigned to them.

Data reduction features reduce the number of required CPU access operations allowing the precise evaluation of analog inputs (high conversion rate) even at a low CPU speed. Result data can be reduced by limit checking or accumulation of results. Two cascadable filters build the hardware to generate a configurable moving average.

The Peripheral Event Controller (PEC) can be used to control the A/D converters or to automatically store conversion results to a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Each A/D converter contains eight result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent the loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise, those pins used for analog input can be disconnected from the digital input stages. This can be selected for each pin separately with the Port x Digital Input Disable registers.

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

Broken wire detection for each channel and a multiplexer test mode provide information to verify the proper operation of the analog signal sources (e.g. a sensor system).

Table 11 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XC2723X, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

8) Value is controlled by on-chip regulator.

4.2 Voltage Range definitions

The XC2723X timing depends on the supply voltage. If such a dependency exists the timing values are given for 2 voltage areas commonly used. The voltage areas are defined in the following tables.

Table 14 Upper Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	4.5	5.0	5.5	V	

Table 15 Lower Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0	3.3	4.5	V	

4.2.1 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XC2723X and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XC2723X provides signals with the specified characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the specified characteristics to the XC2723X.

Table 18 Switching Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT} CC	–	6 + 0.5 x f_{SYS} [1]	8 + 0.75 x f_{SYS} [1]	mA	power_mode= active ; voltage_range= both [2][3][4]
Power supply current in stopover mode, EVVRs on	I_{SSO} CC	–	0.7	2.0	mA	power_mode= stopover ; voltage_range= both

1) f_{SYS} in MHz

2) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched.

3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

4) The pad supply voltage only has a minor influence on this parameter.

Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XC2723X's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.
A small current is consumed because the drivers' input stages are switched.

Table 23 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time[1] t_S
000000_B	f_{SYS}	00_H	$t_{ADCI} \times 2$
000001_B	f_{SYS} / 2	01_H	$t_{ADCI} \times 3$
000010_B	f_{SYS} / 3	02_H	$t_{ADCI} \times 4$
:	f_{SYS} / (DIVA+1)	:	$t_{ADCI} \times$ (STC+2)
111110_B	f_{SYS} / 63	FE_H	$t_{ADCI} \times 256$
111111_B	f_{SYS} / 64	FF_H	$t_{ADCI} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions: f_{SYS} = 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03_H, STC = 00_H
Analog clock f_{ADCI} = f_{SYS} / 4 = 20 MHz, i.e. t_{ADCI} = 50 ns
Sample time t_S = $t_{ADCI} \times 2$ = 100 ns

Conversion 12-bit:

$t_{C12} = 16 \times t_{ADCI} + 2 \times t_{SYS} = 16 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.825\ \mu s$

Conversion 10-bit:

$t_{C10} = 12 \times t_{ADCI} + 2 \times t_{SYS} = 12 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.625\ \mu s$

Conversion 8-bit:

$t_{C8} = 10 \times t_{ADCI} + 2 \times t_{SYS} = 10 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.525\ \mu s$

Converter Timing Example B:

Assumptions: f_{SYS} = 66 MHz (i.e. t_{SYS} = 15.2 ns), DIVA = 03_H, STC = 00_H
Analog clock f_{ADCI} = f_{SYS} / 4 = 16.5 MHz, i.e. t_{ADCI} = 60.6 ns
Sample time t_S = $t_{ADCI} \times 2$ = 121.2 ns

Conversion 12-bit:

$t_{C12} = 16 \times t_{ADCI} + 2 \times t_{SYS} = 16 \times 60.6\text{ ns} + 2 \times 15.2\text{ ns} = 1.0\ \mu s$

Conversion 10-bit:

$t_{C10} = 12 \times t_{ADCI} + 2 \times t_{SYS} = 12 \times 60.6\text{ ns} + 2 \times 15.2\text{ ns} = 0.758\ \mu s$

Coding of bit fields LEVxV in SWD Configuration Registers

After power-on the supply watch dog is preconfigured to operate in the lower voltage range.

Table 25 Coding of bit fields LEVxV in Register SWDCON0

Code	Default Voltage Level	Notes[1)]
0000_B	-	out of valid operation range
0001_B	3.0 V	LEV1V: reset request
0010_B - 0101_B	3.1 V - 3.4 V	step width is 0.1 V
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B - 1110_B	4.6 V - 5.0 V	step width is 0.1 V
1111_B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Coding of bit fields LEVxV in PVC Configuration Registers

The core voltages are controlled internally to the nominal value of 1.5 V; a variation of ±10 % is allowed. These operation conditions limit the possible PVC monitoring values to the predefined reset values shown in **Table 26**.

Table 26 Coding of bit fields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes[1)]
000_B - 011_B	-	out of valid operation range
100_B	1.35 V	LEV1V: reset request
101_B	1.45 V	LEV2V: interrupt request[2)]
110_B - 111_B	-	out of valid operation range

1) The indicated default levels are selected automatically after a power reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.

Direct Drive

When direct drive operation is selected (SYSCON0.CLKSEL = 11_B), the system clock is derived directly from the input clock signal CLKIN1:

$f_{SYS} = f_{IN}$.

The frequency of f_{SYS} is the same as the frequency of f_{IN}. In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{IN}.

Selecting Bypass Operation from the XTAL1[1)] input and using a divider factor of 1 results in a similar configuration.

Prescaler Operation

When prescaler operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 1_B), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

$f_{SYS} = f_{OSC}$ / K1.

If a divider factor of 1 is selected, the frequency of f_{SYS} equals the frequency of f_{OSC}. In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{OSC} (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

$f_{SYS} = f_{OSC}$ / 1024.

4.7.2.1 Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 0_B), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{SYS} = f_{IN} \times$ **F**).
F is calculated from the input divider P (= PDIV+1), the multiplication factor N (= NDIV+1), and the output divider K2 (= K2DIV+1):
(**F** = N / (P $\times$ K2)).

The input clock can be derived either from an external source at XTAL1 or from the on-chip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of f_{SYS} so that it is locked to f_{IN}. The slight variation causes a jitter of f_{SYS} which in turn affects the duration of individual TCSs.

1) Voltages on XTAL1 must comply to the core supply voltage V_{DDIM}.

4.7.4 Pad Properties

The output pad drivers of the XC2723X can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage V_{DDP}. Therefore the following tables list the pad parameters for the upper voltage range and the lower voltage range, respectively.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 30 is valid under the following conditions: $V_{DDP} \leq$ 5.5 V; V_{DDP}typ. 5 V; $V_{DDP} \geq$ 4.5 V

Table 30 Standard Pad Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value)[1)]	I_{Omax} CC	–	–	3.0	mA	Driver_Strength = Medium
		–	–	5.0	mA	Driver_Strength = Strong
		–	–	0.5	mA	Driver_Strength = Weak
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	1.0	mA	Driver_Strength = Medium
		–	–	1.6	mA	Driver_Strength = Strong
		–	–	0.25	mA	Driver_Strength = Weak

Table 30 Standard Pad Parameters for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	38 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	1 + 0.45 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Soft
		–	–	16 + 0.45 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	200 + 2.5 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 25 mA.

Table 31 Standard Pad Parameters for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value)[1)]	I_{Omax} CC	–	–	1.8	mA	Driver_Strength = Medium
		–	–	3.0	mA	Driver_Strength = Strong
		–	–	0.3	mA	Driver_Strength = Weak

Table 31 Standard Pad Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	0.8	mA	Driver_Strength = Medium
		–	–	1.0	mA	Driver_Strength = Strong
		–	–	0.15	mA	Driver_Strength = Weak
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	73 + 0.85 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	6 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Soft
		–	–	33 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	385 + 3.25 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and ΣI_{OH}) must remain below 25 mA.

4.7.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 32 is valid under the following conditions: C_L= 20 pF; SSC= master ; voltage_range= upper

Table 32 USIC SSC Master Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{SYS} - 8[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{SYS} - 6[1)]	–	–	ns	
Data output DOUT valid time	t_3 CC	-6	–	9	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-4	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 34 USIC SSC Slave Mode Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data input DX0 hold time from clock input DX1 receive edge[1)]	t_{13} SR	5	–	–	ns	
Data output DOUT valid time	t_{14} CC	7	–	33	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Table 35 is valid under the following conditions: C_L= 20 pF; *SSC*= slave ; voltage_range= lower

Table 35 USIC SSC Slave Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10} SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11} SR	7	–	–	ns	
Receive data input setup time to shift clock receive edge[1)]	t_{12} SR	7	–	–	ns	
Data input DX0 hold time from clock input DX1 receive edge[1)]	t_{13} SR	5	–	–	ns	
Data output DOUT valid time	t_{14} CC	8	–	41	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

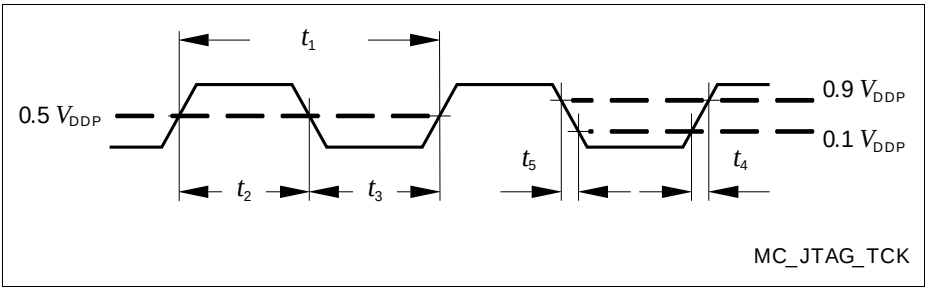


Figure 25 Test Clock Timing (TCK)

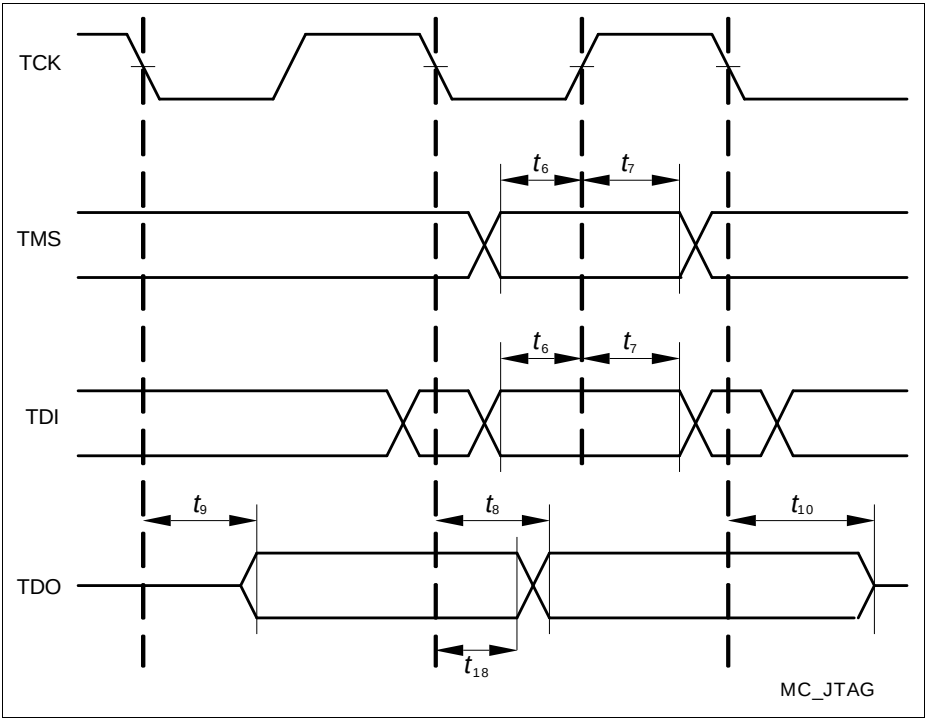


Figure 26 JTAG Timing

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG