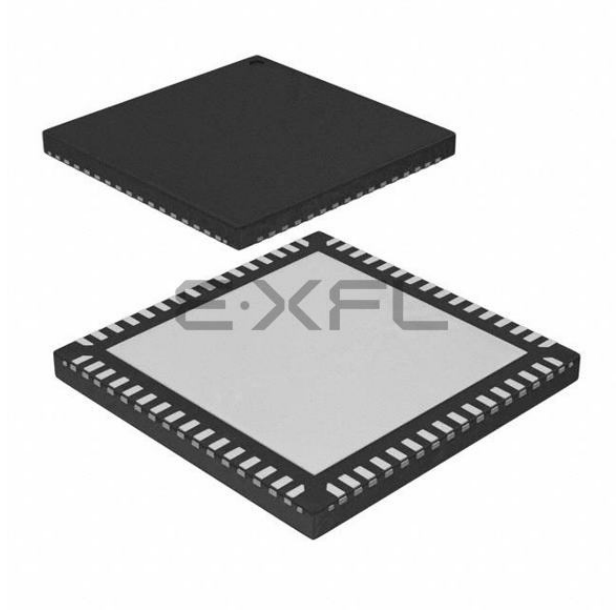


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | AVR |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | SPI, UART/USART, USI |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 54 |
| Program Memory Size | 16KB (8K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atmega165v-8mi |

tors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs.

Port F also serves the functions of the JTAG interface.

**Port G (PG4..PG0)**

Port G is a 5-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port G also serves the functions of various special features of the ATmega165 as listed on page 66.

**$\overline{\text{RESET}}$**

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 16 on page 38. Shorter pulses are not guaranteed to generate a reset.

**XTAL1**

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

**XTAL2**

Output from the inverting Oscillator amplifier.

**AVCC**

AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to $V_{CC}$, even if the ADC is not used. If the ADC is used, it should be connected to $V_{CC}$ through a low-pass filter.

**AREF**

This is the analog reference pin for the A/D Converter.

## About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

These code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".

## Instruction Execution Timing

This section describes the general access timing concepts for instruction execution. The AVR CPU is driven by the CPU clock $clk_{CPU}$, directly generated from the selected clock source for the chip. No internal clock division is used.

Figure 6 shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access Register File concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks, and functions per power-unit.

**Figure 6.** The Parallel Instruction Fetches and Instruction Executions

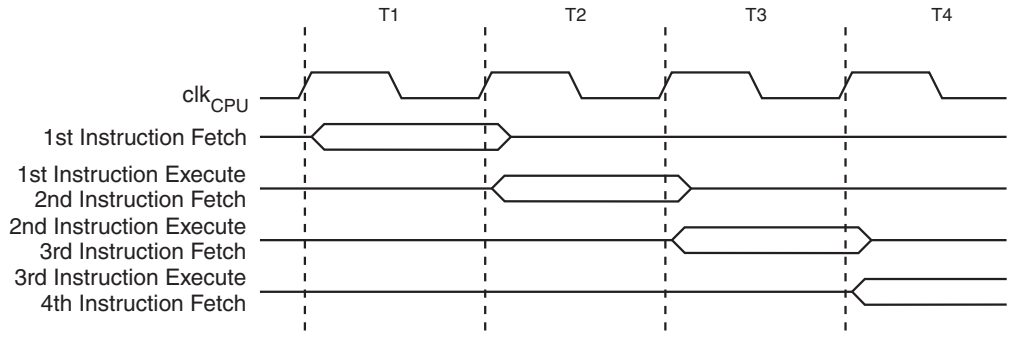
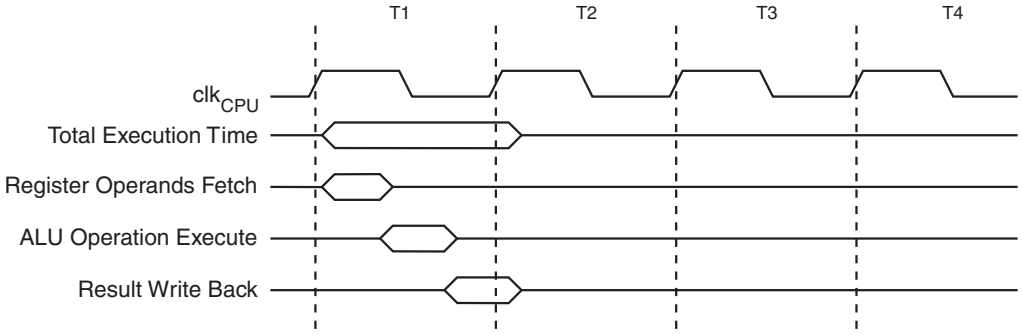



Figure 7 shows the internal timing concept for the Register File. In a single clock cycle an ALU operation using two register operands is executed, and the result is stored back to the destination register.

**Figure 7.** Single Cycle ALU Operation




## Reset and Interrupt Handling

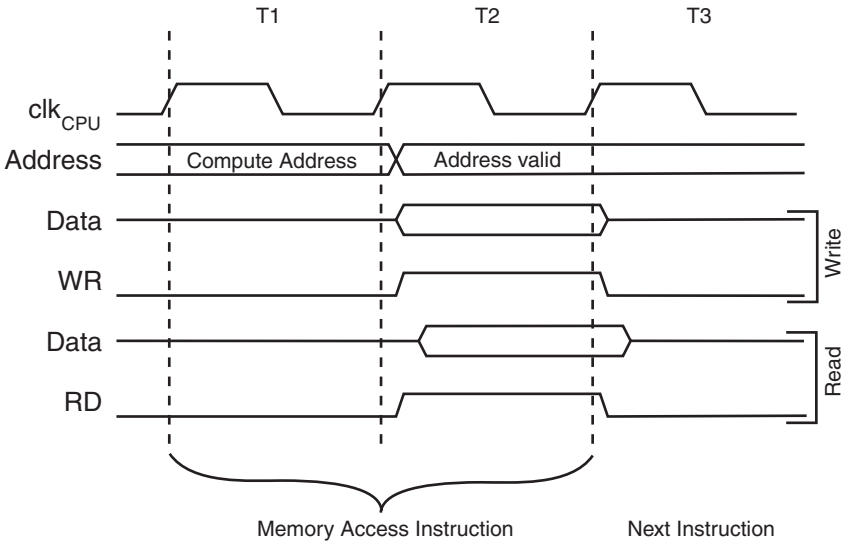
The AVR provides several different interrupt sources. These interrupts and the separate Reset Vector each have a separate program vector in the program memory space. All interrupts are assigned individual enable bits which must be written logic one together with the Global Interrupt Enable bit in the Status Register in order to enable the interrupt. Depending on the Program Counter value, interrupts may be automatically disabled when Boot Lock bits BLB02 or BLB12 are programmed. This feature improves software security. See the section “Memory Programming” on page 246 for details.

The lowest addresses in the program memory space are by default defined as the Reset and Interrupt Vectors. The complete list of vectors is shown in “Interrupts” on page 46. The list also determines the priority levels of the different interrupts. The lower the address the higher is the priority level. RESET has the highest priority, and next is INT0 – the External Interrupt Request 0. The Interrupt Vectors can be moved to the start of the Boot Flash section by setting the IVSEL bit in the MCU Control Register (MCUCR). Refer to “Interrupts” on page 46 for more information. The Reset Vector can also be

### Data Memory Access Times

This section describes the general access timing concepts for internal memory access. The internal data SRAM access is performed in two $clk_{CPU}$ cycles as described in Figure 10.

**Figure 10.** On-chip Data SRAM Access Cycles




## EEPROM Data Memory

The ATmega165 contains 512 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 100,000 write/erase cycles. The access between the EEPROM and the CPU is described in the following, specifying the EEPROM Address Registers, the EEPROM Data Register, and the EEPROM Control Register.

For a detailed description of SPI, JTAG and Parallel data downloading to the EEPROM, see page 261, page 266, and page 249 respectively.

### EEPROM Read/Write Access

The EEPROM Access Registers are accessible in the I/O space.

The write access time for the EEPROM is given in Table 1. A self-timing function, however, lets the user software detect when the next byte can be written. If the user code contains instructions that write the EEPROM, some precautions must be taken. In heavily filtered power supplies, $V_{CC}$ is likely to rise or fall slowly on power-up/down. This causes the device for some period of time to run at a voltage lower than specified as minimum for the clock frequency used. See “Preventing EEPROM Corruption” on page 21. for details on how to avoid problems in these situations.

In order to prevent unintentional EEPROM writes, a specific write procedure must be followed. Refer to the description of the EEPROM Control Register for details on this.

When the EEPROM is read, the CPU is halted for four clock cycles before the next instruction is executed. When the EEPROM is written, the CPU is halted for two clock cycles before the next instruction is executed.

### The EEPROM Address Register – EEARH and EEARL

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| | – | – | – | – | – | – | – | EEAR8 | EEARH |
| | EEAR7 | EEAR6 | EEAR5 | EEAR4 | EEAR3 | EEAR2 | EEAR1 | EEAR0 | EEARL |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Read/Write | R | R | R | R | R | R | R | R/W | |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | |
| | X | X | X | X | X | X | X | X | |

- **Bits 15..9 – Res: Reserved Bits**

These bits are reserved bits in the ATmega165 and will always read as zero.

- **Bits 8..0 – EEAR8..0: EEPROM Address**

The EEPROM Address Registers – EEARH and EEARL specify the EEPROM address in the 512 bytes EEPROM space. The EEPROM data bytes are addressed linearly between 0 and 511. The initial value of EEAR is undefined. A proper value must be written before the EEPROM may be accessed.

### The EEPROM Data Register – EEDR

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | MSB | | | | | | | LSB | EEDR |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bits 7..0 – EEDR7..0: EEPROM Data**

For the EEPROM write operation, the EEDR Register contains the data to be written to the EEPROM in the address given by the EEAR Register. For the EEPROM read operation, the EEDR contains the data read out from the EEPROM at the address given by EEAR.

### The EEPROM Control Register – EECR

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | – | – | – | – | EERIE | EEMWE | EEWE | EERE | EECR |
| Read/Write | R | R | R | R | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | |

- **Bits 7..4 – Res: Reserved Bits**

These bits are reserved bits in the ATmega165 and will always read as zero.

- **Bit 3 – EERIE: EEPROM Ready Interrupt Enable**

Writing EERIE to one enables the EEPROM Ready Interrupt if the I bit in SREG is set. Writing EERIE to zero disables the interrupt. The EEPROM Ready interrupt generates a constant interrupt when EEWE is cleared.

- **Bit 2 – EEMWE: EEPROM Master Write Enable**

The EEMWE bit determines whether setting EEWE to one causes the EEPROM to be written. When EEMWE is set, setting EEWE within four clock cycles will write data to the EEPROM at the selected address. If EEMWE is zero, setting EEWE will have no effect. When EEMWE has been written to one by software, hardware clears the bit to zero after four clock cycles. See the description of the EEWE bit for an EEPROM write procedure.

Oscillator is stopped during sleep. If the Timer/Counter2 is using the synchronous clock, the clock source is stopped during sleep. Note that even if the synchronous clock is running in Power-save, this clock is only available for the Timer/Counter2.

## Standby Mode

When the SM2..0 bits are 110 and an external crystal/resonator clock option is selected, the SLEEP instruction makes the MCU enter Standby mode. This mode is identical to Power-down with the exception that the Oscillator is kept running. From Standby mode, the device wakes up in six clock cycles.

**Table 15.** Active Clock Domains and Wake-up Sources in the Different Sleep Modes.

| | Active Clock Domains | | | | | Oscillators | | Wake-up Sources | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Sleep Mode** | **$clk_{CPU}$** | **$clk_{FLASH}$** | **$clk_{IO}$** | **$clk_{ADC}$** | **$clk_{ASY}$** | **Main Clock Source Enabled** | **Timer Osc Enabled** | **INT0 and Pin Change** | **USI Start Condition** | **Timer2** | **SPM/ EEPROM Ready** | **ADC** | **Other I/O** |
| Idle | | | X | X | X | X | X(2) | X | X | X | X | X | X |
| ADC Noise Reduction | | | | X | X | X | X(2) | X(3) | X | X(2) | X | X | |
| Power-down | | | | | | | | X(3) | X | | | | |
| Power-save | | | | | X | | X | X(3) | X | X | | | |
| Standby(1) | | | | | | X | | X(3) | X | | | | |

Notes: 1. Only recommended with external crystal or resonator selected as clock source.
2. If Timer/Counter2 is not running in asynchronous mode.
3. For INT0, only level interrupt.

## Power Reduction Register

The Power Reduction Register, PRR, provides a method to stop the clock to individual peripherals to reduce power consumption. The current state of the peripheral is frozen and the I/O registers can not be read or written. Resources used by the peripheral when stopping the clock will remain occupied, hence the peripheral should in most cases be disabled before stopping the clock. Waking up a module, which is done by clearing the bit in PRR, puts the module in the same state as before shutdown.

Module shutdown can be used in Idle mode and Active mode to significantly reduce the overall power consumption. See “Supply Current of I/O modules” on page 290 for examples. In all other sleep modes, the clock is already stopped.

### Power Reduction Register - PRR

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | – | – | – | – | PRTIM1 | PRSPI | PRUSART0 | PRADC | PRR |
| Read/Write | R | R | R | R | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bit 7..4 - Res: Reserved bits**

These bits are reserved in ATmega165 and will always read as zero.

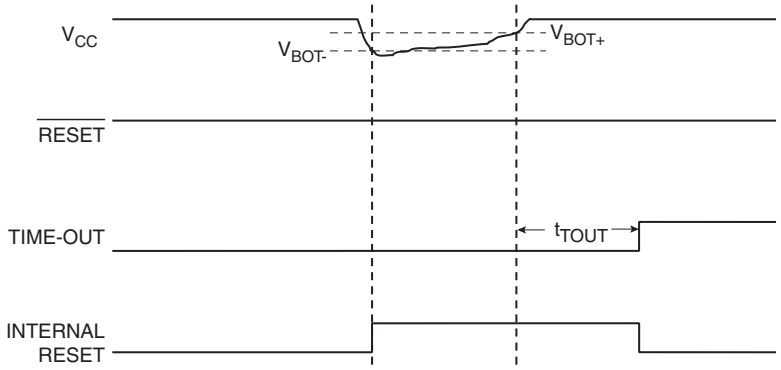
- **Bit 3 - PRTIM1: Power Reduction Timer/Counter1**

Writing a logic one to this bit shuts down the Timer/Counter1 module. When the Timer/Counter1 is enabled, operation will continue like before the shutdown.

When the BOD is enabled, and $V_{CC}$ decreases to a value below the trigger level ($V_{BOT-}$ in Figure 18), the Brown-out Reset is immediately activated. When $V_{CC}$ increases above the trigger level ($V_{BOT+}$ in Figure 18), the delay counter starts the MCU after the Time-out period $t_{TOUT}$ has expired.

The BOD circuit will only detect a drop in $V_{CC}$ if the voltage stays below the trigger level for longer than $t_{BOD}$ given in Table 16.

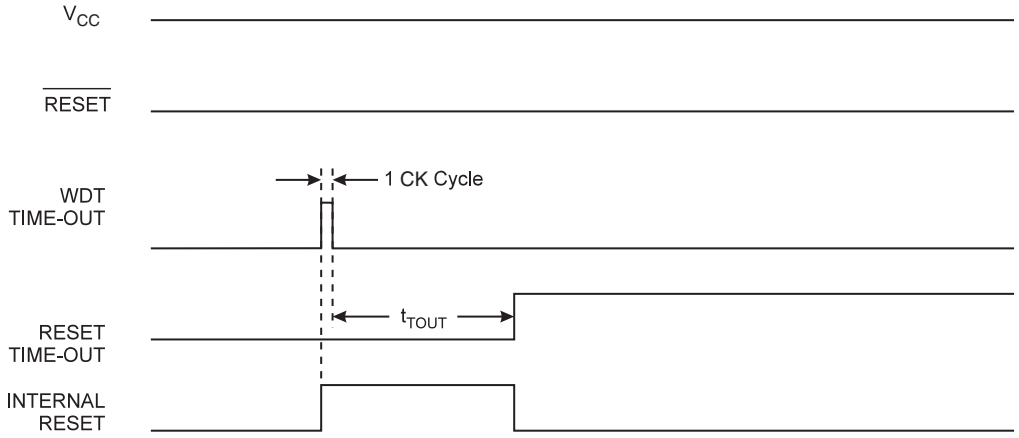
**Figure 18.** Brown-out Reset During Operation




## Watchdog Reset

When the Watchdog times out, it will generate a short reset pulse of one CK cycle duration. On the falling edge of this pulse, the delay timer starts counting the Time-out period $t_{TOUT}$. Refer to page 43 for details on operation of the Watchdog Timer.

**Figure 19.** Watchdog Reset During Operation




## MCU Status Register – MCUSR

The MCU Status Register provides information on which reset source caused an MCU reset.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | – | – | – | JTRF | WDRF | BORF | EXTRF | PORF | MCUSR |
| Read/Write | R | R | R | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | See Bit Description | | | | | |

- **Bit 4 – JTRF: JTAG Reset Flag**

This bit is set if a reset is being caused by a logic one in the JTAG Reset Register selected by the JTAG instruction AVR_RESET. This bit is reset by a Power-on Reset, or by writing a logic zero to the flag.

- **Bit 3 – WDRF: Watchdog Reset Flag**

This bit is set if a Watchdog Reset occurs. The bit is reset by a Power-on Reset, or by writing a logic zero to the flag.

- **Bit 2 – BORF: Brown-out Reset Flag**

This bit is set if a Brown-out Reset occurs. The bit is reset by a Power-on Reset, or by writing a logic zero to the flag.

- **Bit 1 – EXTRF: External Reset Flag**

This bit is set if an External Reset occurs. The bit is reset by a Power-on Reset, or by writing a logic zero to the flag.

- **Bit 0 – PORF: Power-on Reset Flag**

This bit is set if a Power-on Reset occurs. The bit is reset only by writing a logic zero to the flag.

To make use of the Reset Flags to identify a reset condition, the user should read and then Reset the MCUSR as early as possible in the program. If the register is cleared before another reset occurs, the source of the reset can be found by examining the Reset Flags.

## Internal Voltage Reference

ATmega165 features an internal bandgap reference. This reference is used for Brown-out Detection, and it can be used as an input to the Analog Comparator or the ADC.

### Voltage Reference Enable Signals and Start-up Time

The voltage reference has a start-up time that may influence the way it should be used. The start-up time is given in Table 19. To save power, the reference is not always turned on. The reference is on during the following situations:

1. When the BOD is enabled (by programming the BODLEVEL [2..0] Fuse).
2. When the bandgap reference is connected to the Analog Comparator (by setting the ACBG bit in ACSR).
3. When the ADC is enabled.

Thus, when the BOD is not enabled, after setting the ACBG bit or enabling the ADC, the user must always allow the reference to start up before the output from the Analog Comparator or ADC is used. To reduce power consumption in Power-down mode, the user can avoid the three conditions above to ensure that the reference is turned off before entering Power-down mode.

**Table 19.** Internal Voltage Reference Characteristics[1]

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{BG}$ | Bandgap reference voltage | $V_{CC}$ = 2.7V, $T_A$ = 25°C | 1.0 | 1.1 | 1.2 | V |
| $t_{BG}$ | Bandgap reference start-up time | $V_{CC}$ = 2.7V, $T_A$ = 25°C | | 40 | 70 | µs |
| $I_{BG}$ | Bandgap reference current consumption | $V_{CC}$ = 2.7V, $T_A$ = 25°C | | 15 | | µA |

Note: 1. Values are guidelines only. Actual values are TBD.

- **TDO, ADC6 – Port F, Bit 6**

ADC6, Analog to Digital Converter, Channel 6.

TDO, JTAG Test Data Out: Serial output data from Instruction Register or Data Register. When the JTAG interface is enabled, this pin can not be used as an I/O pin. In TAP states that shift out data, the TDO pin drives actively. In other states the pin is pulled high.

- **TMS, ADC5 – Port F, Bit 5**

ADC5, Analog to Digital Converter, Channel 5.

TMS, JTAG Test mode Select: This pin is used for navigating through the TAP-controller state machine. When the JTAG interface is enabled, this pin can not be used as an I/O pin.

- **TCK, ADC4 – Port F, Bit 4**

ADC4, Analog to Digital Converter, Channel 4.

TCK, JTAG Test Clock: JTAG operation is synchronous to TCK. When the JTAG interface is enabled, this pin can not be used as an I/O pin.

- **ADC3 - ADC0 – Port F, Bit 3:0**

Analog to Digital Converter, Channel 3-0.

**Table 36.** Overriding Signals for Alternate Functions in PF7..PF4

| Signal Name | PF7/ADC7/TDI | PF6/ADC6/TDO | PF5/ADC5/TMS | PF4/ADC4/TCK |
|---|---|---|---|---|
| PUOE | JTAGEN | JTAGEN | JTAGEN | JTAGEN |
| PUOV | 1 | 1 | 1 | 1 |
| DDOE | JTAGEN | JTAGEN | JTAGEN | JTAGEN |
| DDOV | 0 | SHIFT_IR + SHIFT_DR | 0 | 0 |
| PVOE | 0 | JTAGEN | 0 | 0 |
| PVOV | 0 | TDO | 0 | 0 |
| PTOE | – | – | – | – |
| DIEOE | JTAGEN | JTAGEN | JTAGEN | JTAGEN |
| DIEOV | 0 | 0 | 0 | 0 |
| DI | – | – | – | – |
| AIO | TDI<br>ADC7 INPUT | ADC6 INPUT | TMS<br>ADC5 INPUT | TCK<br>ADC4 INPUT |

## 8-bit Timer/Counter0 with PWM

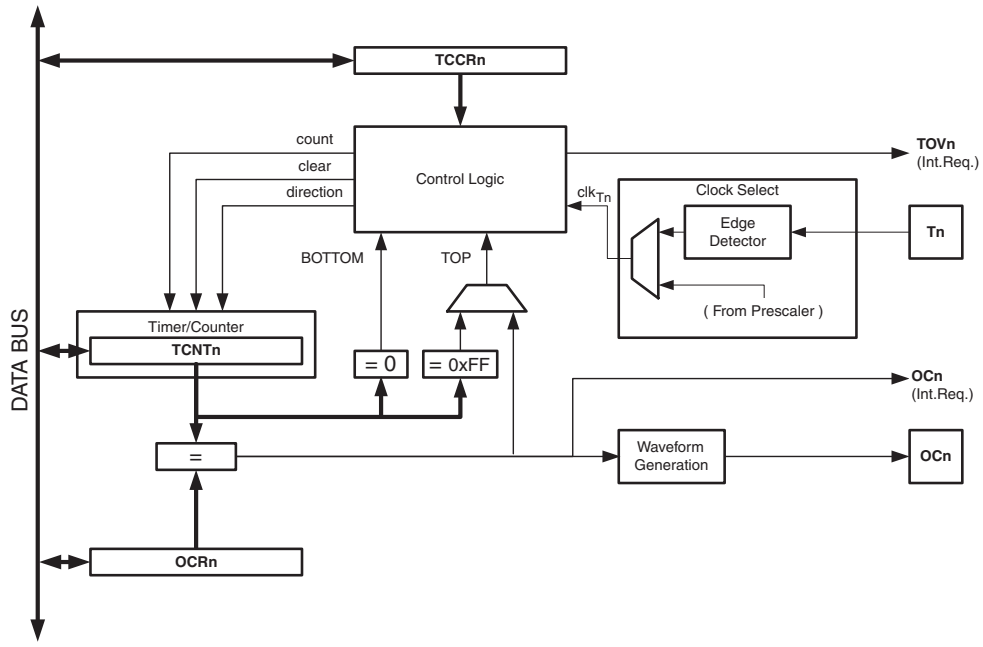
Timer/Counter0 is a general purpose, single compare unit, 8-bit Timer/Counter module. The main features are:

- **Single Compare Unit Counter**
- **Clear Timer on Compare Match (Auto Reload)**
- **Glitch-free, Phase Correct Pulse Width Modulator (PWM)**
- **Frequency Generator**
- **External Event Counter**
- **10-bit Clock Prescaler**
- **Overflow and Compare Match Interrupt Sources (TOV0 and OCF0A)**

### Overview

A simplified block diagram of the 8-bit Timer/Counter is shown in Figure 27. For the actual placement of I/O pins, refer to “Pinout ATmega165” on page 2. CPU accessible I/O Registers, including I/O bits and I/O pins, are shown in bold. The device-specific I/O Register and bit locations are listed in the “8-bit Timer/Counter Register Description” on page 85.

**Figure 27.** 8-bit Timer/Counter Block Diagram




### Registers

The Timer/Counter (TCNT0) and Output Compare Register (OCR0A) are 8-bit registers. Interrupt request (abbreviated to Int.Req. in the figure) signals are all visible in the Timer Interrupt Flag Register (TIFR0). All interrupts are individually masked with the Timer Interrupt Mask Register (TIMSK0). TIFR0 and TIMSK0 are not shown in the figure.

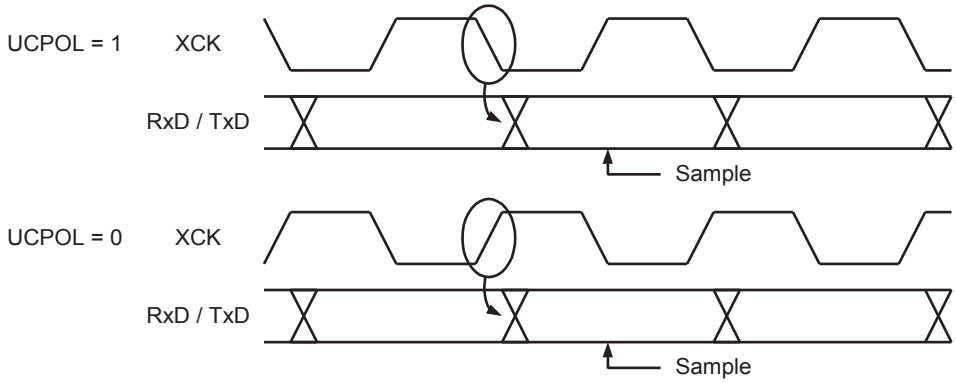
The Timer/Counter can be clocked internally, via the prescaler, or by an external clock source on the T0 pin. The Clock Select logic block controls which clock source and edge the Timer/Counter uses to increment (or decrement) its value. The Timer/Counter is inactive when no clock source is selected. The output from the Clock Select logic is referred to as the timer clock ($clk_{T0}$).

The double buffered Output Compare Register (OCR0A) is compared with the Timer/Counter value at all times. The result of the compare can be used by the Waveform Generator to generate a PWM or variable frequency output on the Output Compare pin (OC0A). See “Output Compare Unit” on page 77. for details. The compare match

### Synchronous Clock Operation

When synchronous mode is used (UMSEL = 1), the XCK pin will be used as either clock input (Slave) or clock output (Master). The dependency between the clock edges and data sampling or data change is the same. The basic principle is that data input (on RxD) is sampled at the opposite XCK clock edge of the edge the data output (TxD) is changed.

**Figure 71.** Synchronous Mode XCK Timing.




The UCPOL bit UCRSC selects which XCK clock edge is used for data sampling and which is used for data change. As Figure 71 shows, when UCPOL is zero the data will be changed at rising XCK edge and sampled at falling XCK edge. If UCPOL is set, the data will be changed at falling XCK edge and sampled at rising XCK edge.

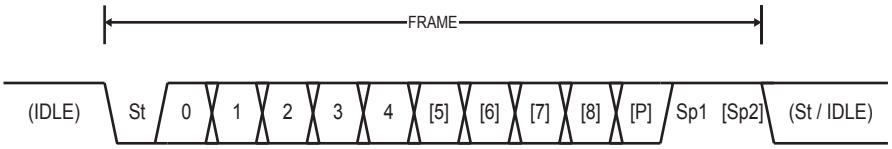
## Frame Formats

A serial frame is defined to be one character of data bits with synchronization bits (start and stop bits), and optionally a parity bit for error checking. The USART accepts all 30 combinations of the following as valid frame formats:

- 1 start bit
- 5, 6, 7, 8, or 9 data bits
- no, even or odd parity bit
- 1 or 2 stop bits

A frame starts with the start bit followed by the least significant data bit. Then the next data bits, up to a total of nine, are succeeding, ending with the most significant bit. If enabled, the parity bit is inserted after the data bits, before the stop bits. When a complete frame is transmitted, it can be directly followed by a new frame, or the communication line can be set to an idle (high) state. Figure 72 illustrates the possible combinations of the frame formats. Bits inside brackets are optional.

**Figure 72.** Frame Formats




**St** Start bit, always low.

**(n)** Data bits (0 to 8).

**P** Parity bit. Can be odd or even.

The Two-wire clock control unit can generate an interrupt when a start condition is detected on the Two-wire bus. It can also generate wait states by holding the clock pin low after a start condition is detected, or after the counter overflows.

## Functional Descriptions

### Three-wire Mode

The USI Three-wire mode is compliant to the Serial Peripheral Interface (SPI) mode 0 and 1, but does not have the slave select (SS) pin functionality. However, this feature can be implemented in software if necessary. Pin names used by this mode are: DI, DO, and USCK.

**Figure 77.** Three-wire Mode Operation, Simplified Diagram

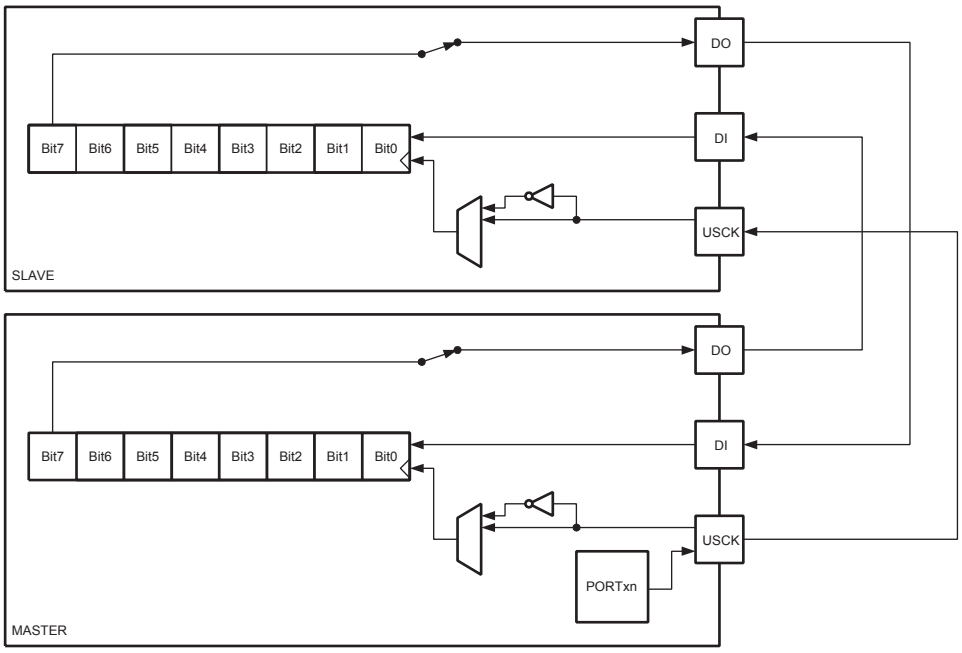



Figure 77 shows two USI units operating in Three-wire mode, one as Master and one as Slave. The two Shift Registers are interconnected in such way that after eight USCK clocks, the data in each register are interchanged. The same clock also increments the USI's 4-bit counter. The Counter Overflow (interrupt) Flag, or USIOIF, can therefore be used to determine when a transfer is completed. The clock is generated by the Master device software by toggling the USCK pin via the PORT Register or by writing a one to the USITC bit in USICR.

**Figure 78.** Three-wire Mode, Timing Diagram

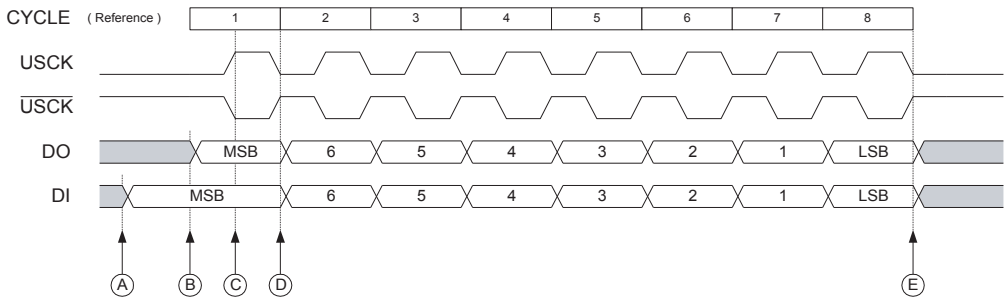


**Table 81.** Correlation Between Input Voltage and Output Codes

| $V_{ADCn}$ | Read Code | Corresponding Decimal Value |
|---|---|---|
| $V_{ADCm} + V_{REF}$ | 0x1FF | 511 |
| $V_{ADCm} + {}^{511}/_{512}\ V_{REF}$ | 0x1FF | 511 |
| $V_{ADCm} + {}^{510}/_{512}\ V_{REF}$ | 0x1FE | 510 |
| ... | ... | ... |
| $V_{ADCm} + {}^{1}/_{512}\ V_{REF}$ | 0x001 | 1 |
| $V_{ADCm}$ | 0x000 | 0 |
| $V_{ADCm} - {}^{1}/_{512}\ V_{REF}$ | 0x3FF | -1 |
| ... | ... | ... |
| $V_{ADCm} - {}^{511}/_{512}\ V_{REF}$ | 0x201 | -511 |
| $V_{ADCm} - V_{REF}$ | 0x200 | -512 |

ADMUX = 0xFB (ADC3 - ADC2, 1.1V reference, left adjusted result)

Voltage on ADC3 is 300 mV, voltage on ADC2 is 500 mV.

ADCR = 512 * (300 - 500) / 1100 = -93 = 0x3A3.

ADCL will thus read 0xC0, and ADCH will read 0xD8. Writing zero to ADLAR right adjusts the result: ADCL = 0xA3, ADCH = 0x03.

### ADC Multiplexer Selection Register – ADMUX

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | REFS1 | REFS0 | ADLAR | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 | ADMUX |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bit 7:6 – REFS1:0: Reference Selection Bits**

These bits select the voltage reference for the ADC, as shown in Table 82. If these bits are changed during a conversion, the change will not go in effect until this conversion is complete (ADIF in ADCSRA is set). The internal voltage reference options may not be used if an external reference voltage is being applied to the AREF pin.

**Table 82.** Voltage Reference Selections for ADC

| REFS1 | REFS0 | Voltage Reference Selection |
|---|---|---|
| 0 | 0 | AREF, Internal Vref turned off |
| 0 | 1 | AVCC with external capacitor at AREF pin |
| 1 | 0 | Reserved |
| 1 | 1 | Internal 1.1V Voltage Reference with external capacitor at AREF pin |

- **Bit 5 – ADLAR: ADC Left Adjust Result**

The ADLAR bit affects the presentation of the ADC conversion result in the ADC Data Register. Write one to ADLAR to left adjust the result. Otherwise, the result is right adjusted. Changing the ADLAR bit will affect the ADC Data Register immediately, regardless of any ongoing conversions. For a complete description of this bit, see “The ADC Data Register – ADCL and ADCH” on page 204.

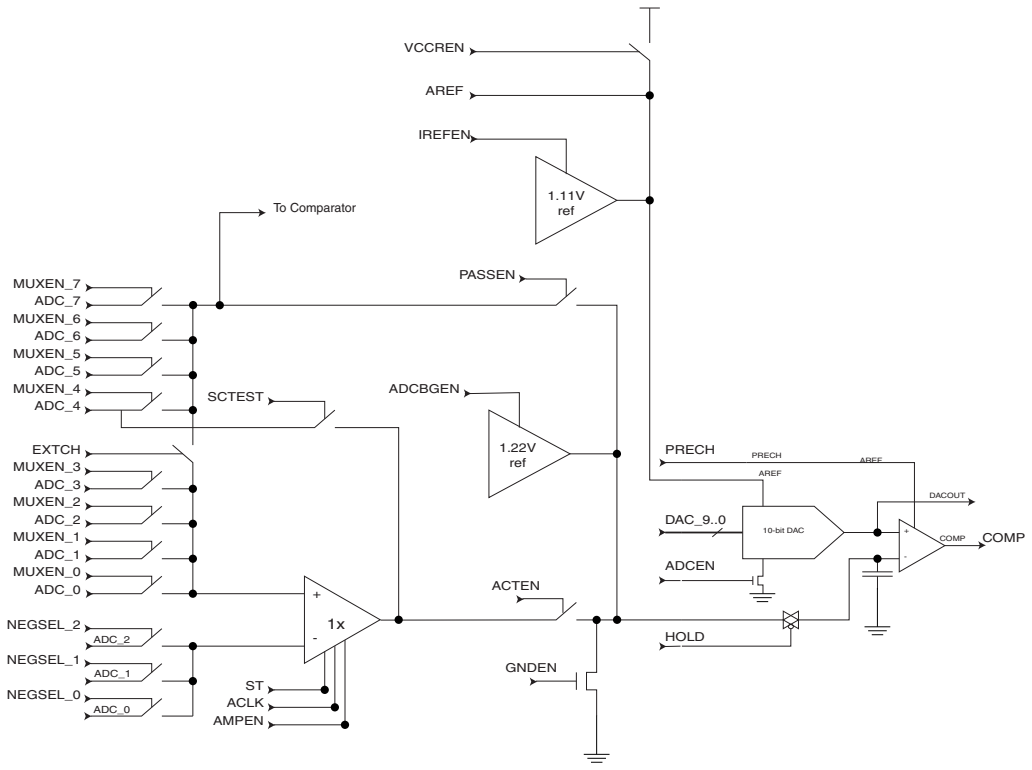
**Table 87.** Boundary-scan Signals for the Analog Comparator

| Signal Name | Direction as Seen from the Comparator | Description | Recommended Input when Not in Use | Output Values when Recommended Inputs are Used |
|---|---|---|---|---|
| AC_IDLE | input | Turns off Analog Comparator when true | 1 | Depends upon µC code being executed |
| ACO | output | Analog Comparator Output | Will become input to µC code being executed | 0 |
| ACME | input | Uses output signal from ADC mux when true | 0 | Depends upon µC code being executed |
| ACBG | input | Bandgap Reference enable | 0 | Depends upon µC code being executed |

## Scanning the ADC

Figure 107 shows a block diagram of the ADC with all relevant control and observe signals. The Boundary-scan cell from Figure 103 is attached to each of these signals. The ADC need not be used for pure connectivity testing, since all analog inputs are shared with a digital port pin as well.

**Figure 107.** Analog to Digital Converter




The signals are described briefly in Table 88.

As an example, consider the task of verifying a 1.5V ± 5% input signal at ADC channel 3 when the power supply is 5.0V and AREF is externally connected to $V_{CC}$.

The lower limit is: $\lceil 1024 \cdot 1.5V \cdot 0{,}95/5V \rceil = 291 = 0x123$
The upper limit is: $\lceil 1024 \cdot 1.5V \cdot 1.05/5V \rceil = 323 = 0x143$

The recommended values from Table 88 are used unless other values are given in the algorithm in Table 89. Only the DAC and port pin values of the Scan Chain are shown. The column “Actions” describes what JTAG instruction to be used before filling the Boundary-scan Register with the succeeding columns. The verification should be done on the data scanned out when scanning in the data on the same row in the table.

**Table 89.** Algorithm for Using the ADC

| Step | Actions | ADCEN | DAC | MUXEN | HOLD | PRECH | PA3. Data | PA3. Control | PA3. Pull-up_ Enable |
|---|---|---|---|---|---|---|---|---|---|
| 1 | SAMPLE_ PRELOAD | 1 | 0x200 | 0x08 | 1 | 1 | 0 | 0 | 0 |
| 2 | EXTEST | 1 | 0x200 | 0x08 | 0 | 1 | 0 | 0 | 0 |
| 3 | | 1 | 0x200 | 0x08 | 1 | 1 | 0 | 0 | 0 |
| 4 | | 1 | 0x123 | 0x08 | 1 | 1 | 0 | 0 | 0 |
| 5 | | 1 | 0x123 | 0x08 | 1 | 0 | 0 | 0 | 0 |
| 6 | Verify the COMP bit scanned out to be 0 | 1 | 0x200 | 0x08 | 1 | 1 | 0 | 0 | 0 |
| 7 | | 1 | 0x200 | 0x08 | 0 | 1 | 0 | 0 | 0 |
| 8 | | 1 | 0x200 | 0x08 | 1 | 1 | 0 | 0 | 0 |
| 9 | | 1 | 0x143 | 0x08 | 1 | 1 | 0 | 0 | 0 |
| 10 | | 1 | 0x143 | 0x08 | 1 | 0 | 0 | 0 | 0 |
| 11 | Verify the COMP bit scanned out to be 1 | 1 | 0x200 | 0x08 | 1 | 1 | 0 | 0 | 0 |

Using this algorithm, the timing constraint on the HOLD signal constrains the TCK clock frequency. As the algorithm keeps HOLD high for five steps, the TCK clock frequency has to be at least five times the number of scan bits divided by the maximum hold time, $t_{hold,max}$

## ATmega165 Boundary-scan Order

Table 90 shows the Scan order between TDI and TDO when the Boundary-scan chain is selected as data path. Bit 0 is the LSB; the first bit scanned in, and the first bit scanned out. The scan order follows the pin-out order as far as possible. Therefore, the bits of Port A is scanned in the opposite bit order of the other ports. Exceptions from the rules are the Scan chains for the analog circuits, which constitute the most significant bits of the scan chain regardless of which physical pin they are connected to. In Figure 101, PXn. Data corresponds to FF0, PXn. Control corresponds to FF1, and PXn. Pull-up_enable corresponds to FF2. Bit 4, 5, 6, and 7of Port F is not in the scan chain, since these pins constitute the TAP pins when the JTAG is enabled.

**Table 90.** ATmega165 Boundary-scan Order

| Bit Number | Signal Name | Module |
|---|---|---|
| 197 | AC_IDLE | Comparator |
| 196 | ACO | |
| 195 | ACME | |
| 194 | AINBG | |
| 193 | COMP | ADC |
| 192 | ACLK | |
| 191 | ACTEN | |
| 190 | PRIVATE_SIGNAL1[1] | |
| 189 | ADCBGEN | |
| 188 | ADCEN | |
| 187 | AMPEN | |
| 186 | DAC_9 | |
| 185 | DAC_8 | |
| 184 | DAC_7 | |
| 183 | DAC_6 | |
| 182 | DAC_5 | |
| 181 | DAC_4 | |
| 180 | DAC_3 | |
| 179 | DAC_2 | |
| 178 | DAC_1 | |
| 177 | DAC_0 | |
| 176 | EXTCH | |
| 175 | GNDEN | |
| 174 | HOLD | |
| 173 | IREFEN | |
| 172 | MUXEN_7 | |
| 171 | MUXEN_6 | |
| 170 | MUXEN_5 | |
| 169 | MUXEN_4 | |

### Programming the Fuse Low Bits

The algorithm for programming the Fuse Low bits is as follows (refer to “Programming the Flash” on page 252 for details on Command and Data loading):

1. A: Load Command “0100 0000”.
2. C: Load Data Byte. Bit n = “0” programs and bit n = “1” erases the Fuse bit.
3. Give $\overline{WR}$ a negative pulse and wait for RDY/$\overline{BSY}$ to go high.

### Programming the Fuse High Bits

The algorithm for programming the Fuse High bits is as follows (refer to “Programming the Flash” on page 252 for details on Command and Data loading):

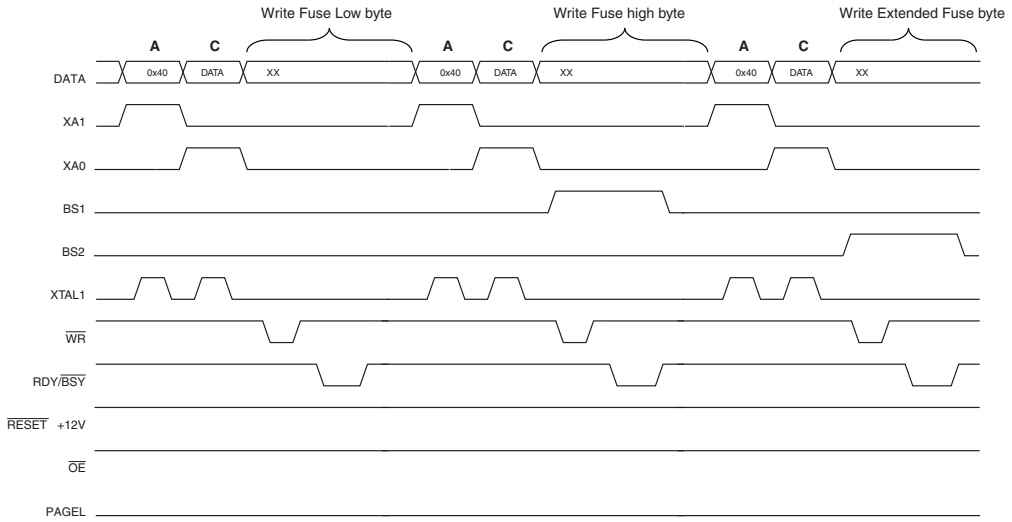
1. A: Load Command “0100 0000”.
2. C: Load Data Byte. Bit n = “0” programs and bit n = “1” erases the Fuse bit.
3. Set BS1 to “1” and BS2 to “0”. This selects high fuse byte.
4. Give $\overline{WR}$ a negative pulse and wait for RDY/$\overline{BSY}$ to go high.
5. Set BS1 to “0”. This selects low data byte.

### Programming the Extended Fuse Bits

The algorithm for programming the Extended Fuse bits is as follows (refer to “Programming the Flash” on page 252 for details on Command and Data loading):

1. 1. A: Load Command “0100 0000”.
2. 2. C: Load Data Byte. Bit n = “0” programs and bit n = “1” erases the Fuse bit.
3. 3. Set BS1 to “0” and BS2 to “1”. This selects extended fuse byte.
4. 4. Give $\overline{WR}$ a negative pulse and wait for RDY/$\overline{BSY}$ to go high.
5. 5. Set BS2 to “0”. This selects low data byte.

**Figure 115.** Programming the FUSES Waveforms




### Programming the Lock Bits

The algorithm for programming the Lock bits is as follows (refer to “Programming the Flash” on page 252 for details on Command and Data loading):

1. A: Load Command “0010 0000”.
2. C: Load Data Low Byte. Bit n = “0” programs the Lock bit. If LB mode 3 is programmed (LB1 and LB2 is programmed), it is not possible to program the Boot Lock bits by any External Programming mode.
3. Give $\overline{WR}$ a negative pulse and wait for RDY/$\overline{BSY}$ to go high.

The Lock bits can only be cleared by executing Chip Erase.

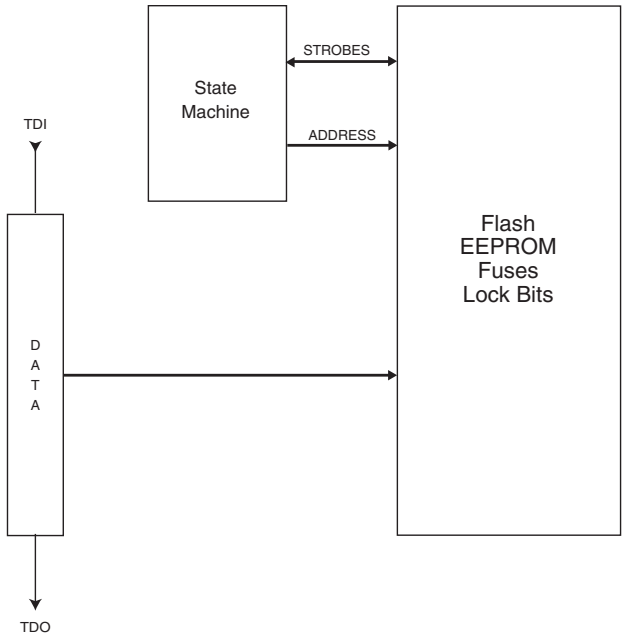
**Table 115.** JTAG Programming Instruction (Continued)
Set (Continued) **a** = address high bits, **b** = address low bits, **H** = 0 - Low byte, 1 - High Byte, **o** = data out, **i** = data in, x = don't care

| Instruction | TDI Sequence | TDO Sequence | Notes |
|---|---|---|---|
| 8f. Read Fuses and Lock Bits | 0111010_00000000<br>0111110_00000000<br>0110010_00000000<br>0110110_00000000<br>0110111_00000000 | xxxxxxx_xxxxxxxx<br>xxxxxxx_**oooooooo**<br>xxxxxxx_**oooooooo**<br>xxxxxxx_**oooooooo**<br>xxxxxxx_**oooooooo** | (5)<br>Fuse Ext. byte<br>Fuse High byte<br>Fuse Low byte<br>Lock bits |
| 9a. Enter Signature Byte Read | 0100011_00001000 | xxxxxxx_xxxxxxxx | |
| 9b. Load Address Byte | 0000011_**bbbbbbbb** | xxxxxxx_xxxxxxxx | |
| 9c. Read Signature Byte | 0110010_00000000<br>0110011_00000000 | xxxxxxx_xxxxxxxx<br>xxxxxxx_**oooooooo** | |
| 10a. Enter Calibration Byte Read | 0100011_00001000 | xxxxxxx_xxxxxxxx | |
| 10b. Load Address Byte | 0000011_**bbbbbbbb** | xxxxxxx_xxxxxxxx | |
| 10c. Read Calibration Byte | 0110110_00000000<br>0110111_00000000 | xxxxxxx_xxxxxxxx<br>xxxxxxx_**oooooooo** | |
| 11a. Load No Operation Command | 0100011_00000000<br>0110011_00000000 | xxxxxxx_xxxxxxxx<br>xxxxxxx_xxxxxxxx | |

Notes:
1. This command sequence is not required if the seven MSB are correctly set by the previous command sequence (which is normally the case).
2. Repeat until **o** = "1".
3. Set bits to "0" to program the corresponding Fuse, "1" to unprogram the Fuse.
4. Set bits to "0" to program the corresponding Lock bit, "1" to leave the Lock bit unchanged.
5. "0" = programmed, "1" = unprogrammed.
6. The bit mapping for Fuses Extended byte is listed in Table 101 on page 247
7. The bit mapping for Fuses High byte is listed in Table 102 on page 248
8. The bit mapping for Fuses Low byte is listed in Table 103 on page 248
9. The bit mapping for Lock bits byte is listed in Table 99 on page 246
10. Address bits exceeding PCMSB and EEAMSB (Table 105 and Table 106) are don't care
11. All TDI and TDO sequences are represented by binary digits (0b...).

including the first read byte. This ensures that the first data is captured from the first address set up by PROG_COMMANDS, and reading the last location in the page makes the program counter increment into the next page.

**Figure 126.** Flash Data Byte Register




The state machine controlling the Flash Data Byte Register is clocked by TCK. During normal operation in which eight bits are shifted for each Flash byte, the clock cycles needed to navigate through the TAP controller automatically feeds the state machine for the Flash Data Byte Register with sufficient number of clock pulses to complete its operation transparently for the user. However, if too few bits are shifted between each Update-DR state during page load, the TAP controller should stay in the Run-Test/Idle state for some TCK cycles to ensure that there are at least 11 TCK cycles between each Update-DR state.

**Programming Algorithm**

All references below of type “1a”, “1b”, and so on, refer to Table 115.

**Entering Programming Mode**

1. Enter JTAG instruction AVR_RESET and shift 1 in the Reset Register.
2. Enter instruction PROG_ENABLE and shift 0b1010_0011_0111_0000 in the Programming Enable Register.

**Leaving Programming Mode**

1. Enter JTAG instruction PROG_COMMANDS.
2. Disable all programming instructions by using no operation instruction 11a.
3. Enter instruction PROG_ENABLE and shift 0b0000_0000_0000_0000 in the programming Enable Register.
4. Enter JTAG instruction AVR_RESET and shift 0 in the Reset Register.

**Performing Chip Erase**

1. Enter JTAG instruction PROG_COMMANDS.
2. Start Chip Erase using programming instruction 1a.
3. Poll for Chip Erase complete using programming instruction 1b, or wait for $t_{WLRH\_CE}$ (refer to Table 112 on page 259).

ending with the MSB of the last instruction in the page (Flash). The Capture-DR state both captures the data from the Flash, and also auto-increments the program counter after each word is read. Note that Capture-DR comes before the shift-DR state. Hence, the first byte which is shifted out contains valid data.

6. Enter JTAG instruction PROG_COMMANDS.
7. Repeat steps 3 to 6 until all data have been read.

**Programming the EEPROM**

Before programming the EEPROM a Chip Erase must be performed, see "Performing Chip Erase" on page 275.

1. Enter JTAG instruction PROG_COMMANDS.
2. Enable EEPROM write using programming instruction 4a.
3. Load address High byte using programming instruction 4b.
4. Load address Low byte using programming instruction 4c.
5. Load data using programming instructions 4d and 4e.
6. Repeat steps 4 and 5 for all data bytes in the page.
7. Write the data using programming instruction 4f.
8. Poll for EEPROM write complete using programming instruction 4g, or wait for $t_{WLRH}$ (refer to Table 112 on page 259).
9. Repeat steps 3 to 8 until all data have been programmed.

Note that the PROG_PAGELOAD instruction can not be used when programming the EEPROM.

**Reading the EEPROM**

1. Enter JTAG instruction PROG_COMMANDS.
2. Enable EEPROM read using programming instruction 5a.
3. Load address using programming instructions 5b and 5c.
4. Read data using programming instruction 5d.
5. Repeat steps 3 and 4 until all data have been read.

Note that the PROG_PAGEREAD instruction can not be used when reading the EEPROM.

**Programming the Fuses**

1. Enter JTAG instruction PROG_COMMANDS.
2. Enable Fuse write using programming instruction 6a.
3. Load data high byte using programming instructions 6b. A bit value of "0" will program the corresponding fuse, a "1" will unprogram the fuse.
4. Write Fuse High byte using programming instruction 6c.
5. Poll for Fuse write complete using programming instruction 6d, or wait for $t_{WLRH}$ (refer to Table 112 on page 259).
6. Load data low byte using programming instructions 6e. A "0" will program the fuse, a "1" will unprogram the fuse.
7. Write Fuse low byte using programming instruction 6f.
8. Poll for Fuse write complete using programming instruction 6g, or wait for $t_{WLRH}$ (refer to Table 112 on page 259).

**Figure 163.** I/O Pin Source Current vs. Output Voltage, Port B ($V_{CC}$ = 2.7V)

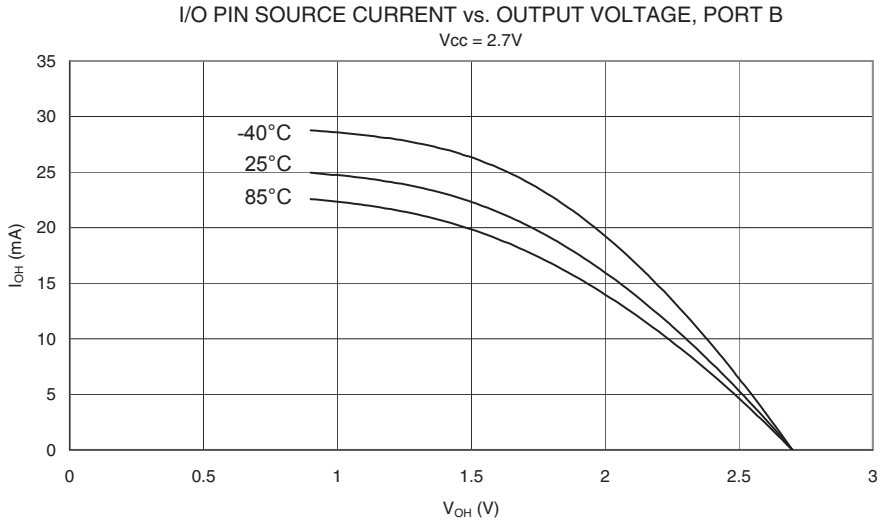



**Figure 164.** I/O Pin Source Current vs. Output Voltage, Port B ($V_{CC}$ = 1.8V)