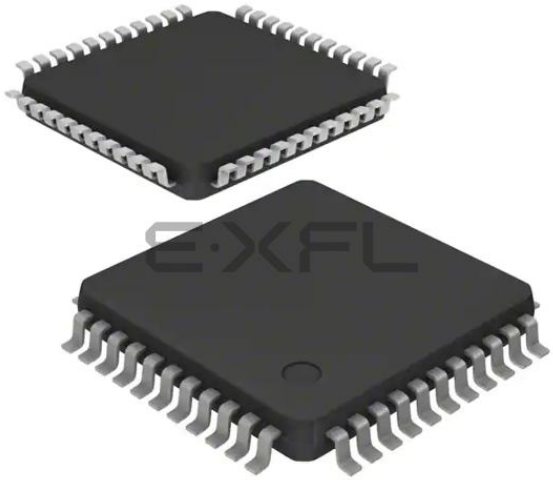

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f1621an020sc00tr

Use of All Uppercase Letters

The use of all uppercase letters designates the names of states, modes, and commands.

- Example 1: The bus is considered BUSY after the Start condition.
- Example 2: A START command triggers the processing of the initialization sequence.
- Example 3: STOP mode.

Bit Numbering

Bits are numbered from *0* to *n–1* where *n* indicates the total number of bits. For example, the 8 bits of a register are numbered from 0 to 7.

Safeguards

It is important that you understand the following safety terms, which are defined here.

Caution: *Indicates a procedure or file may become corrupted if you do not follow directions.*

Register File Address Map

Table 7 provides the address map for the Register File of the 64K Series products. Not all devices and package styles in the 64K Series support Timer 3 and all of the GPIO Ports. Consider registers for unimplemented peripherals as Reserved.

Table 7. Z8 Encore! XP 64K Series Flash Microcontrollers Register File Address Map

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
General-Purpose RAM				
000-EFF	General-Purpose Register File RAM	—	XX	
Timer 0				
F00	Timer 0 High Byte	T0H	00	90
F01	Timer 0 Low Byte	T0L	01	90
F02	Timer 0 Reload High Byte	T0RH	FF	91
F03	Timer 0 Reload Low Byte	T0RL	FF	91
F04	Timer 0 PWM High Byte	T0PWMH	00	92
F05	Timer 0 PWM Low Byte	T0PWML	00	92
F06	Timer 0 Control 0	T0CTL0	00	93
F07	Timer 0 Control 1	T0CTL1	00	94
Timer 1				
F08	Timer 1 High Byte	T1H	00	90
F09	Timer 1 Low Byte	T1L	01	90
F0A	Timer 1 Reload High Byte	T1RH	FF	91
F0B	Timer 1 Reload Low Byte	T1RL	FF	91
F0C	Timer 1 PWM High Byte	T1PWMH	00	92
F0D	Timer 1 PWM Low Byte	T1PWML	00	92
F0E	Timer 1 Control 0	T1CTL0	00	93
F0F	Timer 1 Control 1	T1CTL1	00	94
Timer 2				
F10	Timer 2 High Byte	T2H	00	90
F11	Timer 2 Low Byte	T2L	01	90
F12	Timer 2 Reload High Byte	T2RH	FF	91
F13	Timer 2 Reload Low Byte	T2RL	FF	91
F14	Timer 2 PWM High Byte	T2PWMH	00	92
F15	Timer 2 PWM Low Byte	T2PWML	00	92
F16	Timer 2 Control 0	T2CTL0	00	93
F17	Timer 2 Control 1	T2CTL1	00	94

Timer 1 PWM High Byte
T1PWMH (F0CH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Timer 1 PWM value [15:8]

Timer 1 PWM Low Byte
T1PWML (F0DH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Timer 1 PWM value [7:0]

Timer 1 Control 0
T1CTL0 (F0EH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Reserved

Cascade Timer
0 = Timer 1 Input signal is GPIO pin
1 = Timer 1 Input signal is Timer 0 out

Reserved

Timer 1 Control 1
T1CTL1 (F0FH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Timer Mode
000 = One-Shot mode
001 = CONTINUOUS mode
010 = COUNTER mode
011 = PWM mode
100 = CAPTURE mode
101 = COMPARE mode
110 = GATED mode
111 = Capture/COMPARE mode

Prescale Value
000 = Divide by 1
001 = Divide by 2
010 = Divide by 4
011 = Divide by 8
100 = Divide by 16
101 = Divide by 32
110 = Divide by 64
111 = Divide by 128

Timer Input/Output Polarity
Operation of this bit is a function of the current operating mode of the timer

Timer Enable
0 = Timer is disabled
1 = Timer is enabled

Timer 2 High Byte
T2H (F10H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Timer 2 current count value [15:8]

Timer 2 Low Byte
T2L (F11H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Timer 2 current count value [7:0]

Timer 2 Reload High Byte
T2RH (F12H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Timer 2 reload value [15:8]

Timer 2 Reload Low Byte
T2RL (F13H- Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Timer 2 reload value [7:0]

Timer 2 PWM High Byte
T2PWMH (F14H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Timer 2 PWM value [15:8]

Timer 2 PWM Low Byte
T2PWML (F15H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Timer 2 PWM value [7:0]

Timer 2 Control 0
T2CTL0 (F16H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Reserved

Cascade Timer
0 = Timer 2 Input signal is GPIO pin
1 = Timer 2 Input signal is Timer 1 out

Reserved

UART0 Transmit Data
U0TXD (F40H - Write Only)

D7	D6	D5	D4	D3	D2	D1	D0

UART0 transmitter data byte [7:0]

UART0 Receive Data
U0RXD (F40H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

UART0 receiver data byte [7:0]

UART0 Status 0
U0STAT0 (F41H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

$\overline{\text{CTS}}$ signal
Returns the level of the $\overline{\text{CTS}}$ signal

Transmitter Empty
0 = Data is currently transmitting
1 = Transmission is complete

Transmitter Data Register Empty
0 = Transmit Data Register is full
1 = Transmit Data register is empty

Break Detect
0 = No break occurred
1 = A break occurred

Framing Error
0 = No framing error occurred
1 = A framing occurred

Overrun Error
0 = No overrun error occurred
1 = An overrun error occurred

Parity Error
0 = No parity error occurred
1 = A parity error occurred

Receive Data Available
0 = Receive Data Register is empty
1 = A byte is available in the Receive Data Register

UART0 Control 0
U0CTL0 (F42H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Loop Back Enable
0 = Normal operation
1 = Transmit data is looped back to the receiver

Stop Bit Select
0 = Transmitter sends 1 Stop bit
1 = Transmitter sends 2 Stop bits

Send Break
0 = No break is sent
1 = Output of the transmitter is zero

Parity Select
0 = Even parity
1 = Odd parity

Parity Enable
0 = Parity is disabled
1 = Parity is enabled

$\overline{\text{CTS}}$ Enable
0 = CTS signal has no effect on the transmitter
1 = UART recognizes $\overline{\text{CTS}}$ signal as a transmit enable control signal

Receive Enable
0 = Receiver disabled
1 = Receiver enabled

Transmit Enable
0 = Transmitter disabled
1 = Transmitter enabled

Timers

Overview

The 64K Series products contain up to four 16-bit reloadable timers that can be used for timing, event counting, or generation of pulse width modulated signals. The timers' features include:

- 16-bit reload counter
- Programmable prescaler with prescale values from 1 to 128
- PWM output generation
- Capture and compare capability
- External input pin for timer input, clock gating, or capture signal. External input pin signal frequency is limited to a maximum of one-fourth the system clock frequency.
- Timer output pin
- Timer interrupt

In addition to the timers described in this chapter, the Baud Rate Generators for any unused UART, SPI, or I^2C peripherals may also be used to provide basic timing functionality. For information on using the Baud Rate Generators as timers, see the respective serial communication peripheral. Timer 3 is unavailable in the 44-pin package devices.

Architecture

Figure 12 displays the architecture of the timers.

2. Write to the Timer High and Low Byte registers to set the starting count value (usually 0001H), affecting only the first pass in CONTINUOUS mode. After the first timer Reload in CONTINUOUS mode, counting always begins at the reset value of 0001H.
3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
4. If desired, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
6. Write to the Timer Control 1 register to enable the timer and initiate counting.

In CONTINUOUS mode, the system clock always provides the timer input. The timer period is given by the following equation:

$$\text{CONTINUOUS Mode Time-Out Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, the ONE-SHOT mode equation must be used to determine the first time-out period.

COUNTER Mode

In COUNTER mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO Port pin Timer Input alternate function. The TPOL bit in the Timer Control 1 Register selects whether the count occurs on the rising edge or the falling edge of the Timer Input signal. In COUNTER mode, the prescaler is disabled.

Caution: *The input frequency of the Timer Input signal must not exceed one-fourth the system clock frequency.*

Upon reaching the Reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer Reload.

Follow the steps below for configuring a timer for COUNTER mode and initiating the count:

1. Write to the Timer Control 1 register to:
   – Disable the timer
   – Configure the timer for COUNTER mode

Table 42. Timer 0-3 Reload Low Byte Register (TxRL)

BITS	7	6	5	4	3	2	1	0
FIELD	TRL							
RESET	1							
R/W	R/W							
ADDR	F03H, F0BH, F13H, F1BH							

TRH and TRL—Timer Reload Register High and Low
These two bytes form the 16-bit Reload value, {TRH[7:0], TRL[7:0]}. This value sets the maximum count value which initiates a timer reload to 0001H. In COMPARE mode, these two byte form the 16-bit Compare value.

Timer 0-3 PWM High and Low Byte Registers

The Timer 0-3 PWM High and Low Byte (TxPWMH and TxPWML) registers (see Table 43 and Table 44 on page 92) are used for Pulse-Width Modulator (PWM) operations. These registers also store the Capture values for the Capture and Capture/COMPARE modes.

Table 43. Timer 0-3 PWM High Byte Register (TxPWMH)

BITS	7	6	5	4	3	2	1	0
FIELD	PWMH							
RESET	0							
R/W	R/W							
ADDR	F04H, F0CH, F14H, F1CH							

Table 44. Timer 0-3 PWM Low Byte Register (TxPWML)

BITS	7	6	5	4	3	2	1	0
FIELD	PWML							
RESET	0							
R/W	R/W							
ADDR	F05H, F0DH, F15H, F1DH							

1 = Infrared Encoder/Decoder is enabled. The UART transmits and receives data through the Infrared Encoder/Decoder.

UART Address Compare Register

The UART Address Compare register (Table 58) stores the multi-node network address of the UART. When the MPMD[1] bit of UART Control Register 0 is set, all incoming address bytes are compared to the value stored in the Address Compare register. Receive interrupts and RDA assertions only occur in the event of a match.

Table 58. UART Address Compare Register (U*x*ADDR)

BITS	7	6	5	4	3	2	1	0
FIELD	COMP_ADDR							
RESET	0							
R/W	R/W							
ADDR	F45H and F4DH							

COMP_ADDR—Compare Address
This 8-bit value is compared to the incoming address bytes.

UART Baud Rate High and Low Byte Registers

The UART Baud Rate High and Low Byte registers (see Table 59 and Table 60 on page 121) combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART. To configure the Baud Rate Generator as a timer with interrupt on time-out, complete the following procedure:

1. Disable the UART by clearing the REN and TEN bits in the UART Control 0 register to 0.
2. Load the desired 16-bit count value into the UART Baud Rate High and Low Byte registers.
3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BRGCTL bit in the UART Control 1 register to 1.

When configured as a general purpose timer, the UART BRG interrupt interval is calculated using the following equation:

$$\text{UART BRG Interrupt Interval}(s) = \text{System Clock Period (s)} \times \text{BRG}[15:0]$$

SPI Status Register

The SPI Status register (Table 65) indicates the current state of the SPI. All bits revert to their reset state if the SPIEN bit in the SPICTL register = 0.

Table 65. SPI Status Register (SPISTAT)

BITS	7	6	5	4	3	2	1	0
FIELD	IRQ	OVR	COL	ABT	Reserved		TXST	SLAS
RESET	0							1
R/W	R/W*				R			
ADDR	F62H							
Note: R/W* = Read access. Write a 1 to clear the bit to 0.								

IRQ—Interrupt Request
If SPIEN = 1, this bit is set if the STR bit in the SPICTL register is set, or upon completion of an SPI master or slave transaction. This bit does not set if SPIEN = 0 and the SPI Baud Rate Generator is used as a timer to generate the SPI interrupt.
0 = No SPI interrupt request pending.
1 = SPI interrupt request is pending.

OVR—Overrun
0 = An overrun error has not occurred.
1 = An overrun error has been detected.

COL—Collision
0 = A multi-master collision (mode fault) has not occurred.
1 = A multi-master collision (mode fault) has been detected.

ABT—Slave mode transaction abort
This bit is set if the SPI is configured in slave mode, a transaction is occurring and $\overline{SS}$ deasserts before all bits of a character have been transferred as defined by the NUMBITS field of the SPIMODE register. The IRQ bit also sets, indicating the transaction has completed.
0 = A slave mode transaction abort has not occurred.
1 = A slave mode transaction abort has been detected.

Reserved—Must be 0.

TXST—Transmit Status
0 = No data transmission currently in progress.
1 = Data transmission currently in progress.

SLAS—Slave Select
If SPI enabled as a Slave,

reading the I²C Data register. Once the I²C data register has been read, the I²C reads the next data byte.

Address Only Transaction with a 7-bit Address

In the situation where software determines if a slave with a 7-bit address is responding without sending or receiving data, a transaction can be done which only consists of an address phase. Figure 28 displays this 'address only' transaction to determine if a slave with a 7-bit address will acknowledge. As an example, this transaction can be used after a 'write' has been done to a EEPROM to determine when the EEPROM completes its internal write operation and is once again responding to I²C transactions. If the slave does not Acknowledge, the transaction can be repeated until the slave does Acknowledge.

S	Slave Address	W = 0	A/$\overline{A}$	P

Figure 28. 7-Bit Address Only Transaction Format

Follow the steps below for an address only transaction to a 7-bit addressed slave:

1. Software asserts the IEN bit in the I²C Control register.
2. Software asserts the TXI bit of the I²C Control register to enable Transmit interrupts.
3. The I²C interrupt asserts, because the I²C Data register is empty (TDRE = 1)
4. Software responds to the TDRE bit by writing a 7-bit slave address plus write bit (=0) to the I²C Data register. As an alternative this could be a read operation instead of a write operation.
5. Software sets the START and STOP bits of the I²C Control register and clears the TXI bit.
6. The I²C Controller sends the START condition to the I²C slave.
7. The I²C Controller loads the I²C Shift register with the contents of the I²C Data register.
8. Software polls the STOP bit of the I²C Control register. Hardware deasserts the STOP bit when the address only transaction is completed.
9. Software checks the ACK bit of the I²C Status register. If the slave acknowledged, the ACK bit is = 1. If the slave does not acknowledge, the ACK bit is = 0. The NCKI interrupt does not occur in the not acknowledge case because the STOP bit was set.

Caution: *Software must be cautious in making decisions based on this bit within a transaction because software cannot tell when the bit is updated by hardware. In the case of write transactions, the I²C pauses at the beginning of the Acknowledge cycle if the next transmit data or address byte has not been written (TDRE = 1) and STOP and START = 0. In this case the ACK bit is not updated until the transmit interrupt is serviced and the Acknowledge cycle for the previous byte completes. For examples of how the ACK bit can be used, see* Address Only Transaction with a 7-bit Address *on page 148* and Address Only Transaction with a 10-bit Address *on page 150*.

10B—10-Bit Address
This bit indicates whether a 10- or 7-bit address is being transmitted. After the START bit is set, if the five most-significant bits of the address are 11110B, this bit is set. When set, it is reset once the first byte of the address has been sent.

RD—Read
This bit indicates the direction of transfer of the data. It is active high during a read. The status of this bit is determined by the least-significant bit of the I²C Shift register after the START bit is set.

TAS—Transmit Address State
This bit is active high while the address is being shifted out of the I²C Shift register.

DSS—Data Shift State
This bit is active high while data is being shifted to or from the I²C Shift register.

NCKI—NACK Interrupt
This bit is set high when a Not Acknowledge condition is received or sent and neither the START nor the STOP bit is active. When set, this bit generates an interrupt that can only be cleared by setting the START or STOP bit, allowing you to specify whether to perform a STOP or a repeated START.

I²C Control Register

The I²C Control register (Table 72) enables the I²C operation.

Table 72. I²C Control Register (I2CCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	IEN	START	STOP	BIRQ	TXI	NAK	FLUSH	FILTEN
RESET	0							
R/W	R/W	R/W1	R/W1	R/W	R/W	R/W1	W1	R/W
ADDR	F52H							

Option Bits

Overview

Option Bits allow user configuration of certain aspects of the 64K Series operation. The feature configuration data is stored in the Flash Memory and read during Reset. The features available for control via the Option Bits are:

- Watchdog Timer time-out response selection–interrupt or Reset.
- Watchdog Timer enabled at Reset.
- The ability to prevent unwanted read access to user code in Flash Memory.
- The ability to prevent accidental programming and erasure of the user code in Flash Memory.
- Voltage Brownout configuration-always enabled or disabled during STOP mode to reduce STOP mode power consumption.
- Oscillator mode selection-for high, medium, and low power crystal oscillators, or external RC oscillator.

Operation

Option Bit Configuration By Reset

Each time the Option Bits are programmed or erased, the device must be Reset for the change to take place. During any reset operation (System Reset, Reset, or Stop Mode Recovery), the Option Bits are automatically read from the Flash Memory and written to Option Configuration registers. The Option Configuration registers control operation of the devices within the 64K Series. Option Bit control is established before the device exits Reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the Register File and are not accessible for read or write access.

Option Bit Address Space

The first two bytes of Flash Memory at addresses 0000H (see Table 98 on page 196) and 0001H (see Table 99 on page 197) are reserved for the user Option Bits. The byte at Flash Memory address 0000H configures user options. The byte at Flash Memory address 0001H is reserved for future use and must remain unprogrammed.

- **Write OCD Control Register (04H)**—The Write OCD Control Register command writes the data that follows to the OCDCTL register. When the Read Protect Option Bit is enabled, the DBGMODE bit (OCDCTL[7]) can only be set to 1, it cannot be cleared to 0 and the only method of putting the device back into normal operating mode is to reset the device.

```
DBG ← 04H
DBG ← OCDCTL[7:0]
```

- **Read OCD Control Register (05H)**—The Read OCD Control Register command reads the value of the OCDCTL register.

```
DBG ← 05H
DBG → OCDCTL[7:0]
```

- **Write Program Counter (06H)**—The Write Program Counter command writes the data that follows to the eZ8 CPU's Program Counter (PC). If the device is not in DEBUG mode or if the Read Protect Option Bit is enabled, the Program Counter (PC) values are discarded.

```
DBG ← 06H
DBG ← ProgramCounter[15:8]
DBG ← ProgramCounter[7:0]
```

- **Read Program Counter (07H)**—The Read Program Counter command reads the value in the eZ8 CPU's Program Counter (PC). If the device is not in DEBUG mode or if the Read Protect Option Bit is enabled, this command returns FFFFH.

```
DBG ← 07H
DBG → ProgramCounter[15:8]
DBG → ProgramCounter[7:0]
```

- **Write Register (08H)**—The Write Register command writes data to the Register File. Data can be written 1-256 bytes at a time (256 bytes can be written by setting size to zero). If the device is not in DEBUG mode, the address and data values are discarded. If the Read Protect Option Bit is enabled, then only writes to the Flash Control Registers are allowed and all other register write data values are discarded.

```
DBG ← 08H
DBG ← {4'h0,Register Address[11:8]}
DBG ← Register Address[7:0]
DBG ← Size[7:0]
DBG ← 1-256 data bytes
```

- **Read Register (09H)**—The Read Register command reads data from the Register File. Data can be read 1-256 bytes at a time (256 bytes can be read by setting size to zero). If the device is not in DEBUG mode or if the Read Protect Option Bit is enabled, this command returns FFH for all the data values.

```
DBG ← 09H
DBG ← {4'h0,Register Address[11:8]
DBG ← Register Address[7:0]
```

Table 106. DC Characteristics (Continued)

Symbol	Parameter	T_A = –40 °C to 125 °C			Units	Conditions
		Minimum	Typical	Maximum		
I_{DDS}	Stop Mode Supply Current (See Figure 47 and Figure 48) GPIO pins configured as outputs	–	520	700 650	µA	V_{DD} = 3.6 V, VBO and WDT Enabled V_{DD} = 3.3 V
		–	10	25 20	µA	V_{DD} = 3.6 V, T_A = 0 to 70 ºC VBO Disabled WDT Enabled V_{DD} = 3.3 V
		–		80 70	µA	V_{DD} = 3.6 V, T_A = –40 to +105 ºC VBO Disabled WDT Enabled V_{DD} = 3.3 V
		–		250 150	µA	V_{DD} = 3.6 V, T_A = –40 to +125 ºC VBO Disabled WDT Enabled V_{DD} = 3.3 V

[1]This condition excludes all pins that have on-chip pull-ups, when driven Low.

[2]These values are provided for design guidance only and are not tested in production.

Figure 45 displays the typical current consumption in HALT mode while operating at 25 ºC versus the system clock frequency. All GPIO pins are configured as outputs and driven High.

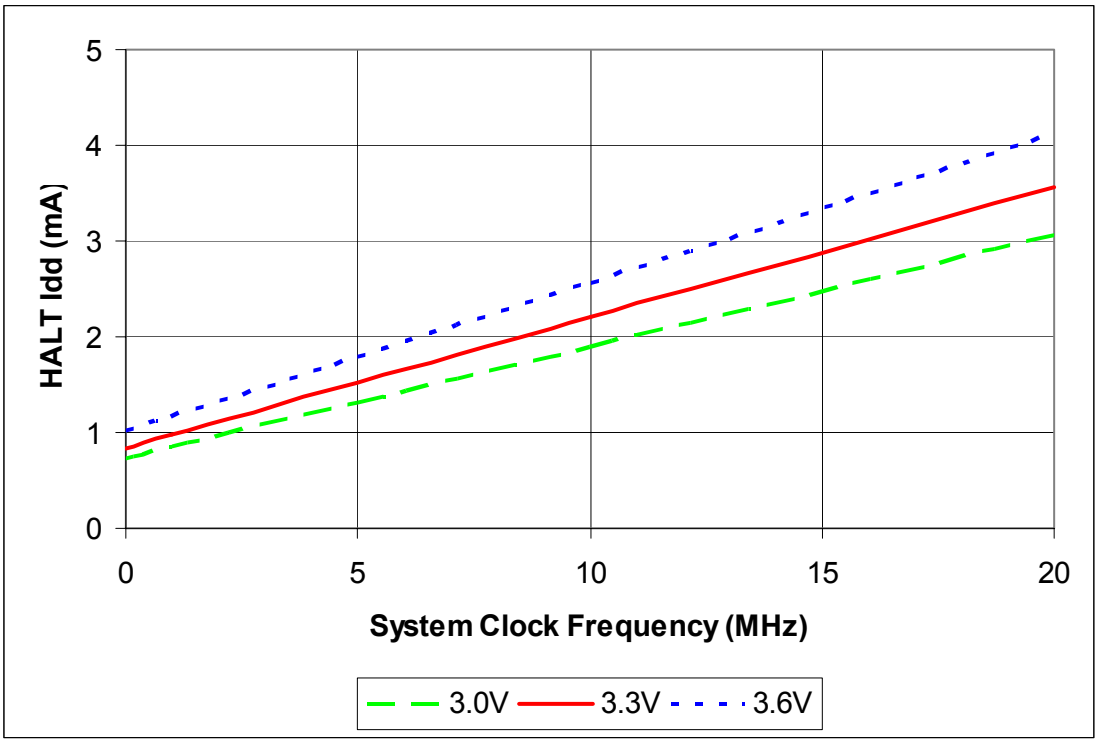


Figure 45. Typical HALT Mode Idd Versus System Clock Frequency

Table 112. Analog-to-Digital Converter Electrical Characteristics and Timing

Symbol	Parameter	V_{DD} = 3.0–3.6 V T_A = –40 °C to 125 °C			Units	Conditions
		Minimum	Typical	Maximum		
	Resolution	10	–	–	bits	External V_{REF} = 3.0 V;
	Differential Nonlinearity (DNL)	-1.0		+1.0	lsb	Guaranteed by design
	Integral Nonlinearity (INL)	-3.0	±1.0	3.0	lsb	External V_{REF} = 3.0 V
	DC Offset Error	-35	–	25	mV	
	DC Offset Error	-50	–	25	mV	44-pin LQFP, 44-pin PLCC, and 68-pin PLCC packages.
V_{REF}	Internal Reference Voltage	1.9	2.0	2.4	V	V_{DD} = 3.0 - 3.6 V T_A = -40 °C to 105 °C
VC_{REF}	Voltage Coefficient of Internal Reference Voltage	–	78	–	mV/V	V_{REF} variation as a function of AVDD.
TC_{REF}	Temperature Coefficient of Internal Reference Voltage	–	1	–	mV/°C	
	Single-Shot Conversion Period	–	5129	–	cycles	System clock cycles
	Continuous Conversion Period	–	256	–	cycles	System clock cycles
R_S	Analog Source Impedance	–	–	150	Ω	Recommended
Zin	Input Impedance		150		kΩ	
V_{REF}	External Reference Voltage			AVDD	V	AVDD <= VDD. When using an external reference voltage, decoupling capacitance should be placed from VREF to AVSS.
I_{REF}	Current draw into VREF pin when driving with external source.		25.0	40.0	µA	

SPI Master Mode Timing

Figure 53 and Table 117 provide timing information for SPI Master mode pins. Timing is shown with SCK rising edge used to source MOSI output data, SCK falling edge used to sample MISO input data. Timing on the SS output pin(s) is controlled by software.

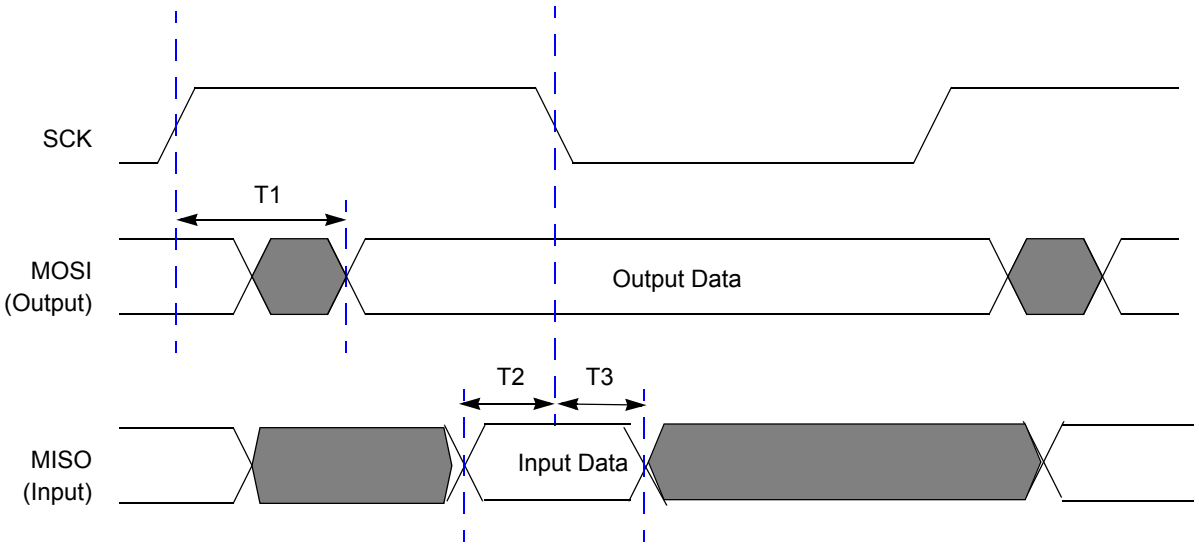


Figure 53. SPI Master Mode Timing

Table 117. SPI Master Mode Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Min**	**Max**
SPI Master			
T_1	SCK Rise to MOSI output Valid Delay	-5	+5
T_2	MISO input to SCK (receive edge) Setup Time	20	
T_3	MISO input to SCK (receive edge) Hold Time	0	

SPI Slave Mode Timing

Figure 54 and Table 118 provide timing information for the SPI slave mode pins. Timing is shown with SCK rising edge used to source MISO output data, SCK falling edge used to sample MOSI input data.

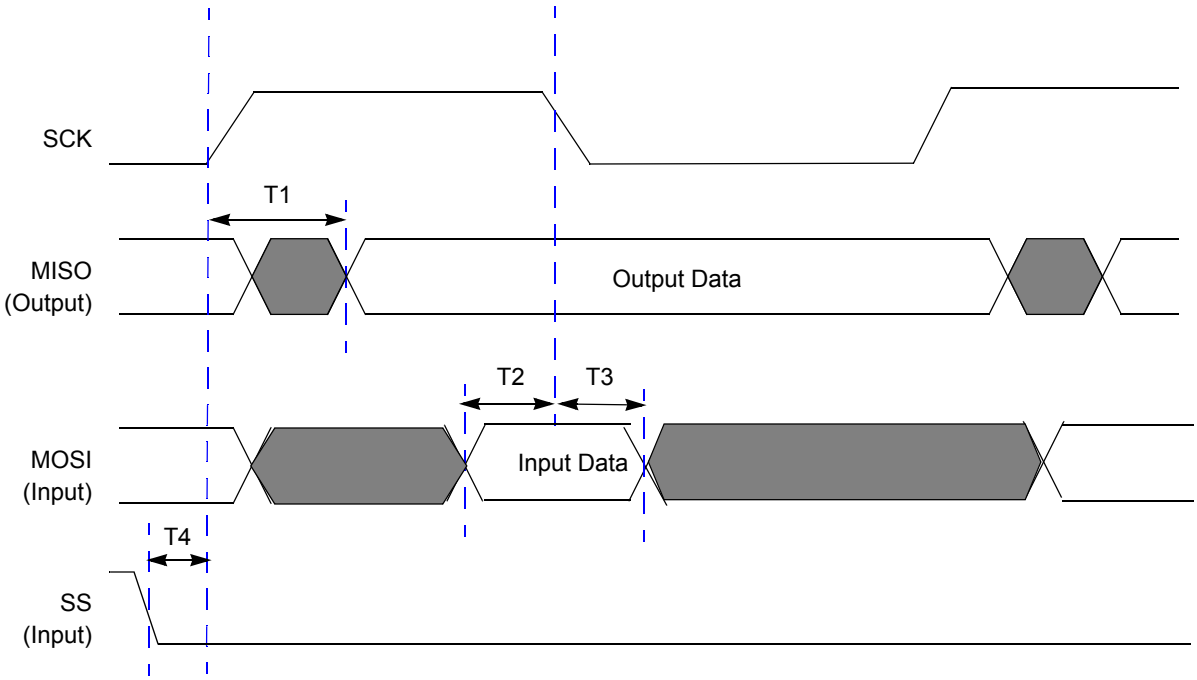


Figure 54. SPI Slave Mode Timing

Table 118. SPI Slave Mode Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
SPI Slave			
T_1	SCK (transmit edge) to MISO output Valid Delay	2 * Xin period	3 * Xin period + 20 nsec
T_2	MOSI input to SCK (receive edge) Setup Time	0	
T_3	MOSI input to SCK (receive edge) Hold Time	3 * Xin period	
T_4	SS input assertion to SCK setup	1 * Xin period	

Table 133. eZ8 CPU Instruction Summary (Continued)

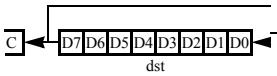
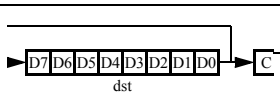
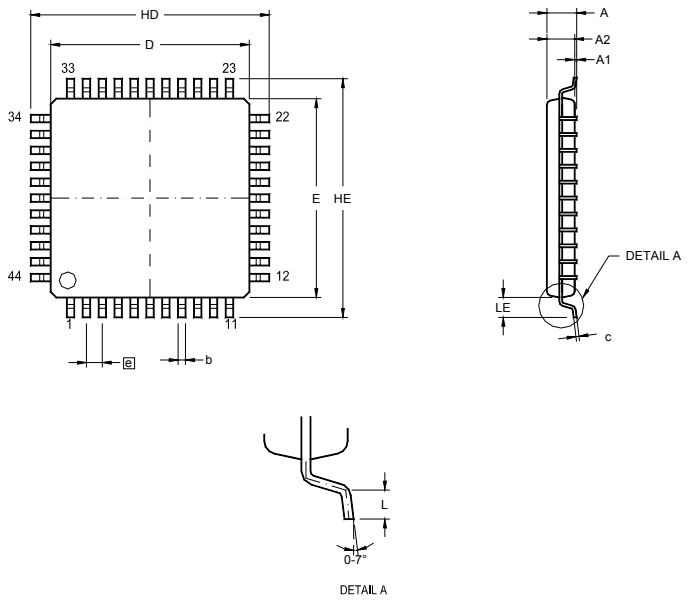
Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
OR dst, src	dst ← dst OR src	r	r	42	-	*	*	0	-	-	2	3
		r	Ir	43							2	4
		R	R	44							3	3
		R	IR	45							3	4
		R	IM	46							3	3
		IR	IM	47							3	4
ORX dst, src	dst ← dst OR src	ER	ER	48	-	*	*	0	-	-	4	3
		ER	IM	49							4	3
POP dst	dst ← @SP SP ← SP + 1	R		50	-	-	-	-	-	-	2	2
		IR		51							2	3
POPX dst	dst ← @SP SP ← SP + 1	ER		D8	-	-	-	-	-	-	3	2
PUSH src	SP ← SP – 1 @SP ← src	R		70	-	-	-	-	-	-	2	2
		IR		71							2	3
		IM		1F 70							3	2
PUSHX src	SP ← SP – 1 @SP ← src	ER		C8	-	-	-	-	-	-	3	2
RCF	C ← 0			CF	0	-	-	-	-	-	1	2
RET	PC ← @SP SP ← SP + 2			AF	-	-	-	-	-	-	1	4
RL dst		R		90	*	*	*	*	-	-	2	2
		IR		91							2	3
RLC dst		R		10	*	*	*	*	-	-	2	2
		IR		11							2	3
RR dst		R		E0	*	*	*	*	-	-	2	2
		IR		E1							2	3

Figure 63 displays the 44-pin Low Profile Quad Flat Package (LQFP) available for the Z8X1621, Z8X2421, Z8X3221, Z8X4821, and Z8X6421 devices.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.30	0.45	0.012	0.018
c	0.09	0.20	0.004	0.008
HD	11.75	12.25	0.463	0.482
D	9.90	10.10	0.390	0.398
HE	11.75	12.25	0.463	0.482
E	9.90	10.10	0.390	0.398
e	0.80 BSC		0.031 BSC	
L	0.45	0.75	0.018	0.030
LE	1.00 REF		0.039 REF	

1. CONTROLLING DIMENSIONS : mm
2. MAX. COPLANARITY : .10mm 0.004"

Figure 63. 44-Lead Low-Profile Quad Flat Package (LQFP)