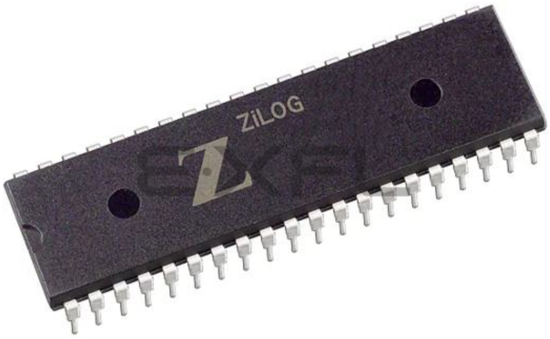

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 29 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.620", 15.75mm) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f1621pm020sg |

**Table 5. Z8 Encore! XP 64K Series Flash Microcontrollers Program Memory Maps (Continued)**

| Program Memory Address (Hex) | Function |
|---|---|
| 0000-0001 | Option Bits |
| 0002-0003 | Reset Vector |
| 0004-0005 | WDT Interrupt Vector |
| 0006-0007 | Illegal Instruction Trap |
| 0008-0037 | Interrupt Vectors* |
| 0038-BFFF | Program Memory |
| **Z8F642x Products** | |
| 0000-0001 | Option Bits |
| 0002-0003 | Reset Vector |
| 0004-0005 | WDT Interrupt Vector |
| 0006-0007 | Illegal Instruction Trap |
| 0008-0037 | Interrupt Vectors* |
| 0038-FFFF | Program Memory |
| *See Table 23 on page 68 for a list of the interrupt vectors. | |

## Data Memory

The Z8 Encore! XP 64K Series Flash Microcontrollers does not use the eZ8 CPU's 64 KB Data Memory address space.

## Information Area

Table 6 on page 22 describes the Z8 Encore! XP 64K Series Flash Microcontrollers Information Area. This 512 byte Information Area is accessed by setting bit 7 of the Page Select Register to 1. When access is enabled, the Information Area is mapped into the Program Memory and overlays the 512 bytes at addresses `FE00H` to `FFFFH`. When the Information Area access is enabled, execution of LDC and LDCI instruction from these Program Memory addresses return the Information Area data rather than the Program Memory data. Reads of these addresses through the On-Chip Debugger also returns the Information Area data. Execution of code from these addresses continues to correctly use the Program Memory. Access to the Information Area is read-only.

**UART1 Control 1**
U0CTL1 (F4BH - Read/Write)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

- D0: Infrared Encoder/Decoder Enable
  0 = Infrared endec is disabled
  1 = Infrared endec is enabled
- D1: Received Data Interrupt Enable
  0 = Received data and errors generate interrupt requests
  1 = Only errors generate interrupt requests. Received data does not.
- D2: Baud Rate Registers Control
  Refer to UART chapter for operation
- D3: Driver Enable Polarity
  0 = DE signal is active High
  1 = DE signal is active Low
- D4: Multiprocessor Bit Transmit
  0 = Send a 0 as the multiprocessor bit
  1 = Send a 1 as the multiprocessor bit
- D5: Multiprocessor Mode [0]
  See Multiprocessor Mode [1] below
- D6: Multiprocessor (9-bit) Enable
  0 = Multiprocessor mode is disabled
  1 = Multiprocessor mode is enabled
- D7: Multiprocessor Mode [1]
  with Multiprocess Mode bit 0:
  00 = Interrupt on all received bytes
  01 = Interrupt only on address bytes
  10 = Interrupt on address match and following data
  11 = Interrupt on data following an address match

**UART1 Status 1**
U0STAT1 (F4CH - Read Only)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

- D0: Mulitprocessor Receive
  Returns value of last multiprocessor bit
- D1: New Frame
  0 = Current byte is not start of frame
  1 = Current byte is start of new frame
- D7–D2: Reserved

**UART1 Address Compare**
U0ADDR (F4DH - Read/Write)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

- D7–D0: UART1 Address Compare [7:0]

**UART1 Baud Rate Generator High Byte**
U0BRH (F4EH - Read/Write)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

- D7–D0: UART1 Baud Rate divisor [15:8]

**UART1 Baud Rate Generator Low Byte**
U1BRL (F4FH - Read/Write)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

- D7–D0: UART1 Baud Rate divisor [7:0]

**I²C Data**
I2CDATA (F50H - Read/Write)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|

- D7–D0: I2C data [7:0]

If interrupts are enabled, following completion of the Stop Mode Recovery the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address.

### WDT Reset in Normal Operation

If configured to generate a Reset when a time-out occurs, the Watchdog Timer forces the device into the Reset state. The `WDT` status bit in the Watchdog Timer Control register is set to 1. For more information on Reset, see Reset and Stop Mode Recovery on page 47.

### WDT Reset in STOP Mode

If enabled in STOP mode and configured to generate a Reset when a time-out occurs and the device is in STOP mode, the Watchdog Timer initiates a Stop Mode Recovery. Both the `WDT` status bit and the `STOP` bit in the Watchdog Timer Control register are set to 1 following WDT time-out in STOP mode. Default operation is for the WDT and its RC oscillator to be enabled during STOP mode.

### WDT RC Disable in STOP Mode

To minimize power consumption in STOP Mode, the WDT and its RC oscillator can be disabled in STOP mode. The following sequence configures the WDT to be disabled when the 64K Series devices enter STOP Mode following execution of a STOP instruction:

1. Write `55H` to the Watchdog Timer Control register (WDTCTL).
2. Write `AAH` to the Watchdog Timer Control register (WDTCTL).
3. Write `81H` to the Watchdog Timer Control register (WDTCTL) to configure the WDT and its oscillator to be disabled during STOP Mode. Alternatively, write `00H` to the Watchdog Timer Control register (WDTCTL) as the third step in this sequence to reconfigure the WDT and its oscillator to be enabled during STOP mode.

This sequence only affects WDT operation in STOP mode.

## Watchdog Timer Reload Unlock Sequence

Writing the unlock sequence to the Watchdog Timer (WDTCTL) Control register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers. Follow the steps below to unlock the Watchdog Timer Reload Byte registers (WDTU, WDTH, and WDTL) for write access.

1. Write `55H` to the Watchdog Timer Control register (WDTCTL).
2. Write `AAH` to the Watchdog Timer Control register (WDTCTL).
3. Write the Watchdog Timer Reload Upper Byte register (WDTU).
4. Write the Watchdog Timer Reload High Byte register (WDTH).

5. Write the Watchdog Timer Reload Low Byte register (WDTL).

All steps of the Watchdog Timer Reload Unlock sequence must be written in the order just listed. There must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur, unless the sequence is restarted. The value in the Watchdog Timer Reload registers is loaded into the counter when the Watchdog Timer is first enabled and every time a WDT instruction is executed.

## Watchdog Timer Control Register Definitions

### Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) register (Table 48) is a Read-Only register that indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event, and indicates a Watchdog Timer time-out. Reading this register resets the upper four bits to 0.

Writing the 55H, AAH unlock sequence to the Watchdog Timer Control (WDTCTL) register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers.

**Table 48. Watchdog Timer Control Register (WDTCTL)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | POR | STOP | WDT | EXT | Reserved | | | SM |
| RESET | See descriptions below | | | 0 | | | | |
| R/W | R | | | | | | | |
| ADDR | FF0H | | | | | | | |

| Reset or Stop Mode Recovery Event | POR | STOP | WDT | EXT |
|---|---|---|---|---|
| Power-On Reset | 1 | 0 | 0 | 0 |
| Reset using $\overline{\text{RESET}}$ pin assertion | 0 | 0 | 0 | 1 |
| Reset using Watchdog Timer time-out | 0 | 0 | 1 | 0 |
| Reset using the On-Chip Debugger (OCDCTL[1] set to 1) | 1 | 0 | 0 | 0 |
| Reset from STOP Mode using DBG Pin driven Low | 1 | 0 | 0 | 0 |
| Stop Mode Recovery using GPIO pin transition | 0 | 1 | 0 | 0 |
| Stop Mode Recovery using Watchdog Timer time-out | 0 | 1 | 1 | 0 |

POR—Power-On Reset Indicator
If this bit is set to 1, a Power-On Reset event occurred. This bit is reset to 0 if a WDT time-out or Stop Mode Recovery occurs. This bit is also reset to 0 when the register is read.

STOP—Stop Mode Recovery Indicator
If this bit is set to 1, a Stop Mode Recovery occurred. If the `STOP` and `WDT` bits are both set to 1, the Stop Mode Recovery occurred due to a WDT time-out. If the `STOP` bit is 1 and the `WDT` bit is 0, the Stop Mode Recovery was not caused by a WDT time-out. This bit is reset by a Power-On Reset or a WDT time-out that occurred while not in STOP mode. Reading this register also resets this bit.

WDT—Watchdog Timer Time-Out Indicator
If this bit is set to 1, a WDT time-out occurred. A Power-On Reset resets this pin. A Stop Mode Recovery from a change in an input pin also resets this bit. Reading this register resets this bit.

EXT—External Reset Indicator
If this bit is set to 1, a Reset initiated by the external $\overline{\text{RESET}}$ pin occurred. A Power-On Reset or a Stop Mode Recovery from a change in an input pin resets this bit. Reading this register resets this bit.

Reserved
These bits are reserved and must be 0.

SM—STOP Mode Configuration Indicator
0 = Watchdog Timer and its internal RC oscillator will continue to operate in STOP Mode.
1 = Watchdog Timer and its internal RC oscillator will be disabled in STOP Mode.

## Watchdog Timer Reload Upper, High and Low Byte Registers

The Watchdog Timer Reload Upper, High and Low Byte (WDTU, WDTH, WDTL) registers (see Table 49 on page 102 through Table 51 on page 102) form the 24-bit reload value that is loaded into the Watchdog Timer when a WDT instruction executes. The 24-bit reload value is {WDTU[7:0], WDTH[7:0], WDTL[7:0]}. Writing to these registers sets the desired Reload Value. Reading from these registers returns the current Watchdog Timer count value.

The Master and Slave are each capable of exchanging a character of data during a sequence of NUMBITS clock cycles (see NUMBITS field in the SPI Mode Register on page 140). In both Master and Slave SPI devices, data is shifted on one edge of the SCK and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI phase and polarity control.

### Slave Select

The active Low Slave Select ($\overline{\text{SS}}$) input signal selects a Slave SPI device. $\overline{\text{SS}}$ must be Low prior to all data communication to and from the Slave device. $\overline{\text{SS}}$ must stay Low for the full duration of each character transferred. The $\overline{\text{SS}}$ signal may stay Low during the transfer of multiple characters or may deassert between each character.

When the SPI is configured as the only Master in an SPI system, the $\overline{\text{SS}}$ pin can be set as either an input or an output. For communication between the Z8F642x family Z8R642x family device's SPI Master and external Slave devices, the $\overline{\text{SS}}$ signal, as an output, can assert the $\overline{\text{SS}}$ input pin on one of the Slave devices. Other GPIO output pins can also be employed to select external SPI Slave devices.

When the SPI is configured as one Master in a multi-master SPI system, the $\overline{\text{SS}}$ pin must be set as an input. The $\overline{\text{SS}}$ input signal on the Master must be High. If the $\overline{\text{SS}}$ signal goes Low (indicating another Master is driving the SPI bus), a Collision error Flag is set in the SPI Status register.

## SPI Clock Phase and Polarity Control

The SPI supports four combinations of serial clock phase and polarity using two bits in the SPI Control register. The clock polarity bit, `CLKPOL`, selects an active high or active Low clock and has no effect on the transfer format. Table 62 lists the SPI Clock Phase and Polarity Operation parameters. The clock phase bit, `PHASE`, selects one of two fundamentally different transfer formats. For proper data transmission, the clock phase and polarity must be identical for the SPI Master and the SPI Slave. The Master always places data on the MOSI line a half-cycle before the receive clock edge (SCK signal), in order for the Slave to latch the data.

**Table 62. SPI Clock Phase (PHASE) and Clock Polarity (CLKPOL) Operation**

| PHASE | CLKPOL | SCK Transmit Edge | SCK Receive Edge | SCK Idle State |
|---|---|---|---|---|
| 0 | 0 | Falling | Rising | Low |
| 0 | 1 | Rising | Falling | High |
| 1 | 0 | Rising | Falling | Low |
| 1 | 1 | Falling | Rising | High |

## Configuring DMA0 and DMA1 for Data Transfer

Follow the steps below to configure and enable DMA0 or DMA1:

1. Write to the DMA*x* I/O Address register to set the Register File address identifying the on-chip peripheral control register. The upper nibble of the 12-bit address for on-chip peripheral control registers is always `FH`. The full address is {FH, DMA*x*_IO[7:0]}.
2. Determine the 12-bit Start and End Register File addresses. The 12-bit Start Address is given by {DMA*x*_H[3:0], DMA_START[7:0]}. The 12-bit End Address is given by {DMA*x*_H[7:4], DMA_END[7:0]}.
3. Write the Start and End Register File address high nibbles to the DMA*x* End/Start Address High Nibble register.
4. Write the lower byte of the Start Address to the DMA*x* Start/Current Address register.
5. Write the lower byte of the End Address to the DMA*x* End Address register.
6. Write to the DMA*x* Control register to complete the following:
   – Select loop or single-pass mode operation
   – Select the data transfer direction (either from the Register File RAM to the on-chip peripheral control register; or from the on-chip peripheral control register to the Register File RAM)
   – Enable the DMA*x* interrupt request, if desired
   – Select Word or Byte mode
   – Select the DMA*x* request trigger
   – Enable the DMA*x* channel

## DMA_ADC Operation

DMA_ADC transfers data from the ADC to the Register File. The sequence of operations in a DMA_ADC data transfer is:

1. ADC completes conversion on the current ADC input channel and signals the DMA controller that two-bytes of ADC data are ready for transfer.
2. DMA_ADC requests control of the system bus (address and data) from the eZ8 CPU.
3. After the eZ8 CPU acknowledges the bus request, DMA_ADC transfers the two-byte ADC output value to the Register File and then returns system bus control back to the eZ8 CPU.
4. If the current ADC Analog Input is the highest numbered input to be converted:
   – DMA_ADC resets the ADC Analog Input number to 0 and initiates data conversion on ADC Analog Input 0.
   – If configured to generate an interrupt, DMA_ADC sends an interrupt request to the Interrupt Controller

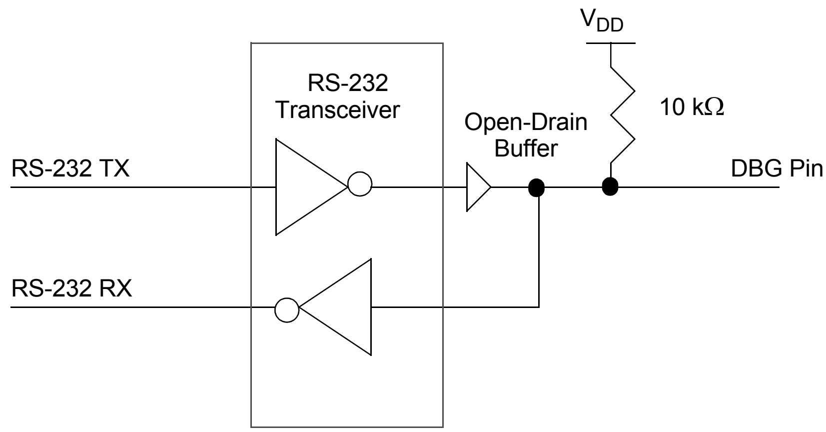



**Figure 38. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (2)**

## DEBUG Mode

The operating characteristics of the 64K Series devices in DEBUG mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions.
- The system clock operates unless in STOP mode.
- All enabled on-chip peripherals operate unless in STOP mode.
- Automatically exits HALT mode.
- Constantly refreshes the Watchdog Timer, if enabled.

### Entering DEBUG Mode

The device enters DEBUG mode following any of the following operations:

- Writing the `DBGMODE` bit in the OCD Control Register to 1 using the OCD interface.
- eZ8 CPU execution of a BRK (Breakpoint) instruction (when enabled).
- If the DBG pin is Low when the device exits Reset, the On-Chip Debugger automatically puts the device into DEBUG mode.

### Exiting DEBUG Mode

The device exits DEBUG mode following any of the following operations:

- Clearing the `DBGMODE` bit in the OCD Control Register to 0.
- Power-On Reset
- Voltage Brownout reset

# Electrical Characteristics

## Absolute Maximum Ratings

Stresses greater than those listed in Table 105 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs must be tied to one of the supply voltages ($V_{DD}$ or $V_{SS}$).

**Table 105. Absolute Maximum Ratings**

| Parameter | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|
| Ambient temperature under bias | -40 | +125 | C | |
| Storage temperature | -65 | +150 | C | |
| Voltage on any pin with respect to $V_{SS}$ | -0.3 | +5.5 | V | 1 |
| Voltage on $V_{DD}$ pin with respect to $V_{SS}$ | -0.3 | +3.6 | V | |
| Maximum current on input and/or inactive output pin | -5 | +5 | µA | |
| Maximum output current from active output pin | -25 | +25 | mA | |
| **80-Pin QFP Maximum Ratings at –40 °C to 70 °C** | | | | |
| Total power dissipation | | 550 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 150 | mA | |
| **80-Pin QFP Maximum Ratings at 70 °C to 125 °C** | | | | |
| Total power dissipation | | 200 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 56 | mA | |
| **68-Pin PLCC Maximum Ratings at –40 °C to 70 °C** | | | | |
| Total power dissipation | | 1000 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 275 | mA | |
| **68-Pin PLCC Maximum Ratings at 70 °C to 125 °C** | | | | |
| Total power dissipation | | 500 | mW | |

Figure 45 displays the maximum HALT mode current consumption across the full operating temperature range of the device and versus the system clock frequency. All GPIO pins are configured as outputs and driven High.

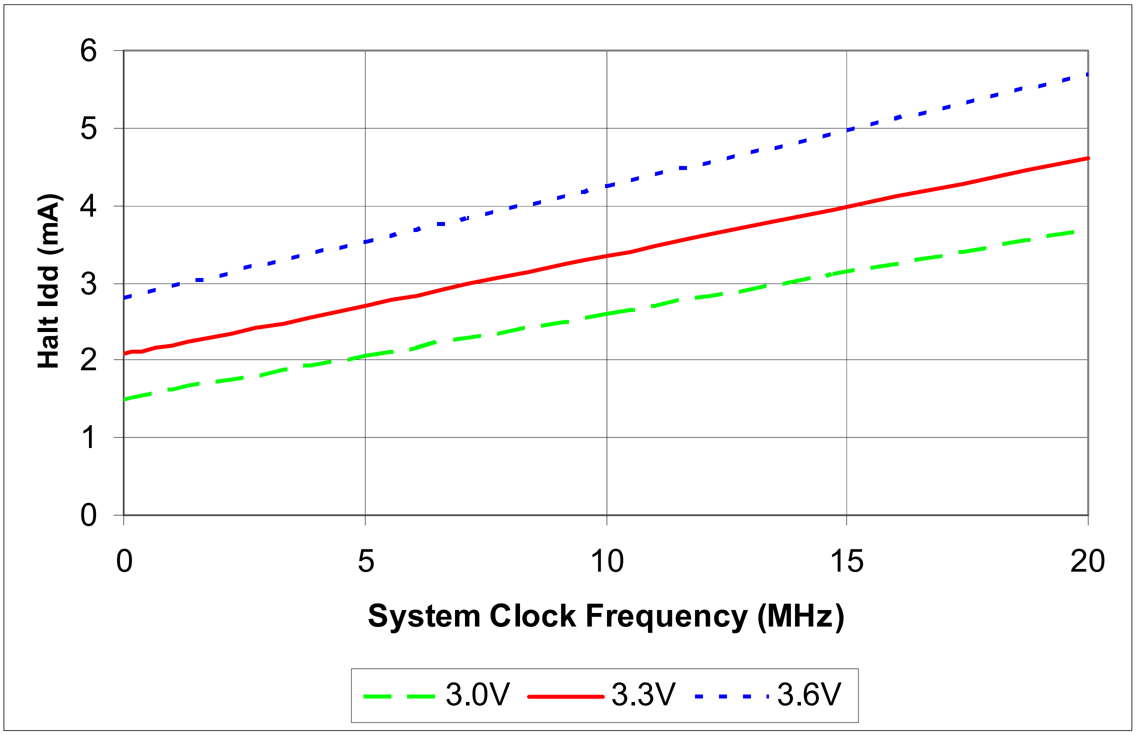



**Figure 46. Maximum HALT Mode Icc Versus System Clock Frequency**

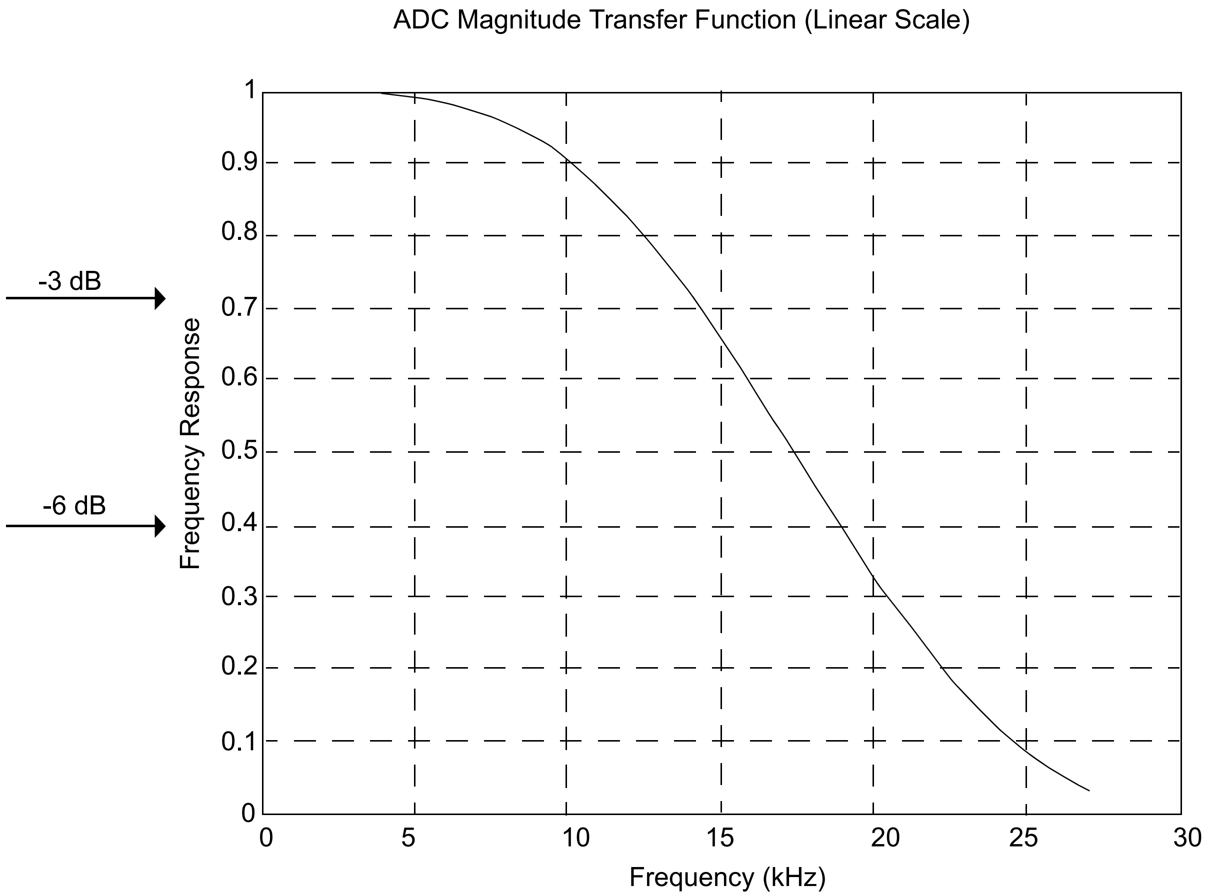



**Figure 49. Analog-to-Digital Converter Frequency Response**

## General-Purpose I/O Port Input Data Sample Timing

Figure 50 displays timing of the GPIO Port input sampling. Table 114 lists the GPIO port input timing.

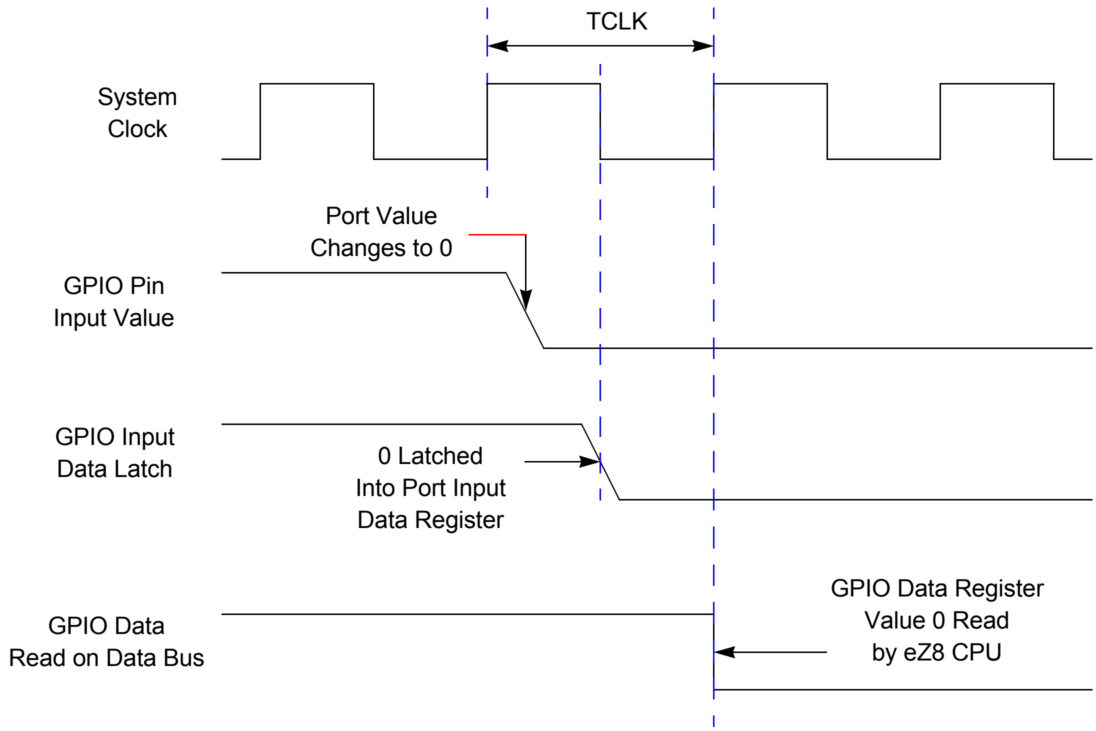



**Figure 50. Port Input Sample Timing**

**Table 114. GPIO Port Input Timing**

| | | Delay (ns) | |
|---|---|---|---|
| **Parameter** | **Abbreviation** | **Min** | **Max** |
| $T_{S\_PORT}$ | Port Input Transition to XIN Fall Setup Time (Not pictured) | 5 | – |
| $T_{H\_PORT}$ | XIN Fall to Port Input Transition Hold Time (Not pictured) | 6 | – |
| $T_{SMR}$ | GPIO Port Pin Pulse Width to Insure Stop Mode Recovery (for GPIO Port Pins enabled as SMR sources) | 1 µs | |

## SPI Master Mode Timing

Figure 53 and Table 117 provide timing information for SPI Master mode pins. Timing is shown with SCK rising edge used to source MOSI output data, SCK falling edge used to sample MISO input data. Timing on the SS output pin(s) is controlled by software.

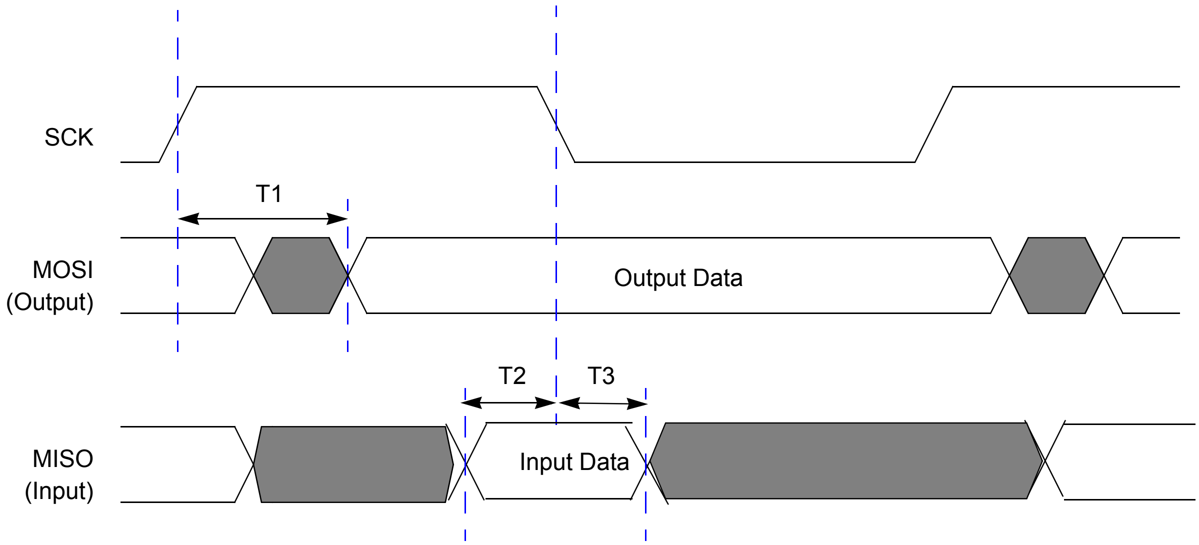



**Figure 53. SPI Master Mode Timing**

**Table 117. SPI Master Mode Timing**

| | | Delay (ns) | |
|---|---|---|---|
| **Parameter** | **Abbreviation** | **Min** | **Max** |
| **SPI Master** | | | |
| $T_1$ | SCK Rise to MOSI output Valid Delay | -5 | +5 |
| $T_2$ | MISO input to SCK (receive edge) Setup Time | 20 | |
| $T_3$ | MISO input to SCK (receive edge) Hold Time | 0 | |

### Table 128. CPU Control Instructions

| Mnemonic | Operands | Instruction |
|---|---|---|
| STOP | — | STOP Mode |
| WDT | — | Watchdog Timer Refresh |

### Table 129. Load Instructions

| Mnemonic | Operands | Instruction |
|---|---|---|
| CLR | dst | Clear |
| LD | dst, src | Load |
| LDC | dst, src | Load Constant to/from Program Memory |
| LDCI | dst, src | Load Constant to/from Program Memory and Auto-Increment Addresses |
| LDE | dst, src | Load External Data to/from Data Memory |
| LDEI | dst, src | Load External Data to/from Data Memory and Auto-Increment Addresses |
| LDWX | dst, src | Load Word using Extended Addressing |
| LDX | dst, src | Load using Extended Addressing |
| LEA | dst, X(src) | Load Effective Address |
| POP | dst | Pop |
| POPX | dst | Pop using Extended Addressing |
| PUSH | src | Push |
| PUSHX | src | Push using Extended Addressing |

### Table 130. Logical Instructions

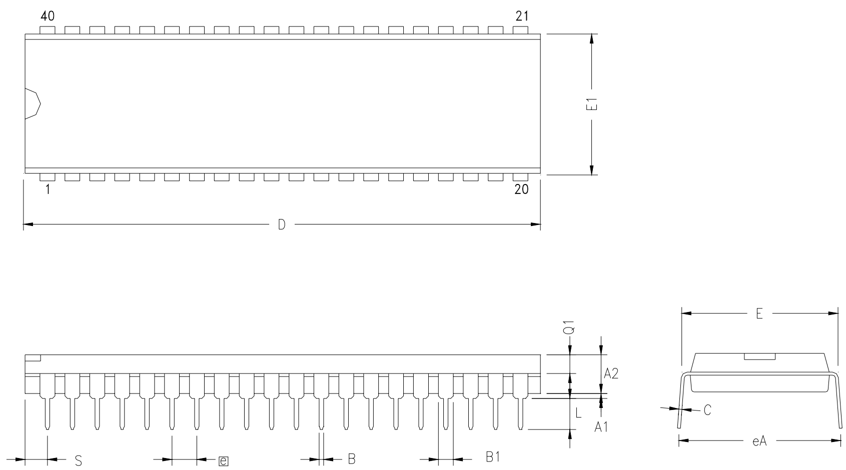
| Mnemonic | Operands | Instruction |
|---|---|---|
| AND | dst, src | Logical AND |
| ANDX | dst, src | Logical AND using Extended Addressing |
| COM | dst | Complement |
| OR | dst, src | Logical OR |
| ORX | dst, src | Logical OR using Extended Addressing |

**Table 133. eZ8 CPU Instruction Summary (Continued)**

| Assembly Mnemonic | Symbolic Operation | Address Mode dst | Address Mode src | Opcode(s) (Hex) | Flags C | Z | S | V | D | H | Fetch Cycles | Instr. Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SWAP dst | dst[7:4] ↔ dst[3:0] | R | | F0 | X | * | * | X | - | - | 2 | 2 |
| | | IR | | F1 | | | | | | | 2 | 3 |
| TCM dst, src | (NOT dst) AND src | r | r | 62 | - | * | * | 0 | - | - | 2 | 3 |
| | | r | Ir | 63 | | | | | | | 2 | 4 |
| | | R | R | 64 | | | | | | | 3 | 3 |
| | | R | IR | 65 | | | | | | | 3 | 4 |
| | | R | IM | 66 | | | | | | | 3 | 3 |
| | | IR | IM | 67 | | | | | | | 3 | 4 |
| TCMX dst, src | (NOT dst) AND src | ER | ER | 68 | - | * | * | 0 | - | - | 4 | 3 |
| | | ER | IM | 69 | | | | | | | 4 | 3 |
| TM dst, src | dst AND src | r | r | 72 | - | * | * | 0 | - | - | 2 | 3 |
| | | r | Ir | 73 | | | | | | | 2 | 4 |
| | | R | R | 74 | | | | | | | 3 | 3 |
| | | R | IR | 75 | | | | | | | 3 | 4 |
| | | R | IM | 76 | | | | | | | 3 | 3 |
| | | IR | IM | 77 | | | | | | | 3 | 4 |
| TMX dst, src | dst AND src | ER | ER | 78 | - | * | * | 0 | - | - | 4 | 3 |
| | | ER | IM | 79 | | | | | | | 4 | 3 |
| TRAP Vector | SP ← SP – 2<br>@SP ← PC<br>SP ← SP – 1<br>@SP ← FLAGS<br>PC ← @Vector | | Vector | F2 | - | - | - | - | - | - | 2 | 6 |
| WDT | | | | 5F | - | - | - | - | - | - | 1 | 2 |

# Packaging

Figure 62 displays the 40-pin Plastic Dual-inline Package (PDIP) available for the Z8X1601, Z8X2401, Z8X3201, Z8X4801, and Z8X6401 devices.




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.51 | 1.02 | .020 | .040 |
| A2 | 3.18 | 3.94 | .125 | .155 |
| B | 0.38 | 0.53 | .015 | .021 |
| B1 | 1.02 | 1.52 | .040 | .060 |
| C | 0.23 | 0.38 | .009 | .015 |
| D | 52.07 | 52.58 | 2.050 | 2.070 |
| E | 15.24 | 15.75 | .600 | .620 |
| E1 | 13.59 | 14.22 | .535 | .560 |
| e | 2.54 TYP | | .100 TYP | |
| eA | 15.49 | 16.76 | .610 | .660 |
| L | 3.05 | 3.81 | .120 | .150 |
| Q1 | 1.40 | 1.91 | .055 | .075 |
| S | 1.52 | 2.29 | .060 | .090 |

CONTROLLING DIMENSIONS : INCH

**Figure 62. 40-Lead Plastic Dual-Inline Package (PDIP)**

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | $I^2C$ | SPI | UARTs with IrDA | Description |
|---|---|---|---|---|---|---|---|---|---|---|
| **Z8F322x with 32 KB Flash, 10-Bit Analog-to-Digital Converter** | | | | | | | | | | |
| Standard Temperature: 0 °C to 70 °C | | | | | | | | | | |
| Z8F3221PM020SC | 32 KB | 2 KB | 29 | 23 | 3 | 8 | 1 | 1 | 2 | PDIP 40-pin package |
| Z8F3221AN020SC | 32 KB | 2 KB | 31 | 23 | 3 | 8 | 1 | 1 | 2 | LQFP 44-pin package |
| Z8F3221VN020SC | 32 KB | 2 KB | 31 | 23 | 3 | 8 | 1 | 1 | 2 | PLCC 44-pin package |
| Z8F3222AR020SC | 32 KB | 2 KB | 46 | 24 | 4 | 12 | 1 | 1 | 2 | LQFP 64-pin package |
| Z8F3222VS020SC | 32 KB | 2 KB | 46 | 24 | 4 | 12 | 1 | 1 | 2 | PLCC 68-pin package |
| Extended Temperature: –40 °C to 105 °C | | | | | | | | | | |
| Z8F3221PM020EC | 32 KB | 2 KB | 29 | 23 | 3 | 8 | 1 | 1 | 2 | PDIP 40-pin package |
| Z8F3221AN020EC | 32 KB | 2 KB | 31 | 23 | 3 | 8 | 1 | 1 | 2 | LQFP 44-pin package |
| Z8F3221VN020EC | 32 KB | 2 KB | 31 | 23 | 3 | 8 | 1 | 1 | 2 | PLCC 44-pin package |
| Z8F3222AR020EC | 32 KB | 2 KB | 46 | 24 | 4 | 12 | 1 | 1 | 2 | LQFP 64-pin package |
| Z8F3222VS020EC | 32 KB | 2 KB | 46 | 24 | 4 | 12 | 1 | 1 | 2 | PLCC 68-pin package |
| Automotive/Industrial Temperature: –40 °C to 125°C | | | | | | | | | | |
| Z8F3221PM020AC | 32 KB | 2 KB | 29 | 23 | 3 | 8 | 1 | 1 | 2 | PDIP 40-pin package |
| Z8F3221AN020AC | 32 KB | 2 KB | 31 | 23 | 3 | 8 | 1 | 1 | 2 | LQFP 44-pin package |
| Z8F3221VN020AC | 32 KB | 2 KB | 31 | 23 | 3 | 8 | 1 | 1 | 2 | PLCC 44-pin package |
| Z8F3222AR020AC | 32 KB | 2 KB | 46 | 24 | 4 | 12 | 1 | 1 | 2 | LQFP 64-pin package |
| Z8F3222VS020AC | 32 KB | 2 KB | 46 | 24 | 4 | 12 | 1 | 1 | 2 | PLCC 68-pin package |

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