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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Detail	s
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Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	46
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f1622vs020ec00tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Braces

The curly braces, { }, indicate a single register or bus created by concatenating some combination of smaller registers, buses, or individual bits.

• Example: The 12-bit register address {0H, RP[7:4], R1[3:0]} is composed of a 4-bit hexadecimal value (0H) and two 4-bit register values taken from the Register Pointer (RP) and Working Register R1. 0H is the most-significant nibble (4-bit value) of the 12-bit register, and R1[3:0] is the least significant nibble of the 12-bit register.

Parentheses

The parentheses, (), indicate an indirect register address lookup.

• Example: (R1) is the memory location referenced by the address contained in the Working Register R1.

Parentheses/Bracket Combinations

The parentheses, (), indicate an indirect register address lookup and the square brackets, [], indicate a register or bus.

• Example: Assume PC[15:0] contains the value 1234h. (PC[15:0]) then refers to the contents of the memory location at address 1234h.

Use of the Words Set, Reset and Clear

The word *set* implies that a register bit or a condition contains a logical 1. The words reset or *clear* imply that a register bit or a condition contains a logical 0. When either of these terms is followed by a number, the word *logical* may not be included; however, it is implied.

Notation for Bits and Similar Registers

A field of bits within a register is designated as: Register[*n*:*n*].

• Example: ADDR[15:0] refers to bits 15 through bit 0 of the Address.

Use of the Terms LSB, MSB, Isb, and msb

In this document, the terms *LSB* and *MSB*, when appearing in upper case, mean *least* significant byte and most significant byte, respectively. The lowercase forms, *lsb* and *msb*, mean *least* significant bit and most significant bit, respectively.

Use of Initial Uppercase Letters

Initial uppercase letters designate settings and conditions in general text.

- Example 1: The receiver forces the SCL line to Low.
- Example 2: The Master can generate a Stop condition to abort the transfer.



Block Diagram

Figure 1 displays the block diagram of the architecture of the Z8 Encore! XP 64K Series Flash Microcontrollers.





CPU and Peripheral Overview

eZ8[™] CPU Features

The latest 8-bit eZ8 CPU meets the continuing demand for faster and more code-efficient microcontrollers. The eZ8 CPU executes a superset of the original $Z8^{\mathbb{R}}$ instruction set.



Address Space

Overview

The eZ8[™] CPU can access three distinct address spaces:

- The Register File contains addresses for the general-purpose registers and the eZ8 CPU, peripheral, and general-purpose I/O port control registers.
- The Program Memory contains addresses for all memory locations having executable code and/or data.
- The Data Memory consists of the addresses for all memory locations that hold only data.

These three address spaces are covered briefly in the following subsections. For more information on eZ8 CPU and its address space, refer to $eZ8^{TM}$ CPU Core User Manual (UM0128) available for download at www.zilog.com.

Register File

The Register File address space in the 64K Series is 4 KB (4096 bytes). The Register File is composed of two sections—control registers and general-purpose registers. When instructions are executed, registers are read from when defined as sources and written to when defined as destinations. The architecture of the eZ8 CPU allows all general-purpose registers to function as accumulators, address pointers, index registers, stack areas, or scratch pad memory.

The upper 256 bytes of the 4 KB Register File address space are reserved for control of the eZ8 CPU, the on-chip peripherals, and the I/O ports. These registers are located at addresses from F00H to FFFH. Some of the addresses within the 256-byte control register section are reserved (unavailable). Reading from an reserved Register File addresses returns an undefined value. Writing to reserved Register File addresses is not recommended and can produce unpredictable results.

The on-chip RAM always begins at address 000H in the Register File address space. The 64K Series provide 2 KB to 4 KB of on-chip RAM depending upon the device. Reading from Register File addresses outside the available RAM addresses (and not within the control register address space) returns an undefined value. Writing to these Register File addresses produces no effect. To determine the amount of RAM available for the specific 64K Series device, see Part Selection Guide on page 2.

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
F61	SPI Control	SPICTL	00	137
F62	SPI Status	SPISTAT	01	139
F63	SPI Mode	SPIMODE	00	140
F64	SPI Diagnostic State	SPIDST	00	141
F65	Reserved	_	XX	
F66	SPI Baud Rate High Byte	SPIBRH	FF	142
F67	SPI Baud Rate Low Byte	SPIBRL	FF	142
F68-F6F	Reserved		XX	
Analog-to-Digit	al Converter			
F70	ADC Control	ADCCTL	20	179
F71	Reserved		XX	
F72	ADC Data High Byte	ADCD_H	XX	180
F73	ADC Data Low Bits	ADCD_L	XX	180
F74-FAF	Reserved		XX	
DMA 0				
FB0	DMA0 Control	DMA0CTL	00	167
FB1	DMA0 I/O Address	DMA0IO	XX	169
FB2	DMA0 End/Start Address High Nibble	DMA0H	XX	169
FB3	DMA0 Start Address Low Byte	DMA0START	XX	170
FB4	DMA0 End Address Low Byte	DMA0END	XX	170
DMA 1				
FB8	DMA1 Control	DMA1CTL	00	167
FB9	DMA1 I/O Address	DMA1IO	XX	169
FBA	DMA1 End/Start Address High Nibble	DMA1H	XX	169
FBB	DMA1 Start Address Low Byte	DMA1START	XX	170
FBC	DMA1 End Address Low Byte	DMA1END	XX	170
DMA ADC				
FBD	DMA_ADC Address	DMAA_ADDR	XX	171
FBE	DMA_ADC Control	DMAACTL	00	172
FBF	DMA_ADC Status	DMAASTAT	00	173
Interrupt Control	oller			
FC0	Interrupt Request 0	IRQ0	00	71
FC1	IRQ0 Enable High Bit	IRQ0ENH	00	74
FC2	IRQ0 Enable Low Bit	IRQ0ENL	00	74
FC3	Interrupt Request 1	IRQ1	00	72
FC4	IRQ1 Enable High Bit	IRQ1ENH	00	75
FC5	IRQ1 Enable Low Bit	IRQ1ENL	00	75
FC6	Interrupt Request 2	IRQ2	00	73
FC7	IRQ2 Enable High Bit	IRQ2ENH	00	76
FC8	IRQ2 Enable Low Bit	IRQ2ENL	00	76
FC9-FCC	Reserved	_	XX	

Table 7. Z8 Encore! XP 64K Series Flash Microcontrollers Register File Address Map (Continued)



IRQ0 Enable Low Bit IRQ0ENL (FC2H - Read/Write)



Interrupt Request 1

IRQ1 (FC3H - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0 Port A or D Pin Interrupt Request

0 = IRQ from corresponding pin [7:0] is not pending 1 = IRQ from corresponding pin [7:0] is awaiting service

IRQ1 Enable High Bit

IRQ1ENH (FC4H - Read/Write) D7 D6 D5 D4 D3 D2 D1 D0

- Port A or D Pin IRQ Enable High Bit

IRQ1 Enable Low Bit IRQ1ENL (FC5H - Read/Write) D7 D6 D5 D4 D3 D2 D1 D0

- Port A or D Pin IRQ Enable Low Bit

Interrupt Request 2 IRQ2 (FC6H - Read/V D7D6D5D4D3D2D1D0	Vrite)
	Port C Pin Interrupt Request 0 = IRQ from corresponding pin [3:0] is not pending 1 = IRQ from corresponding pin [3:0] is awaiting service
	DMA Interrupt Request
	UART 1 Transmitter Interrupt
	UART 1 Receiver Interrupt Request
	Timer 3 Interrupt Request
	For all of the above peripherals: 0 = Peripheral IRQ is not pending 1 = Peripheral IRQ is awaiting

service

IRQ2 Enable High Bit IRQ2ENH (FC7H - Read/Write)

D7	D6	D:	5 D	4 D.	3 D2	D1	D0	,
T	T	T	-				_	Port C Pin IRQ Enable High Bit
			ļ					DMA IRQ Enable High Bit
								UART 1 Transmitter IRQ Enable
								UART 1 Receiver IRQ Enable High
								Timer 3 IRQ Enable High Bit

IRQ2 Enable Low Bit

IRQ2ENL (FC8H - Read/Write) D7 D6 D5 D4 D3 D2 D1 D0

T	Port C Pin IRQ Enable Low Bit
	DMA IRQ Enable Low Bit
	UART 1 Transmitter IRQ Enable
	UART 1 Receiver IRQ Enable Low
	Timer 3 IRQ Enable Low Bit

Interrupt Edge Select IRQES (FCDH - Read/Write) D7 D6 D5 D4 D3 D2 D1 D0

Port A or D Interrupt Edge Select 0 = Falling edge 1 = Rising edge

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- Select either the rising edge or falling edge of the Timer Input signal for the count. This also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function does not have to be enabled
- 2. Write to the Timer High and Low Byte registers to set the starting count value. This only affects the first pass in COUNTER mode. After the first timer Reload in COUNTER mode, counting always begins at the reset value of 0001H. Generally, in COUNTER mode the Timer High and Low Byte registers must be written with the value 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. If desired, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 7. Write to the Timer Control 1 register to enable the timer.

In COUNTER mode, the number of Timer Input transitions since the timer start is given by the following equation:

COUNTER Mode Timer Input Transitions = Current Count Value – Start Value

PWM Mode

In PWM mode, the timer outputs a Pulse-Width Modulator (PWM) output signal through a GPIO Port pin. The timer input is the system clock. The timer first counts up to the 16bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control 1 register is set to 1, the Timer Output signal begins as a High (1) and then transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the Reload value and is reset to 0001H.

If the TPOL bit in the Timer Control 1 register is set to 0, the Timer Output signal begins as a Low (0) and then transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the Reload value and is reset to 0001H.







Operation

Data Format

The UART always transmits and receives data in an 8-bit data format, least-significant bit first. An even or odd parity bit can be optionally added to the data stream. Each character begins with an active Low Start bit and ends with either 1 or 2 active High Stop bits. Figure 14 and Figure 15 on page 105 displays the asynchronous data format employed by the UART without parity and with parity, respectively.

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- 1 = Infrared Encoder/Decoder is enabled. The UART transmits and receives data through the Infrared Encoder/Decoder.

UART Address Compare Register

The UART Address Compare register (Table 58) stores the multi-node network address of the UART. When the MPMD[1] bit of UART Control Register 0 is set, all incoming address bytes are compared to the value stored in the Address Compare register. Receive interrupts and RDA assertions only occur in the event of a match.

Table 58. UART Address Compare Register (UxADDR)

BITS	7	6	5	4	3	2	1	0
FIELD	COMP_ADDR							
RESET	0							
R/W	R/W							
ADDR		F45H and F4DH						

COMP_ADDR—Compare Address

This 8-bit value is compared to the incoming address bytes.

UART Baud Rate High and Low Byte Registers

The UART Baud Rate High and Low Byte registers (see Table 59 and Table 60 on page 121) combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART. To configure the Baud Rate Generator as a timer with interrupt on time-out, complete the following procedure:

- 1. Disable the UART by clearing the REN and TEN bits in the UART Control 0 register to 0.
- 2. Load the desired 16-bit count value into the UART Baud Rate High and Low Byte registers.
- 3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BRGCTL bit in the UART Control 1 register to 1.

When configured as a general purpose timer, the UART BRG interrupt interval is calculated using the following equation:

UART BRG Interrupt Interval(s) = System Clock Period (s) × BRG[15:0]

5.5296 MHz System Clock



Table 61. UART Baud Rates (Continued)

1.20	868	1.20	0.01	1.20	576	1.20	0.00
0.60	1736	0.60	0.01	0.60	1152	0.60	0.00
0.30	3472	0.30	0.01	0.30	2304	0.30	0.00

10.0 MHz System Clock

Desired Rate	BRG Divisor	Actual Rate	Error
(kHz)	(Decimal)	(kHz)	(%)
1250.0	N/A	N/A	N/A
625.0	1	625.0	0.00
250.0	3	208.33	-16.67
115.2	5	125.0	8.51
57.6	11	56.8	-1.36
38.4	16	39.1	1.73
19.2	33	18.9	0.16
9.60	65	9.62	0.16
4.80	130	4.81	0.16
2.40	260	2.40	-0.03
1.20	521	1.20	-0.03
0.60	1042	0.60	-0.03
0.30	2083	0.30	0.2

Desired Rate	BRG Divisor	Actual Rate	Error
(kHz)	(Decimal)	(kHz)	(%)
1250.0	N/A	N/A	N/A
625.0	N/A	N/A	N/A
250.0	1	345.6	38.24
115.2	3	115.2	0.00
57.6	6	57.6	0.00
38.4	9	38.4	0.00
19.2	18	19.2	0.00
9.60	36	9.60	0.00
4.80	72	4.80	0.00
2.40	144	2.40	0.00
1.20	288	1.20	0.00
0.60	576	0.60	0.00
0.30	1152	0.30	0.00

3.579545 MHz System Clock

Desired Rate	BRG Divisor	Actual Rate	Error	Desired Rate
(kHz)	(Decimal)	(kHz)	(%)	(kHz)
1250.0	N/A	N/A	N/A	1250.0
625.0	N/A	N/A	N/A	625.0
250.0	1	223.72	-10.51	250.0
115.2	2	111.9	-2.90	115.2
57.6	4	55.9	-2.90	57.6
38.4	6	37.3	-2.90	38.4
19.2	12	18.6	-2.90	19.2

1.8432 MHz System Clock

Desired Rate	BRG Divisor	Actual Rate	Error
(kHz)	(Decimal)	(kHz)	(%)
1250.0	N/A	N/A	N/A
625.0	N/A	N/A	N/A
250.0	N/A	N/A	N/A
115.2	1	115.2	0.00
57.6	2	57.6	0.00
38.4	3	38.4	0.00
19.2	6	19.2	0.00

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Infrared Encoder/Decoder

Overview

The 64K Series products contain two fully-functional, high-performance UART to Infrared Encoder/Decoders (Endecs). Each Infrared Endec is integrated with an on-chip UART to allow easy communication between the 64K Series and IrDA Physical Layer Specification, Version 1.3-compliant infrared transceivers. Infrared communication provides secure, reliable, low-cost, point-to-point communication between PCs, PDAs, cell phones, printers, and other infrared enabled devices.

Architecture



Figure 19 displays the architecture of the Infrared Endec.







Figure 23. SPI Configured as a Master in a Single Master, Multiple Slave System



Figure 24. SPI Configured as a Slave

Operation

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (serial clock, transmit, receive and Slave select). The SPI block consists of a transmit/receive shift register, a Baud Rate (clock) Generator and a control unit.





Figure 26. SPI Timing When PHASE is 1

Multi-Master Operation

In a multi-master SPI system, all SCK pins are tied together, all MOSI pins are tied together and all MISO pins are tied together. All SPI pins must then be configured in OPEN-DRAIN mode to prevent bus contention. At any one time, only one SPI device is configured as the Master and all other SPI devices on the bus are configured as Slaves. The Master enables a single Slave by asserting the \overline{SS} pin on that Slave only. Then, the single Master drives data out its SCK and MOSI pins to the SCK and MOSI pins on the Slaves (including those which are not enabled). The enabled Slave drives data out its MISO pin to the MISO Master pin.

For a Master device operating in a multi-master system, if the \overline{SS} pin is configured as an input and is driven Low by another Master, the COL bit is set to 1 in the SPI Status Register. The COL bit indicates the occurrence of a multi-master collision (mode fault error condition).

Slave Operation

The SPI block is configured for SLAVE mode operation by setting the SPIEN bit to 1 and the MMEN bit to 0 in the SPICTL register and setting the SSIO bit to 0 in the SPIMODE

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DMA_ADC Address Register

The DMA_ADC Address register (Table 83) points to a block of the Register File to store ADC conversion values as displayed in Table 82. This register contains the seven most-significant bits of the 12-bit Register File addresses. The five least-significant bits are calculated from the ADC Analog Input number (5-bit base address is equal to twice the ADC Analog Input number). The 10-bit ADC conversion data is stored as two bytes with the most significant byte of the ADC data stored at the even numbered Register File address.

Table 82 provides an example of the Register File addresses if the DMA_ADC Address register contains the value 72H.

ADC Analog Input	Register File Address (Hex) ¹
0	720H-721H
1	722H-723H
2	724H-725H
3	726H-727H
4	728H-729H
5	72AH-72BH
6	72CH-72DH
7	72EH-72FH
8	730H-731H
9	732H-733H
10	734H-735H
11	736H-737H

Table 82. DMA_ADC Register File Address Example

¹DMAA_ADDR set to 72H.

Table 83. DMA_ADC Address Register (DMAA_ADDR)

BITS	7	6	5	4	3	2	1	0			
FIELD	DMAA_ADDR										
RESET	X										
R/W	R/W										
ADDR	FBDH										







Figure 34. Analog-to-Digital Converter Block Diagram

The sigma-delta ADC architecture provides alias and image attenuation below the amplitude resolution of the ADC in the frequency range of DC to one-half the ADC clock rate (one-fourth the system clock rate). The ADC provides alias free conversion for frequencies up to one-half the ADC clock rate. Thus the sigma-delta ADC exhibits high noise immunity making it ideal for embedded applications. In addition, monotonicity (no missing codes) is guaranteed by design.

Operation

Automatic Power-Down

If the ADC is idle (no conversions in progress) for 160 consecutive system clock cycles, portions of the ADC are automatically powered-down. From this power-down state, the ADC requires 40 system clock cycles to power-up. The ADC powers up when a conversion is requested using the ADC Control register.



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Debug Command	Command Byte	Enabled when NOT in DEBUG mode?	Disabled by Read Protect Option Bit
Write Program Counter	06H	-	Disabled
Read Program Counter	07H	-	Disabled
Write Register	08H	-	Only writes of the Flash Memory Control registers are allowed. Additionally, only the Mass Erase command is allowed to be written to the Flash Control register.
Read Register	09H	-	Disabled
Write Program Memory	0AH	-	Disabled
Read Program Memory	0BH	-	Disabled
Write Data Memory	0CH	-	Disabled
Read Data Memory	0DH	-	Disabled
Read Program Memory CRC	0EH	-	-
Reserved	0FH	-	-
Step Instruction	10H	-	Disabled
Stuff Instruction	11H	-	Disabled
Execute Instruction	12H	-	Disabled
Reserved	13H - FFH	-	-

Table 101. On-Chip Debugger Commands (Continued)

In the following list of OCD Commands, data and commands sent from the host to the On-Chip Debugger are identified by 'DBG \leftarrow Command/Data'. Data sent from the On-Chip Debugger back to the host is identified by 'DBG \rightarrow Data'

• **Read OCD Revision (00H)**—The Read OCD Revision command determines the version of the On-Chip Debugger. If OCD commands are added, removed, or changed, this revision number changes.

DBG \leftarrow 00H DBG \rightarrow OCDREV[15:8] (Major revision number) DBG \rightarrow OCDREV[7:0] (Minor revision number)

• **Read OCD Status Register (02H)**—The Read OCD Status Register command reads the OCDSTAT register.

```
DBG \leftarrow 02H
DBG \rightarrow OCDSTAT[7:0]
```

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must add no more than 4 pF of stray capacitance to either the $X_{\rm IN}$ or $X_{\rm OUT}$ pins. If oscillation does not occur, reduce the values of capacitors C1 and C2 to decrease loading.



Figure 40. Recommended 20 MHz Crystal Oscillator Configuration

Parameter	Value	Units	Comments
Frequency	20	MHz	
Resonance	Parallel		
Mode	Fundamental		
Series Resistance (R _S)	25	Ω	Maximum
Load Capacitance (CL)	20	pF	Maximum
Shunt Capacitance (C ₀)	7	pF	Maximum
Drive Level	1	mW	Maximum

Table 104. Recommended Crystal Oscillator Specifications (20 MHz Operation)



Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than those listed in Table 105 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs must be tied to one of the supply voltages (V_{DD} or V_{SS}).

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	+125	С	
Storage temperature	-65	+150	С	
Voltage on any pin with respect to V _{SS}	-0.3	+5.5	V	1
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
80-Pin QFP Maximum Ratings at –40 °C to 70 °C				
Total power dissipation		550	mW	
Maximum current into V_{DD} or out of V_{SS}		150	mA	
80-Pin QFP Maximum Ratings at 70 °C to 125 °C				
Total power dissipation		200	mW	
Maximum current into V _{DD} or out of V _{SS}		56	mA	
68-Pin PLCC Maximum Ratings at –40 °C to 70 °C				
Total power dissipation		1000	mW	
Maximum current into V_{DD} or out of V_{SS}		275	mA	
68-Pin PLCC Maximum Ratings at 70 °C to 125 °C				
Total power dissipation		500	mW	

Table 105. Absolute Maximum Ratings



AC Characteristics

The section provides information on the AC characteristics and timing. All AC timing information assumes a standard load of 50 pF on all outputs. Table 113 lists the 64K Series AC characteristics and timing.

Table 113. AC Characteristics

		V _{DD} = 3 T _A = -40 ° (8.0–3.6V C to 125 °C		
Symbol	Parameter	Minimum	Minimum Maximum		Conditions
F _{syscik}	System Clock Frequency	_	20.0	MHz	Read-only from Flash memory.
		0.032768	20.0	MHz	Program or erasure of the Flash memory.
F _{XTAL}	Crystal Oscillator Frequency	0.032768	20.0	MHz	System clock frequencies below the crystal oscillator minimum require an external clock driver.
T _{XIN}	Crystal Oscillator Clock Period	50	-	ns	T _{CLK} = 1/F _{syscik}
T _{XINH}	System Clock High Time	20		ns	
T _{XINL}	System Clock Low Time	20		ns	
T _{XINR}	System Clock Rise Time	_	3	ns	T _{CLK} = 50 ns. Slower rise times can be tolerated with longer clock periods.
T _{XINF}	System Clock Fall Time	_	3	ns	T _{CLK} = 50 ns. Slower fall times can be tolerated with longer clock periods.



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	-

Binary	Hex	Assembly Mnemonic	Definition	Flag Test Operation
0011	3	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0100	4	OV	Overflow	V = 1
0101	5	MI	Minus	S = 1
0110	6	Z	Zero	Z = 1
0110	6	EQ	Equal	Z = 1
0111	7	С	Carry	C = 1
0111	7	ULT	Unsigned Less Than	C = 1
1000	8	T (or blank)	Always True	-
1001	9	GE	Greater Than or Equal	(S XOR V) = 0
1010	А	GT	Greater Than	(Z OR (S XOR V)) = 0
1011	В	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
1100	С	NOV	No Overflow	V = 0
1101	D	PL	Plus	S = 0
1110	Е	NZ	Non-Zero	Z = 0
1110	Е	NE	Not Equal	Z = 0
1111	F	NC	No Carry	C = 0
1111	F	UGE	Unsigned Greater Than or Equal	C = 0

Table 124. Condition Codes (Continued)

eZ8 CPU Instruction Classes

eZ8 CPU instructions can be divided functionally into the following groups:

- Arithmetic
- Bit Manipulation
- Block Transfer
- CPU Control
- Load
- Logical
- Program Control
- Rotate and Shift



Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	1 ² C	SPI	UARTs with IrDA	Description
Z8F482x with 48 KB Flash	n, 10-Bit	Analog	-to-D	ligita	l Co	onver	ter			
Standard Temperature: 0 °C	C to 70 °C)								
Z8F4821PM020SC	48 KB	4 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F4821AN020SC	48 KB	4 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F4821VN020SC	48 KB	4 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F4822AR020SC	48 KB	4 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F4822VS020SC	48 KB	4 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F4823FT020SC	48 KB	4 KB	60	24	4	12	1	1	2	QFP 80-pin package
Extended Temperature: -40	0 °C to +′	105 °C								
Z8F4821PM020EC	48 KB	4 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F4821AN020EC	48 KB	4 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F4821VN020EC	48 KB	4 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F4822AR020EC	48 KB	4 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F4822VS020EC	48 KB	4 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F4823FT020EC	48 KB	4 KB	60	24	4	12	1	1	2	QFP 80-pin package
Automotive/Industrial Temp	erature: -	–40 °C t	:0 +1:	25 °C	2					
Z8F4821PM020AC	48 KB	4 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F4821AN020AC	48 KB	4 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F4821VN020AC	48 KB	4 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F4822AR020AC	48 KB	4 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F4822VS020AC	48 KB	4 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F4823FT020AC	48 KB	4 KB	60	24	4	12	1	1	2	QFP 80-pin package