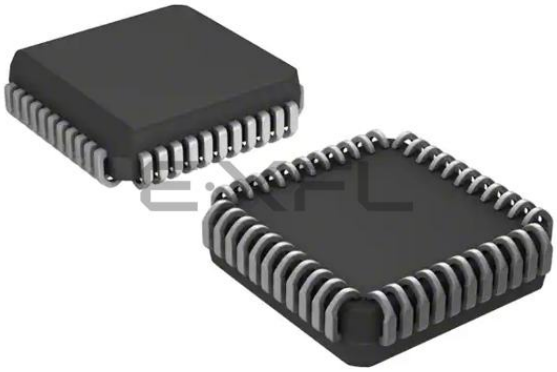

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f2421vn020ec00tr

Block Diagram

Figure 1 displays the block diagram of the architecture of the Z8 Encore! XP 64K Series Flash Microcontrollers.

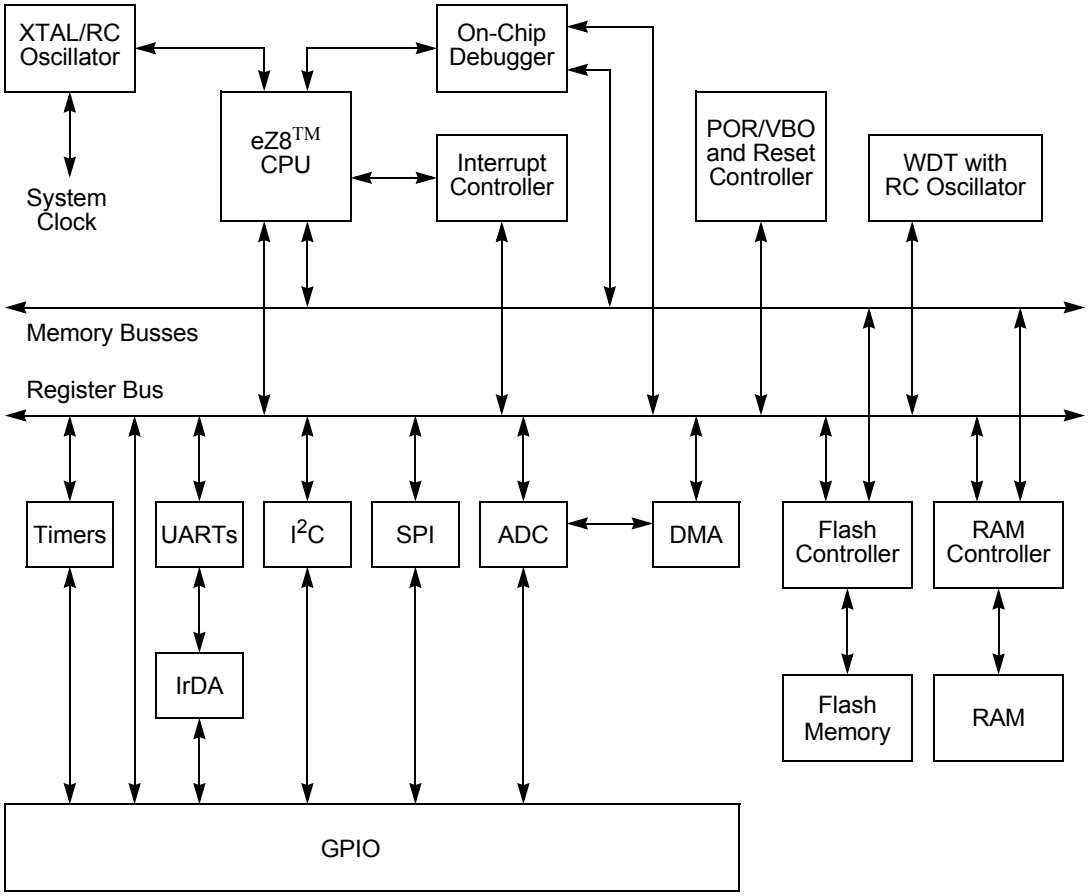


Figure 1. Z8 Encore! XP 64K Series Flash Microcontrollers Block Diagram

CPU and Peripheral Overview

eZ8™ CPU Features

The latest 8-bit eZ8 CPU meets the continuing demand for faster and more code-efficient microcontrollers. The eZ8 CPU executes a superset of the original Z8® instruction set.

UART0 Transmit Data
U0TXD (F40H - Write Only)

D7	D6	D5	D4	D3	D2	D1	D0

UART0 transmitter data byte [7:0]

UART0 Receive Data
U0RXD (F40H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

UART0 receiver data byte [7:0]

UART0 Status 0
U0STAT0 (F41H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

$\overline{\text{CTS}}$ signal
Returns the level of the $\overline{\text{CTS}}$ signal

Transmitter Empty
0 = Data is currently transmitting
1 = Transmission is complete

Transmitter Data Register Empty
0 = Transmit Data Register is full
1 = Transmit Data register is empty

Break Detect
0 = No break occurred
1 = A break occurred

Framing Error
0 = No framing error occurred
1 = A framing occurred

Overrun Error
0 = No overrun error occurred
1 = An overrun error occurred

Parity Error
0 = No parity error occurred
1 = A parity error occurred

Receive Data Available
0 = Receive Data Register is empty
1 = A byte is available in the Receive Data Register

UART0 Control 0
U0CTL0 (F42H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Loop Back Enable
0 = Normal operation
1 = Transmit data is looped back to the receiver

Stop Bit Select
0 = Transmitter sends 1 Stop bit
1 = Transmitter sends 2 Stop bits

Send Break
0 = No break is sent
1 = Output of the transmitter is zero

Parity Select
0 = Even parity
1 = Odd parity

Parity Enable
0 = Parity is disabled
1 = Parity is enabled

$\overline{\text{CTS}}$ Enable
0 = CTS signal has no effect on the transmitter
1 = UART recognizes $\overline{\text{CTS}}$ signal as a transmit enable control signal

Receive Enable
0 = Receiver disabled
1 = Receiver enabled

Transmit Enable
0 = Transmitter disabled
1 = Transmitter enabled

IRQ0 Enable Low Bit
IRQ0ENL (FC2H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: ADC IRQ Enable Hit Bit
- D1: SPI IRQ Enable Low Bit
- D2: I2C IRQ Enable Low Bit
- D3: UART 0 Transmitter IRQ Enable
- D4: UART 0 Receiver IRQ Enable Low
- D5: Timer 0 IRQ Enable Low Bit
- D6: Timer 1 IRQ Enable Low Bit
- D7: Timer 2 IRQ Enable Low Bit

Interrupt Request 1
IRQ1 (FC3H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: Port A or D Pin Interrupt Request
  0 = IRQ from corresponding pin [7:0] is not pending
  1 = IRQ from corresponding pin [7:0] is awaiting service

IRQ1 Enable High Bit
IRQ1ENH (FC4H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: Port A or D Pin IRQ Enable High Bit

IRQ1 Enable Low Bit
IRQ1ENL (FC5H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: Port A or D Pin IRQ Enable Low Bit

Interrupt Request 2
IRQ2 (FC6H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: Port C Pin Interrupt Request
  0 = IRQ from corresponding pin [3:0] is not pending
  1 = IRQ from corresponding pin [3:0] is awaiting service
- D1: DMA Interrupt Request
- D2: UART 1 Transmitter Interrupt
- D3: UART 1 Receiver Interrupt Request
- D4: Timer 3 Interrupt Request
- D5–D7: For all of the above peripherals:
  0 = Peripheral IRQ is not pending
  1 = Peripheral IRQ is awaiting service

IRQ2 Enable High Bit
IRQ2ENH (FC7H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: Port C Pin IRQ Enable High Bit
- D1: DMA IRQ Enable High Bit
- D2: UART 1 Transmitter IRQ Enable
- D3: UART 1 Receiver IRQ Enable High
- D4: Timer 3 IRQ Enable High Bit

IRQ2 Enable Low Bit
IRQ2ENL (FC8H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: Port C Pin IRQ Enable Low Bit
- D1: DMA IRQ Enable Low Bit
- D2: UART 1 Transmitter IRQ Enable
- D3: UART 1 Receiver IRQ Enable Low
- D4: Timer 3 IRQ Enable Low Bit

Interrupt Edge Select
IRQES (FCDH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: Port A or D Interrupt Edge Select
  0 = Falling edge
  1 = Rising edge

Interrupt Port Select
IRQPS (FCEH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port A or D Port Pin Select [7:0]
0 = Port A pin is the interrupt source
1 = Port D pin is the interrupt source

Interrupt Control
IRQCTL (FCFH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Reserved

Interrupt Request Enable
0 = Interrupts are disabled
1 = Interrupts are enabled

Port A Address
PAADDR (FD0H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = Stop Mode Recovery enable
06H-FFH = No function

Port A Control
PACTL (FD1H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Control[7:0]
Provides Access to Port Sub-Registers

Port A Input Data
PAIN (FD2H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Input Data [7:0]

Port A Output Data
PAOUT (FD3H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Output Data [7:0]

Port B Address
PBADDR (FD4H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port B Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = Stop Mode Recovery enable
06H-FFH = No function

Port B Control
PBCTL (FD5H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port B Control[7:0]
Provides Access to Port Sub-Registers

Port B Input Data
PBIN (FD6H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

Port B Input Data [7:0]

Port B Output Data
PBOUT (FD7H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port B Output Data [7:0]

Port C Address
PCADDR (FD8H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port C Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = Stop Mode Recovery enable
06H-FFH = No function

Flags

FLAGS (FFC - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0 — F1 - User Flag 1
- D1 — F2 - User Flag 2
- D2 — H - Half Carry
- D3 — D - Decimal Adjust
- D4 — V - Overflow Flag
- D5 — S - Sign Flag
- D6 — Z - Zero Flag
- D7 — C - Carry Flag

Register Pointer

RP (FFDH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D3:D0 — Working Register Page Address
- D7:D6 — Working Register Group Address

Stack Pointer High Byte

SPH (FFEH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D7:D0 — Stack Pointer [15:8]

Stack Pointer Low Byte

SPL (FFFH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D7:D0 — Stack Pointer [7:0]

110 = Divide by 64
111 = Divide by 128

TMODE—TIMER mode
000 = ONE-SHOT mode
001 = CONTINUOUS mode
010 = COUNTER mode
011 = PWM mode
100 = CAPTURE mode
101 = COMPARE mode
110 = GATED mode
111 = CAPTURE/COMPARE mode

Caution: *The 24-bit WDT Reload Value must not be set to a value less than* `000004H`.

Table 49. Watchdog Timer Reload Upper Byte Register (WDTU)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTU							
RESET	1							
R/W	R/W*							
ADDR	FF1H							

Note: R/W* - Read returns the current WDT count value. Write sets the desired Reload Value.

WDTU—WDT Reload Upper Byte
Most significant byte, Bits[23:16], of the 24-bit WDT reload value.

Table 50. Watchdog Timer Reload High Byte Register (WDTH)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTH							
RESET	1							
R/W	R/W*							
ADDR	FF2H							

Note: R/W* - Read returns the current WDT count value. Write sets the desired Reload Value.

WDTH—WDT Reload High Byte
Middle byte, Bits[15:8], of the 24-bit WDT reload value.

Table 51. Watchdog Timer Reload Low Byte Register (WDTL)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTL							
RESET	1							
R/W	R/W*							
ADDR	FF3H							

Note: R/W* - Read returns the current WDT count value. Write sets the desired Reload Value.

WDTL—WDT Reload Low
Least significant byte, Bits[7:0], of the 24-bit WDT reload value.

REN—Receive Enable
This bit enables or disables the receiver.
0 = Receiver disabled.
1 = Receiver enabled.

CTSE—CTS Enable
0 = The $\overline{\text{CTS}}$ signal has no effect on the transmitter.
1 = The UART recognizes the $\overline{\text{CTS}}$ signal as an enable control from the transmitter.

PEN—Parity Enable
This bit enables or disables parity. Even or odd is determined by the PSEL bit. It is overridden by the MPEN bit.
0 = Parity is disabled.
1 = The transmitter sends data with an additional parity bit and the receiver receives an additional parity bit.

PSEL—Parity Select
0 = Even parity is transmitted and expected on all received data.
1 = Odd parity is transmitted and expected on all received data.

SBRK—Send Break
This bit pauses or breaks data transmission. Sending a break interrupts any transmission in progress, so ensure that the transmitter has finished sending data before setting this bit.
0 = No break is sent.
1 = The output of the transmitter is zero.

STOP—Stop Bit Select
0 = The transmitter sends one stop bit.
1 = The transmitter sends two stop bits.

LBEN—Loop Back Enable
0 = Normal operation.
1 = All transmitted data is looped back to the receiver.

Table 57. UART Control 1 Register (U*x*CTL1)

BITS	7	6	5	4	3	2	1	0
FIELD	MPMD[1]	MPEN	MPMD[0]	MPBT	DEPOL	BRGCTL	RDAIRQ	IREN
RESET	0							
R/W	R/W							
ADDR	F43H and F4BH							

MPMD[1:0]—MULTIPROCESSOR Mode
If MULTIPROCESSOR (9-bit) mode is enabled,
00 = The UART generates an interrupt request on all received bytes (data and address).

Operation

When the Infrared Endec is enabled, the transmit data from the associated on-chip UART is encoded as digital signals in accordance with the IrDA standard and output to the infrared transceiver via the TXD pin. Likewise, data received from the infrared transceiver is passed to the Infrared Endec via the RXD pin, decoded by the Infrared Endec, and then passed to the UART. Communication is half-duplex, which means simultaneous data transmission and reception is not allowed.

The baud rate is set by the UART's Baud Rate Generator and supports IrDA standard baud rates from 9600 baud to 115.2 Kbaud. Higher baud rates are possible, but do not meet IrDA specifications. The UART must be enabled to use the Infrared Endec. The Infrared Endec data rate is calculated using the following equation:

$$\text{Infrared Data Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$$

Transmitting IrDA Data

The data to be transmitted using the infrared transceiver is first sent to the UART. The UART's transmit signal (TXD) and baud rate clock are used by the IrDA to generate the modulation signal (IR_TXD) that drives the infrared transceiver. Each UART/Infrared data bit is 16-clock wide. If the data to be transmitted is 1, the IR_TXD signal remains low for the full 16-clock period. If the data to be transmitted is 0, a 3-clock high pulse is output following a 7-clock low period. After the 3-clock high pulse, a 6-clock low pulse is output to complete the full 16-clock data period. Figure 20 displays IrDA data transmission. When the Infrared Endec is enabled, the UART's TXD signal is internal to the 64K Series products while the IR_TXD signal is output through the TXD pin.

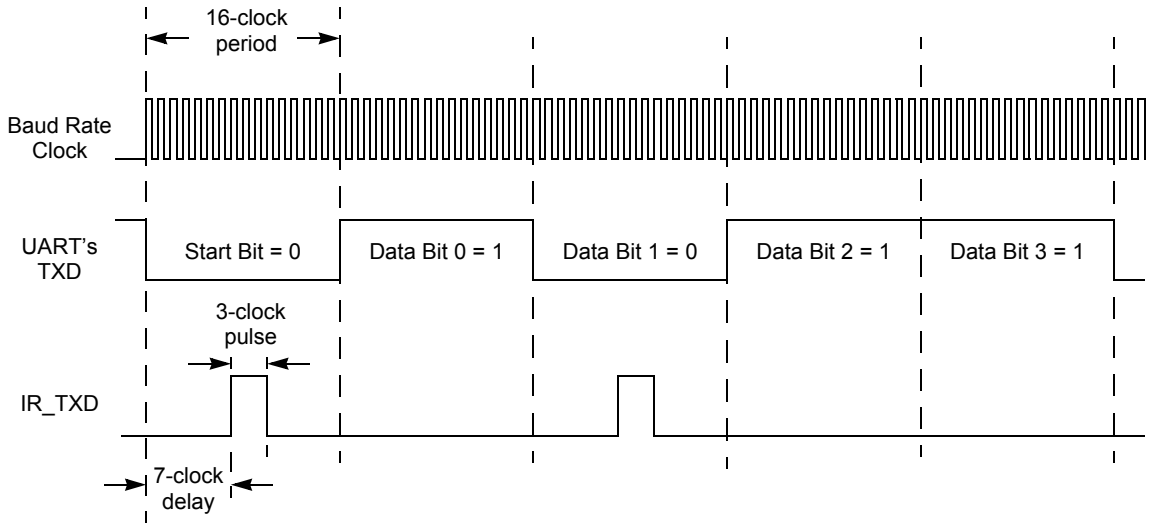


Figure 20. Infrared Data Transmission

Serial Peripheral Interface

Overview

The Serial Peripheral Interface is a synchronous interface allowing several SPI-type devices to be interconnected. SPI-compatible devices include EEPROMs, Analog-to-Digital Converters, and ISDN devices. Features of the SPI include:

- Full-duplex, synchronous, character-oriented communication
- Four-wire interface
- Data transfers rates up to a maximum of one-half the system clock frequency
- Error detection
- Dedicated Baud Rate Generator

Architecture

The SPI may be configured as either a Master (in single or multi-master systems) or a Slave as displayed in Figure 22 through Figure 24.

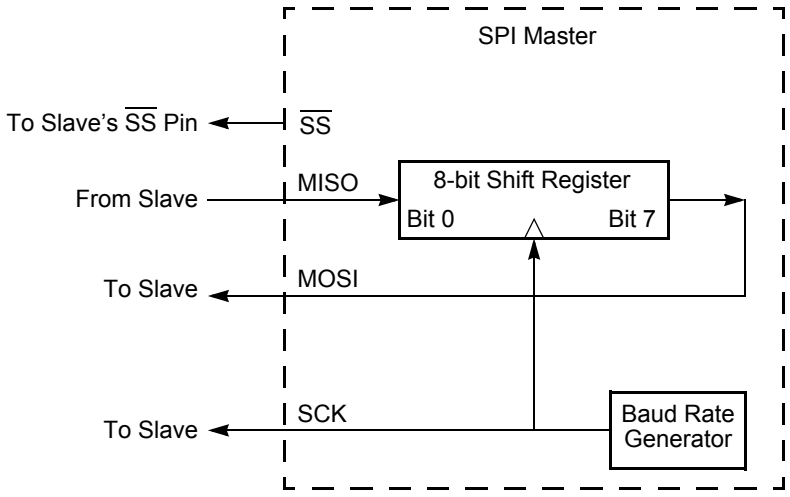


Figure 22. SPI Configured as a Master in a Single Master, Single Slave System

IEN—I2C Enable
1 = The I2C transmitter and receiver are enabled.
0 = The I2C transmitter and receiver are disabled.

START—Send Start Condition
This bit sends the Start condition. Once asserted, it is cleared by the I2C Controller after it sends the START condition or if the IEN bit is deasserted. If this bit is 1, it cannot be cleared to 0 by writing to the register. After this bit is set, the Start condition is sent if there is data in the I2C Data or I2C Shift register. If there is no data in one of these registers, the I2C Controller waits until the Data register is written. If this bit is set while the I2C Controller is shifting out data, it generates a START condition after the byte shifts and the acknowledge phase completes. If the STOP bit is also set, it also waits until the STOP condition is sent before the sending the START condition.

STOP—Send Stop Condition
This bit causes the I2C Controller to issue a Stop condition after the byte in the I2C Shift register has completed transmission or after a byte has been received in a receive operation. Once set, this bit is reset by the I2C Controller after a Stop condition has been sent or by deasserting the IEN bit. If this bit is 1, it cannot be cleared to 0 by writing to the register.

BIRQ—Baud Rate Generator Interrupt Request
This bit allows the I2C Controller to be used as an additional timer when the I2C Controller is disabled. This bit is ignored when the I2C Controller is enabled.
1 = An interrupt occurs every time the baud rate generator counts down to one.
0 = No baud rate generator interrupt occurs.

TXI—Enable TDRE interrupts
This bit enables the transmit interrupt when the I2C Data register is empty (TDRE = 1).
1 = Transmit interrupt (and DMA transmit request) is enabled.
0 = Transmit interrupt (and DMA transmit request) is disabled.

NAK—Send NAK
This bit sends a Not Acknowledge condition after the next byte of data has been read from the I2C slave. Once asserted, it is deasserted after a Not Acknowledge is sent or the IEN bit is deasserted. If this bit is 1, it cannot be cleared to 0 by writing to the register.

FLUSH—Flush Data
Setting this bit to 1 clears the I2C Data register and sets the TDRE bit to 1. This bit allows flushing of the I2C Data register when a Not Acknowledge interrupt is received after the data has been sent to the I2C Data register. Reading this bit always returns 0.

FILTEN—I2C Signal Filter Enable
This bit enables low-pass digital filters on the SDA and SCL input signals. These filters reject any input pulse with periods less than a full system clock cycle. The filters introduce a 3-system clock cycle latency on the inputs.
1 = low-pass filters are enabled.
0 = low-pass filters are disabled.

Table 88. ADC Data Low Bits Register (ADCD_L)

BITS	7	6	5	4	3	2	1	0
FIELD	ADCD_L		Reserved					
RESET	X							
R/W	R							
ADDR	F73H							

ADCD_L—ADC Data Low Bits
These are the least significant two bits of the 10-bit ADC output. These bits are undefined after a Reset.

Reserved
These bits are reserved and are always undefined.

Information Area

Table 91 describes the 64K Series Information Area. This 512-byte Information Area is accessed by setting bit 7 of the Page Select Register to 1. When access is enabled, the Information Area is mapped into Flash Memory and overlays the 512 bytes at addresses FE00H to FFFFH. When the Information Area access is enabled, LDC instructions return data from the Information Area. CPU instruction fetches always comes from Flash Memory regardless of the Information Area access bit. Access to the Information Area is read-only.

Table 91. Z8 Encore! XP 64K Series Flash Microcontrollers Information Area Map

Flash Memory Address (Hex)	Function
FE00H-FE3FH	Reserved
FE40H-FE53H	Part Number 20-character ASCII alphanumeric code Left justified and filled with zeros
FE54H-FFFFH	Reserved

Operation

The Flash Controller provides the proper signals and timing for Byte Programming, Page Erase, and Mass Erase of the Flash memory. The Flash Controller contains a protection mechanism, via the Flash Control register (FCTL), to prevent accidental programming or erasure. The following subsections provide details on the various operations (Lock, Unlock, Sector Protect, Byte Programming, Page Erase, and Mass Erase).

On-Chip Debugger Timing

Figure 52 and Table 116 provide timing information for the DBG pin. The DBG pin timing specifications assume a 4 µs maximum rise and fall time.

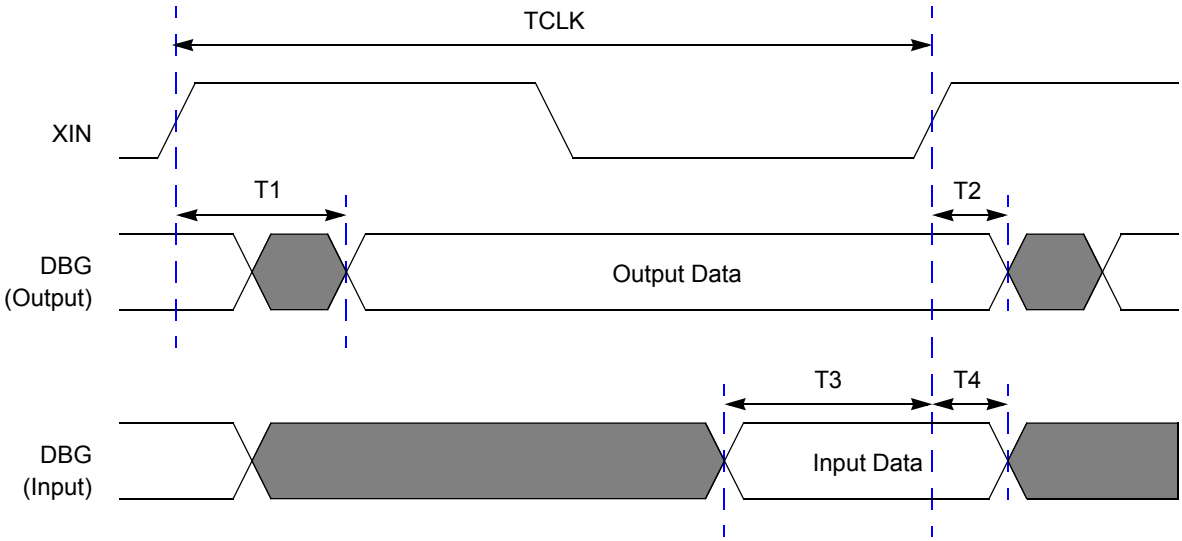


Figure 52. On-Chip Debugger Timing

Table 116. On-Chip Debugger Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
DBG			
T_1	XIN Rise to DBG Valid Delay	–	30
T_2	XIN Rise to DBG Output Hold Time	2	–
T_3	DBG to XIN Rise Input Setup Time	10	–
T_4	DBG to XIN Rise Input Hold Time	5	–
	DBG frequency		System Clock/4

Table 125 through Table 132 contain the instructions belonging to each group and the number of operands required for each instruction. Some instructions appear in more than one table as these instruction can be considered as a subset of more than one category. Within these tables, the source operand is identified as 'src', the destination operand is 'dst' and a condition code is 'cc'.

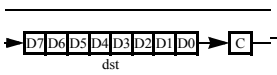
Table 125. Arithmetic Instructions

Mnemonic	Operands	Instruction
ADC	dst, src	Add with Carry
ADCX	dst, src	Add with Carry using Extended Addressing
ADD	dst, src	Add
ADDX	dst, src	Add using Extended Addressing
CP	dst, src	Compare
CPC	dst, src	Compare with Carry
CPCX	dst, src	Compare with Carry using Extended Addressing
CPX	dst, src	Compare using Extended Addressing
DA	dst	Decimal Adjust
DEC	dst	Decrement
DECW	dst	Decrement Word
INC	dst	Increment
INCW	dst	Increment Word
MULT	dst	Multiply
SBC	dst, src	Subtract with Carry
SBCX	dst, src	Subtract with Carry using Extended Addressing
SUB	dst, src	Subtract
SUBX	dst, src	Subtract using Extended Addressing

Table 126. Bit Manipulation Instructions

Mnemonic	Operands	Instruction
BCLR	bit, dst	Bit Clear
BIT	p, bit, dst	Bit Set or Clear
BSET	bit, dst	Bit Set

Table 133. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
RRC dst		R		C0	*	*	*	*	-	-	2	2
		IR		C1							2	3
SBC dst, src	dst ← dst – src - C	r	r	32	*	*	*	*	1	*	2	3
		r	Ir	33							2	4
		R	R	34							3	3
		R	IR	35							3	4
		R	IM	36							3	3
		IR	IM	37							3	4
SBCX dst, src	dst ← dst – src - C	ER	ER	38	*	*	*	*	1	*	4	3
		ER	IM	39							4	3
SCF	C ← 1			DF	1	-	-	-	-	-	1	2
SRA dst		R		D0	*	*	*	0	-	-	2	2
		IR		D1							2	3
SRL dst		R		1F C0	*	*	0	*	-	-	3	2
		IR		1F C1							3	3
SRP src	RP ← src		IM	01	-	-	-	-	-	-	2	2
STOP	STOP Mode			6F	-	-	-	-	-	-	1	2
SUB dst, src	dst ← dst – src	r	r	22	*	*	*	*	1	*	2	3
		r	Ir	23							2	4
		R	R	24							3	3
		R	IR	25							3	4
		R	IM	26							3	3
		IR	IM	27							3	4
SUBX dst, src	dst ← dst – src	ER	ER	28	*	*	*	*	1	*	4	3
		ER	IM	29							4	3

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