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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	46
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f2422vs020ec

Port C Control
PCCTL (FD9H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port C Control[7:0]
Provides Access to Port Sub-Registers

Port C Input Data
PCIN (FDAH - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

Port C Input Data [7:0]

Port C Output Data
PCOUT (FDBH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port C Output Data [7:0]

Port D Address
PDADDR (FDCH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port D Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = Stop Mode Recovery enable
06H-FFH = No function

Port D Control
PDCTL (FDDH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port D Control[7:0]
Provides Access to Port Sub-Registers

Port D Input Data
PDIN (FDE H- Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

Port D Input Data [7:0]

Port D Output Data
PDOUT (FDFH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port D Output Data [7:0]

Port E Address
PEADDR (FE0H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port E Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = Stop Mode Recovery enable
06H-FFH = No function

Port E Control
PECTL (FE1H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port E Control[7:0]
Provides Access to Port Sub-Registers

Port E Input Data
PEIN (FE2H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

Port E Input Data [7:0]

Port E Output Data
PEOUT (FE3H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port E Output Data [7:0]

Port F Address
PFADDR (FE4H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port F Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = Stop Mode Recovery enable
06H-FFH = No function

Table 12. Port Alternate Function Mapping (Continued)

Port	Pin	Mnemonic	Alternate Function Description
Port C	PC0	T1IN	Timer 1 Input
	PC1	T1OUT	Timer 1 Output
	PC2	SS	SPI Slave Select
	PC3	SCK	SPI Serial Clock
	PC4	MOSI	SPI Master Out/Slave In
	PC5	MISO	SPI Master In/Slave Out
	PC6	T2IN	Timer 2 In
	PC7	T2OUT	Timer 2 Out
Port D	PD0	T3IN	Timer 3 In (unavailable in 44-pin packages)
	PD1	T3OUT	Timer 3 Out (unavailable in 44-pin packages)
	PD2	N/A	No alternate function
	PD3	DE1	UART 1 Driver Enable
	PD4	RXD1/IRRX1	UART 1/IrDA 1 Receive Data
	PD5	TXD1/IRTX1	UART 1/IrDA 1 Transmit Data
	PD6	CTS1	UART 1 Clear to Send
	PD7	RCOUT	Watchdog Timer RC Oscillator Output
Port E	PE[7:0]	N/A	No alternate functions
Port F	PF[7:0]	N/A	No alternate functions
Port G	PG[7:0]	N/A	No alternate functions
Port H	PH0	ANA8	ADC Analog Input 8
	PH1	ANA9	ADC Analog Input 9
	PH2	ANA10	ADC Analog Input 10
	PH3	ANA11	ADC Analog Input 11

GPIO Interrupts

Many of the GPIO port pins can be used as interrupt sources. Some port pins may be configured to generate an interrupt request on either the rising edge or falling edge of the pin input signal. Other port pin interrupts generate an interrupt when any edge occurs (both rising and falling). For more information on interrupts using the GPIO pins, see Interrupt Controller on page 67.

Port A–H Data Direction Sub-Registers

The Port A–H Data Direction sub-register is accessed through the Port A–H Control register by writing 01H to the Port A–H Address register (Table 16).

Table 16. Port A–H Data Direction Sub-Registers

BITS	7	6	5	4	3	2	1	0
FIELD	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET	1							
R/W	R/W							
ADDR	If 01H in Port A–H Address Register, accessible through Port A–H Control Register							

DD[7:0]—Data Direction
These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction register setting.
0 = Output. Data in the Port A–H Output Data register is driven onto the port pin.
1 = Input. The port pin is sampled and the value written into the Port A–H Input Data Register. The output driver is tri-stated.

Port A–H Alternate Function Sub-Registers

The Port A–H Alternate Function sub-register (Table 17) is accessed through the Port A–H Control register by writing `02H` to the Port A–H Address register. The Port A–H Alternate Function sub-registers select the alternate functions for the selected pins. To determine the alternate function associated with each port pin, see GPIO Alternate Functions on page 59.

Caution: *Do not enable alternate function for GPIO port pins which do not have an associated alternate function. Failure to follow this guideline may result in unpredictable operation.*

Table 17. Port A–H Alternate Function Sub-Registers

BITS	7	6	5	4	3	2	1	0
FIELD	AF7	AF6	AF5	AF4	AF3	AF2	AF1	AF0
RESET	0							
R/W	R/W							
ADDR	If 02H in Port A–H Address Register, accessible through Port A–H Control Register							

Table 42. Timer 0-3 Reload Low Byte Register (TxRL)

BITS	7	6	5	4	3	2	1	0
FIELD	TRL							
RESET	1							
R/W	R/W							
ADDR	F03H, F0BH, F13H, F1BH							

TRH and TRL—Timer Reload Register High and Low
These two bytes form the 16-bit Reload value, {TRH[7:0], TRL[7:0]}. This value sets the maximum count value which initiates a timer reload to `0001H`. In COMPARE mode, these two byte form the 16-bit Compare value.

Timer 0-3 PWM High and Low Byte Registers

The Timer 0-3 PWM High and Low Byte (TxPWMH and TxPWML) registers (see Table 43 and Table 44 on page 92) are used for Pulse-Width Modulator (PWM) operations. These registers also store the Capture values for the Capture and Capture/COMPARE modes.

Table 43. Timer 0-3 PWM High Byte Register (TxPWMH)

BITS	7	6	5	4	3	2	1	0
FIELD	PWMH							
RESET	0							
R/W	R/W							
ADDR	F04H, F0CH, F14H, F1CH							

Table 44. Timer 0-3 PWM Low Byte Register (TxPWML)

BITS	7	6	5	4	3	2	1	0
FIELD	PWML							
RESET	0							
R/W	R/W							
ADDR	F05H, F0DH, F15H, F1DH							

Caution: *The 24-bit WDT Reload Value must not be set to a value less than* `000004H`.

Table 49. Watchdog Timer Reload Upper Byte Register (WDTU)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTU							
RESET	1							
R/W	R/W*							
ADDR	FF1H							
Note: R/W* - Read returns the current WDT count value. Write sets the desired Reload Value.								

WDTU—WDT Reload Upper Byte
Most significant byte, Bits[23:16], of the 24-bit WDT reload value.

Table 50. Watchdog Timer Reload High Byte Register (WDTH)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTH							
RESET	1							
R/W	R/W*							
ADDR	FF2H							
Note: R/W* - Read returns the current WDT count value. Write sets the desired Reload Value.								

WDTH—WDT Reload High Byte
Middle byte, Bits[15:8], of the 24-bit WDT reload value.

Table 51. Watchdog Timer Reload Low Byte Register (WDTL)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTL							
RESET	1							
R/W	R/W*							
ADDR	FF3H							
Note: R/W* - Read returns the current WDT count value. Write sets the desired Reload Value.								

WDTL—WDT Reload Low
Least significant byte, Bits[7:0], of the 24-bit WDT reload value.

3. Clear the UART Receiver interrupt in the applicable Interrupt Request register.
4. Execute the IRET instruction to return from the interrupt-service routine and await more data.

Clear To Send (CTS) Operation

The CTS pin, if enabled by the CTSE bit of the UART Control 0 register, performs flow control on the outgoing transmit datastream. The Clear To Send (CTS) input pin is sampled one system clock before beginning any new character transmission. To delay transmission of the next data character, an external receiver must deassert CTS at least one system clock cycle before a new data transmission begins. For multiple character transmissions, this would typically be done during Stop Bit transmission. If CTS deasserts in the middle of a character transmission, the current character is sent completely.

MULTIPROCESSOR (9-bit) Mode

The UART has a MULTIPROCESSOR (9-bit) mode that uses an extra (9th) bit for selective communication when a number of processors share a common UART bus. In MULTIPROCESSOR mode (also referred to as 9-Bit mode), the multiprocessor bit (MP) is transmitted immediately following the 8-bits of data and immediately preceding the Stop bit(s) as displayed in Figure 16. The character format is:

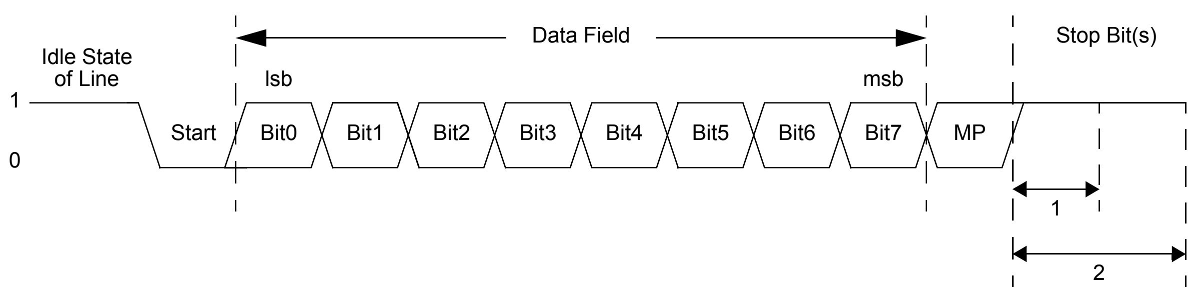


Figure 16. UART Asynchronous MULTIPROCESSOR Mode Data Format

In MULTIPROCESSOR (9-bit) mode, the Parity bit location (9th bit) becomes the MULTIPROCESSOR control bit. The UART Control 1 and Status 1 registers provide MULTIPROCESSOR (9-bit) mode control and status information. If an automatic address matching scheme is enabled, the UART Address Compare register holds the network address of the device.

MULTIPROCESSOR (9-bit) Mode Receive Interrupts

When MULTIPROCESSOR mode is enabled, the UART only processes frames addressed to it. The determination of whether a frame of data is addressed to the UART can be made in hardware, software or some combination of the two, depending on the multiprocessor

Infrared Encoder/Decoder

Overview

The 64K Series products contain two fully-functional, high-performance UART to Infrared Encoder/Decoders (Endecs). Each Infrared Endec is integrated with an on-chip UART to allow easy communication between the 64K Series and IrDA Physical Layer Specification, Version 1.3-compliant infrared transceivers. Infrared communication provides secure, reliable, low-cost, point-to-point communication between PCs, PDAs, cell phones, printers, and other infrared enabled devices.

Architecture

Figure 19 displays the architecture of the Infrared Endec.

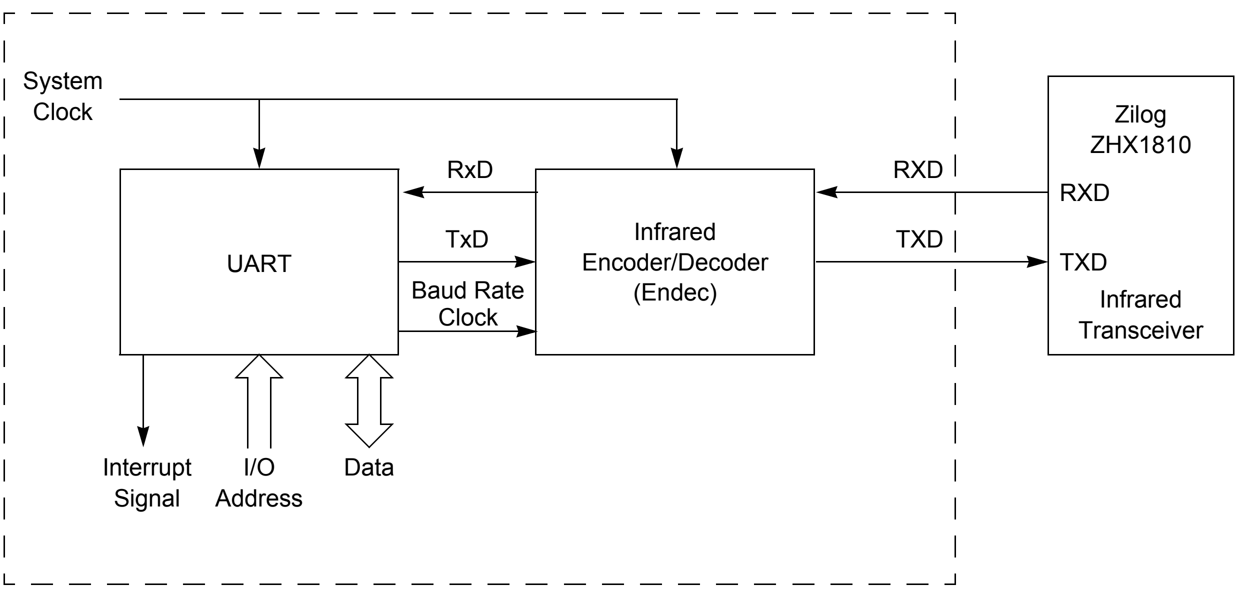


Figure 19. Infrared Data Communication System Block Diagram

The first seven bits transmitted in the first byte are 11110XX. The two bits XX are the two most-significant bits of the 10-bit address. The lowest bit of the first byte transferred is the read/write control bit (=0). The transmit operation is carried out in the same manner as 7-bit addressing.

Follow the steps below for a transmit operation on a 10-bit addressed slave:

1. Software asserts the IEN bit in the I^2C Control register.
2. Software asserts the TXI bit of the I^2C Control register to enable Transmit interrupts.
3. The I^2C interrupt asserts because the I^2C Data register is empty.
4. Software responds to the TDRE interrupt by writing the first slave address byte to the I^2C Data register. The least-significant bit must be 0 for the write operation.
5. Software asserts the START bit of the I^2C Control register.
6. The I^2C Controller sends the START condition to the I^2C slave.
7. The I^2C Controller loads the I^2C Shift register with the contents of the I^2C Data register.
8. After one bit of address is shifted out by the SDA signal, the Transmit interrupt is asserted.
9. Software responds by writing the second byte of address into the contents of the I^2C Data register.
10. The I^2C Controller shifts the rest of the first byte of address and write bit out the SDA signal.
11. If the I^2C slave acknowledges the first address byte by pulling the SDA signal low during the next high period of SCL, the I^2C Controller sets the ACK bit in the I^2C Status register. Continue with step 12.

    If the slave does not acknowledge the first address byte, the I^2C Controller sets the NCKI bit and clears the ACK bit in the I^2C Status register. Software responds to the Not Acknowledge interrupt by setting the STOP and FLUSH bits and clearing the TXI bit. The I^2C Controller sends the STOP condition on the bus and clears the STOP and NCKI bits. The transaction is complete (ignore the following steps).
12. The I^2C Controller loads the I^2C Shift register with the contents of the I^2C Data register.
13. The I^2C Controller shifts the second address byte out the SDA signal. After the first bit has been sent, the Transmit interrupt is asserted.
14. Software responds by writing a data byte to the I^2C Data register.
15. The I^2C Controller completes shifting the contents of the shift register on the SDA signal.

4. The I^2C Controller sends the START condition.
5. The I^2C Controller shifts the address and read bit out the SDA signal.
6. If the I^2C slave acknowledges the address by pulling the SDA signal Low during the next high period of SCL, the I^2C Controller sets the ACK bit in the I^2C Status register. Continue with step 7.

   If the slave does not acknowledge, the Not Acknowledge interrupt occurs (NCKI bit is set in the Status register, ACK bit is cleared). Software responds to the Not Acknowledge interrupt by setting the STOP bit and clearing the TXI bit. The I^2C Controller sends the STOP condition on the bus and clears the STOP and NCKI bits. The transaction is complete (ignore the following steps).
7. The I^2C Controller shifts in the byte of data from the I^2C slave on the SDA signal. The I^2C Controller sends a Not Acknowledge to the I^2C slave if the NAK bit is set (last byte), else it sends an Acknowledge.
8. The I^2C Controller asserts the Receive interrupt (RDRF bit set in the Status register).
9. Software responds by reading the I^2C Data register which clears the RDRF bit. If there is only one more byte to receive, set the NAK bit of the I^2C Control register.
10. If there are more bytes to transfer, return to step 7.
11. After the last byte is shifted in, a Not Acknowledge interrupt is generated by the I^2C Controller.
12. Software responds by setting the `STOP` bit of the I^2C Control register.
13. A STOP condition is sent to the I^2C slave, the STOP and NCKI bits are cleared.

Read Transaction with a 10-Bit Address

Figure 33 displays the read transaction format for a 10-bit addressed slave. The shaded regions indicate data transferred from the I^2C Controller to slaves and unshaded regions indicate data transferred from the slaves to the I^2C Controller.

S	Slave Address 1st 7 bits	W=0	A	Slave Address 2nd Byte	A	S	Slave Address 1st 7 bits	R=1	A	Data	A	Data	$\overline{A}$	P

Figure 33. Receive Data Format for a 10-Bit Addressed Slave

The first seven bits transmitted in the first byte are `11110XX`. The two bits `XX` are the two most-significant bits of the 10-bit address. The lowest bit of the first byte transferred is the write control bit.

Direct Memory Access Controller

Overview

The 64K Series Direct Memory Access (DMA) Controller provides three independent Direct Memory Access channels. Two of the channels (DMA0 and DMA1) transfer data between the on-chip peripherals and the Register File. The third channel (DMA_ADC) controls the ADC operation and transfers SINGLE-SHOT mode ADC output data to the Register File.

Operation

DMA0 and DMA1 Operation

DMA0 and DMA1, referred to collectively as DMA*x*, transfer data either from the on-chip peripheral control registers to the Register File, or from the Register File to the on-chip peripheral control registers. The sequence of operations in a DMA*x* data transfer is:

1. DMA*x* trigger source requests a DMA data transfer.
2. DMA*x* requests control of the system bus (address and data) from the eZ8 CPU.
3. After the eZ8 CPU acknowledges the bus request, DMA*x* transfers either a single byte or a two-byte word (depending upon configuration) and then returns system bus control back to the eZ8 CPU.
4. If Current Address equals End Address:
   – DMA*x* reloads the original Start Address
   – If configured to generate an interrupt, DMA*x* sends an interrupt request to the Interrupt Controller
   – If configured for single-pass operation, DMA*x* resets the DEN bit in the DMA*x* Control register to 0 and the DMA is disabled.

   If Current Address does not equal End Address, the Current Address increments by 1 (single-byte transfer) or 2 (two-byte word transfer).

Table 88. ADC Data Low Bits Register (ADCD_L)

BITS	7	6	5	4	3	2	1	0
FIELD	ADCD_L		Reserved					
RESET	X							
R/W	R							
ADDR	F73H							

ADCD_L—ADC Data Low Bits
These are the least significant two bits of the 10-bit ADC output. These bits are undefined after a Reset.

Reserved
These bits are reserved and are always undefined.

On-Chip Debugger Control Register Definitions

OCD Control Register

The OCD Control register (Table 102) controls the state of the On-Chip Debugger. This register enters or exits DEBUG mode and enables the BRK instruction. It can also reset the Z8F642x family, Z8R642x family device.

A 'reset and stop' function can be achieved by writing 81H to this register. A 'reset and go' function can be achieved by writing 41H to this register. If the device is in DEBUG mode, a 'run' function can be implemented by writing 40H to this register.

Table 102. OCD Control Register (OCDCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	DBGMODE	BRKEN	DBGACK	BRKLOOP			Reserved	RST
RESET	0							
R/W	R/W			R				R/W

DBGMODE—DEBUG Mode
Setting this bit to 1 causes the device to enter DEBUG mode. When in DEBUG mode, the eZ8 CPU stops fetching new instructions. Clearing this bit causes the eZ8 CPU to start running again. This bit is automatically set when a BRK instruction is decoded and Breakpoints are enabled. If the Read Protect Option Bit is enabled, this bit can only be cleared by resetting the device, it cannot be written to 0.
0 = The 64K Series device is operating in NORMAL mode.
1 = The 64K Series device is in DEBUG mode.

BRKEN—Breakpoint Enable
This bit controls the behavior of the BRK instruction (opcode 00H). By default, Breakpoints are disabled and the BRK instruction behaves like a NOP. If this bit is set to 1 and a BRK instruction is decoded, the OCD takes action dependent upon the BRKLOOP bit.
0 = BRK instruction is disabled.
1 = BRK instruction is enabled.

DBGACK—Debug Acknowledge
This bit enables the debug acknowledge feature. If this bit is set to 1, then the OCD sends an Debug Acknowledge character (FFH) to the host when a Breakpoint occurs.
0 = Debug Acknowledge is disabled.
1 = Debug Acknowledge is enabled.

BRKLOOP—Breakpoint Loop
This bit determines what action the OCD takes when a BRK instruction is decoded if breakpoints are enabled (BRKEN is 1). If this bit is 0, then the DBGMODE bit is automatically set to 1 and the OCD entered DEBUG mode. If BRKLOOP is set to 1, then the

Figure 45 displays the typical current consumption in HALT mode while operating at 25 ºC versus the system clock frequency. All GPIO pins are configured as outputs and driven High.

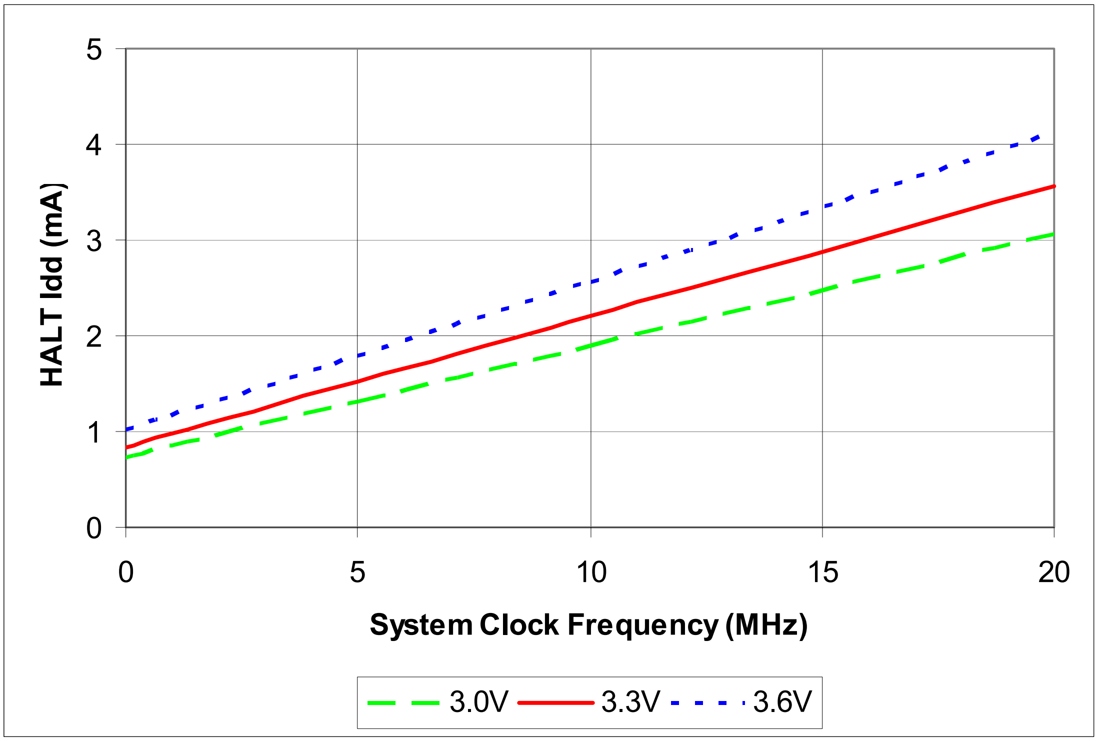


Figure 45. Typical HALT Mode Idd Versus System Clock Frequency

I^2C Timing

Figure 55 and Table 119 provide timing information for I^2C pins.

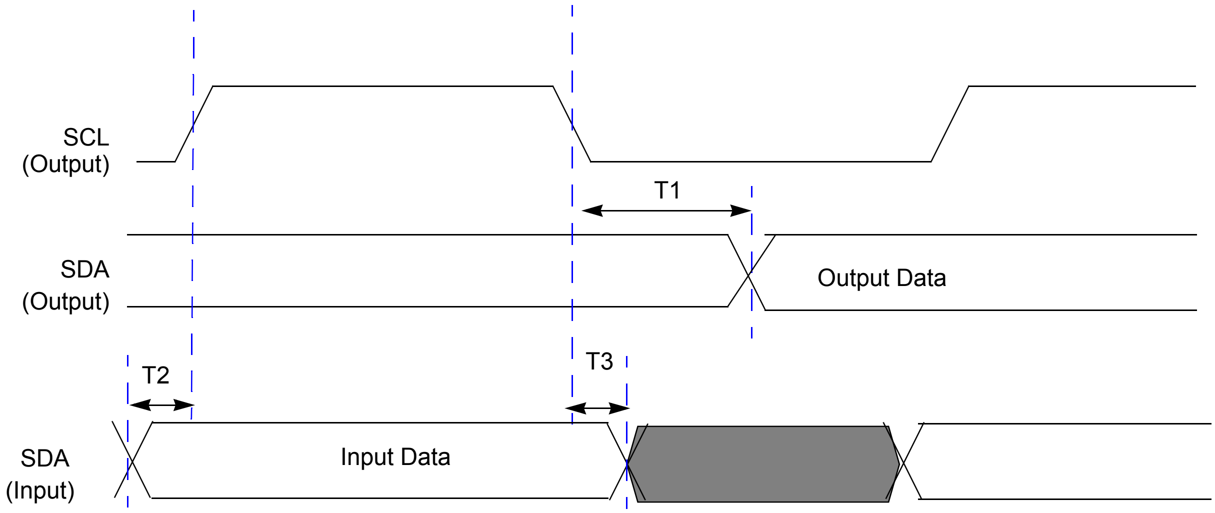
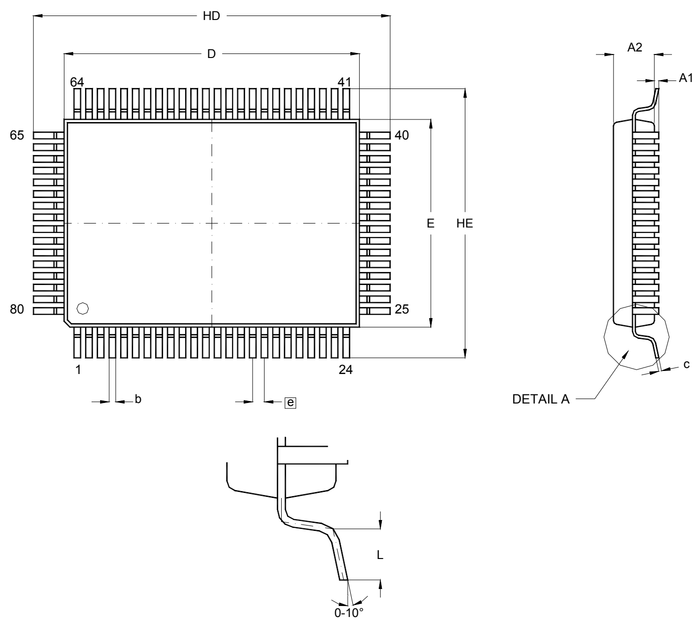


Figure 55. I^2C Timing

Table 119. I^2C Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
I^2C			
T_1	SCL Fall to SDA output delay	SCL period/4	
T_2	SDA Input to SCL rising edge Setup Time	0	
T_3	SDA Input to SCL falling edge Hold Time	0	

Figure 67 displays the 80-pin Quad Flat Package (QFP) available for the Z8X4823 and Z8X6423 devices.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.38	.004	.015
A2	2.60	2.80	.102	.110
b	0.30	0.45	.012	.018
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.80 BSC		.0315 BSC	
L	0.70	1.10	.028	.043

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 67. 80-Lead Quad-Flat Package (QFP)

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I^{2}C	SPI	UARTs with IrDA	Description
Z8F162x with 16 KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0 °C to 70 °C										
Z8F1621PM020SC	16 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F1621AN020SC	16 KB	2 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F1621VN020SC	16 KB	2 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F1622AR020SC	16 KB	2 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F1622VS020SC	16 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Extended Temperature: –40 °C to +105 °C										
Z8F1621PM020EC	16 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F1621AN020EC	16 KB	2 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F1621VN020EC	16 KB	2 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F1622AR020EC	16 KB	2 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F1622VS020EC	16 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Automotive/Industrial Temperature: –40 °C to +125 °C										
Z8F1621PM020AC	16 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F1621AN020AC	16 KB	2 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F1621VN020AC	16 KB	2 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F1622AR020AC	16 KB	2 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F1622VS020AC	16 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F64200100KITG										Development Kit
ZUSBSC00100ZACG										USB Smart Cable Accessory Kit
ZUSBOPTSC01ZACG										Opto-Isolated USB Smart Cable Accessory Kit

Note: Replace C with G for lead-free packaging.