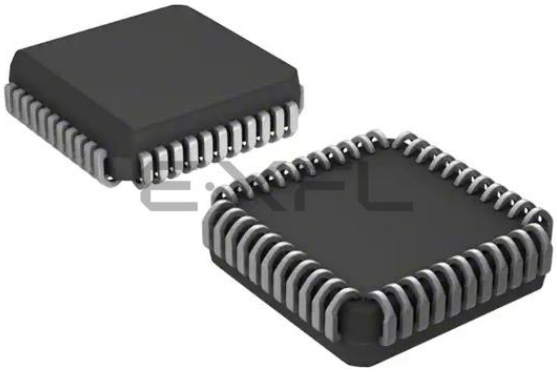

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f3221vn020sc

Use of All Uppercase Letters

The use of all uppercase letters designates the names of states, modes, and commands.

- Example 1: The bus is considered BUSY after the Start condition.
- Example 2: A START command triggers the processing of the initialization sequence.
- Example 3: STOP mode.

Bit Numbering

Bits are numbered from *0* to *n–1* where *n* indicates the total number of bits. For example, the 8 bits of a register are numbered from 0 to 7.

Safeguards

It is important that you understand the following safety terms, which are defined here.

Caution: *Indicates a procedure or file may become corrupted if you do not follow directions.*

Table 7. Z8 Encore! XP 64K Series Flash Microcontrollers Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
F61	SPI Control	SPICTL	00	137
F62	SPI Status	SPISTAT	01	139
F63	SPI Mode	SPIMODE	00	140
F64	SPI Diagnostic State	SPIDST	00	141
F65	Reserved	—	XX	
F66	SPI Baud Rate High Byte	SPIBRH	FF	142
F67	SPI Baud Rate Low Byte	SPIBRL	FF	142
F68-F6F	Reserved	—	XX	
Analog-to-Digital Converter				
F70	ADC Control	ADCCTL	20	179
F71	Reserved	—	XX	
F72	ADC Data High Byte	ADCD_H	XX	180
F73	ADC Data Low Bits	ADCD_L	XX	180
F74-FAF	Reserved	—	XX	
DMA 0				
FB0	DMA0 Control	DMA0CTL	00	167
FB1	DMA0 I/O Address	DMA0IO	XX	169
FB2	DMA0 End/Start Address High Nibble	DMA0H	XX	169
FB3	DMA0 Start Address Low Byte	DMA0START	XX	170
FB4	DMA0 End Address Low Byte	DMA0END	XX	170
DMA 1				
FB8	DMA1 Control	DMA1CTL	00	167
FB9	DMA1 I/O Address	DMA1IO	XX	169
FBA	DMA1 End/Start Address High Nibble	DMA1H	XX	169
FBB	DMA1 Start Address Low Byte	DMA1START	XX	170
FBC	DMA1 End Address Low Byte	DMA1END	XX	170
DMA ADC				
FBD	DMA_ADC Address	DMAA_ADDR	XX	171
FBE	DMA_ADC Control	DMAACTL	00	172
FBF	DMA_ADC Status	DMAASTAT	00	173
Interrupt Controller				
FC0	Interrupt Request 0	IRQ0	00	71
FC1	IRQ0 Enable High Bit	IRQ0ENH	00	74
FC2	IRQ0 Enable Low Bit	IRQ0ENL	00	74
FC3	Interrupt Request 1	IRQ1	00	72
FC4	IRQ1 Enable High Bit	IRQ1ENH	00	75
FC5	IRQ1 Enable Low Bit	IRQ1ENL	00	75
FC6	Interrupt Request 2	IRQ2	00	73
FC7	IRQ2 Enable High Bit	IRQ2ENH	00	76
FC8	IRQ2 Enable Low Bit	IRQ2ENL	00	76
FC9-FCC	Reserved	—	XX	

SPI Data
SPIDATA (F60H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

SPI Data [7:0]

SPI Control
SPICTL (F61H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

SPI Enable
0 = SPI disabled
1 = SPI enabled

Master Mode Enabled
0 = SPI configured in Slave mode
1 = SPI configured in Master mode

Wire-OR (open-drain) Mode
0 = SPI signals not configured for open-drain
1 = SPI signals (SCK, $\overline{SS}$, MISO, and MOSI) configured for open-drain

Clock Polarity
0 = SCK idles Low
1 = SPI idles High

Phase Select
Sets the phase relationship of the data to the clock.

BRG Timer Interrupt Request
0 = BRG timer function is disabled
1 = BRG time-out interrupt is enabled

Start an SPI Interrupt Request
0 = No effect
1 = Generate an SPI interrupt request

Interrupt Request Enable
0 = SPI interrupt requests are disabled
1 = SPI interrupt requests are enabled

SPI Status
SPISTAT (F62H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

Slave Select
0 = If Slave, $\overline{SS}$ pin is asserted
1 = If Slave, SS pin is not asserted

Transmit Status
0 = No data transmission in progress
1 = Data transmission now in progress

Reserved

Slave Mode Transaction Abort
0 = No slave mode transaction abort detected
1 = Slave mode transaction abort was detected

Collision
0 = No multi-master collision detected
1 = Multi-master collision was detected

Overrun
0 = No overrun error detected
1 = Overrun error was detected

Interrupt Request
0 = No SPI interrupt request pending
1 = SPI interrupt request is pending

SPI Mode
SPIMODE (F63H - Read/Write)

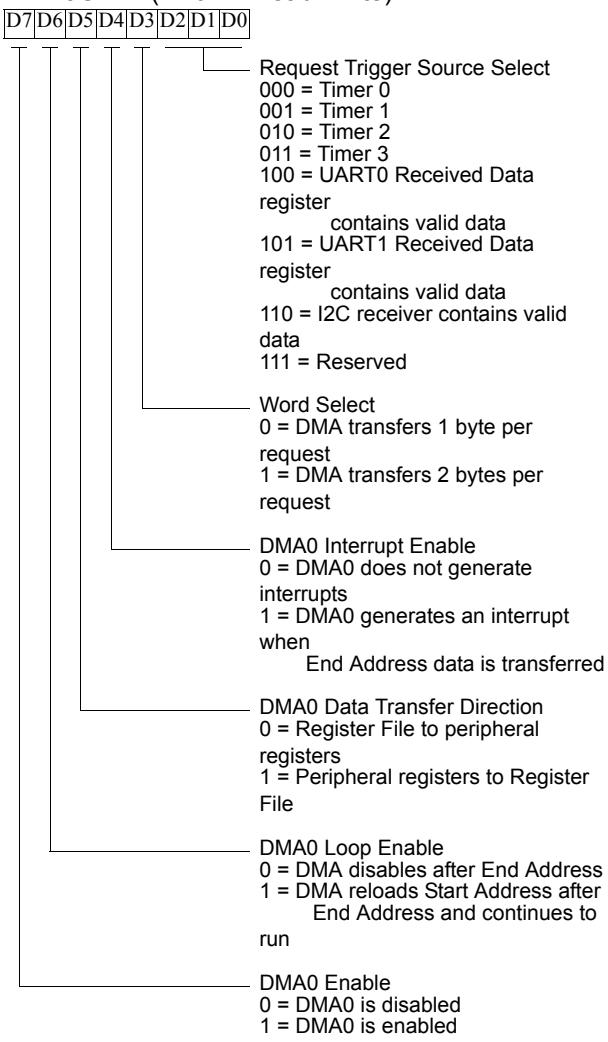
D7	D6	D5	D4	D3	D2	D1	D0

Slave Select Value
If Master and SPIMODE[1] = 1:
0 = $\overline{SS}$ pin driven Low
1 = SS pin driven High

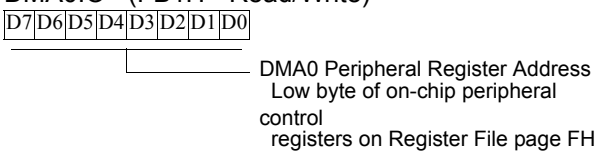
Slave Select I/O
0 = $\overline{SS}$ pin configured as an input
1 = SS pin configured as an output (Master mode only)

Number of Data Bits Per Character
000 = 8 bits
001 = 1 bit
010 = 2 bits
011 = 3 bits
100 = 4 bits
101 = 5 bit
110 = 6 bits

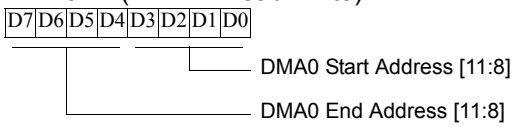
DMA0 Control
DMA0CTL (FB0H - Read/Write)



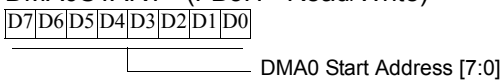
DMA0 I/O Address
DMA0IO (FB1H - Read/Write)



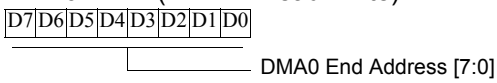
DMA0 Address High Nibble
DMA0H (FB2H - Read/Write)



DMA0 Start/Current Address Low Byte
DMA0START (FB3H - Read/Write)



DMA0 End Address Low Byte
DMA0END (FB4H - Read/Write)



DMA1 Control
DMA1CTL (FB8H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Request Trigger Source Select
000 = Timer 0
001 = Timer 1
010 = Timer 2
011 = Timer 3
100 = UART0 Transmit Data register is empty
101 = UART1 Transmit Data register is empty
110 = I2C Transmit Data register is empty
111 = Reserved

Word Select
0 = DMA transfers 1 byte per request
1 = DMA transfers 2 bytes per request

DMA1 Interrupt Enable
0 = DMA1 does not generate interrupts
1 = DMA1 generates an interrupt when End Address data is transferred

DMA1 Data Transfer Direction
0 = Register File to peripheral registers
1 = Peripheral registers to Register File

DMA1 Loop Enable
0 = DMA disables after End Address
1 = DMA reloads Start Address after End Address and continues to run

DMA1 Enable
0 = DMA1 is disabled
1 = DMA1 is enabled

DMA1 I/O Address
DMA1IO (FB9H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

DMA1 Peripheral Register Address
Low byte of on-chip peripheral control registers on Register File page FH

DMA1 Address High Nibble
DMA1H (FBAH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

DMA1 Start Address [11:8]

DMA1 End Address [11:8]

DMA1 Start/Current Address Low Byte
DMA1START (FBBH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

DMA1 Start Address [7:0]

DMA1 End Address Low Byte
DMA1END (FBCH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

DMA1 End Address [7:0]

DMA_ADC Address
DMAA_ADDR (FBDH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Reserved

DMA_ADC Address

Interrupt Port Select
IRQPS (FCEH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port A or D Port Pin Select [7:0]
0 = Port A pin is the interrupt source
1 = Port D pin is the interrupt source

Interrupt Control
IRQCTL (FCFH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Reserved

Interrupt Request Enable
0 = Interrupts are disabled
1 = Interrupts are enabled

Port A Address
PAADDR (FD0H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = Stop Mode Recovery enable
06H-FFH = No function

Port A Control
PACTL (FD1H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Control[7:0]
Provides Access to Port Sub-Registers

Port A Input Data
PAIN (FD2H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Input Data [7:0]

Port A Output Data
PAOUT (FD3H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Output Data [7:0]

Port B Address
PBADDR (FD4H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port B Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = Stop Mode Recovery enable
06H-FFH = No function

Port B Control
PBCTL (FD5H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port B Control[7:0]
Provides Access to Port Sub-Registers

Port B Input Data
PBIN (FD6H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

Port B Input Data [7:0]

Port B Output Data
PBOUT (FD7H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port B Output Data [7:0]

Port C Address
PCADDR (FD8H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port C Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = Stop Mode Recovery enable
06H-FFH = No function

Watchdog Timer Control
WDTCTL (FF0H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: SM Configuration Indicator
- D1: Reserved
- D2: EXT
  0 = Reset not generated by $\overline{\text{RESET}}$ pin
  1 = Reset generated by $\overline{\text{RESET}}$ pin
- D3: WDT
  0 = WDT timeout has not occurred
  1 = WDT timeout occurred
- D4: STOP
  0 = SMR has not occurred
  1 = SMR has occurred
- D5: POR
  0 = POR has not occurred
  1 = POR has occurred

Watchdog Timer Reload Upper Byte
WDTU (FF1H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: WDT reload value [23:16]

Watchdog Timer Reload Middle Byte
WDTH (FF2 H- Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: WDT reload value [15:8]

Watchdog Timer Reload Low Byte
WDTL (FF3H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: WDT reload value [7:0]

Flash Control
FCTL (FF8H - Write Only)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: Flash Command
  73H = First unlock command
  8CH = Second unlock command
  95H = Page erase command
  63H = Mass erase command
  5EH = Flash Sector Protect reg select

Flash Status
FSTAT (FF8H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D3: Flash Controller Status
  00_0000 = Flash controller locked
  00_0001 = First unlock received
  00_0010 = Second unlock received
  00_0011 = Flash controller unlocked
  00_0100 = Flash Sector Protect register selected
  00_1xxx = Programming in progress
  01_0xxx = Page erase in progress
  10_0xxx = Mass erase in progress
- D4–D6: Reserved

Page Select
FPS (FF9H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D6: Page Select [6:0]
  Identifies the Flash memory page for Page Erase operation.
- D7: Information Area Enable
  0 = Information Area access is disabled
  1 = Information Area access is enabled

Flash Sector Protect
FPROT (FF9H - Read/Write to 1's)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: Flash Sector Protect [7:0]
  0 = Sector can be programmed or erased from user code
  1 = Sector is protected and cannot be programmed or erased from user code

Flash Frequency High Byte
FFREQH (FFAH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: Flash Frequency value [15:8]

Flash Frequency Low Byte
FFREQL (FFBH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: Flash Frequency value [7:0]

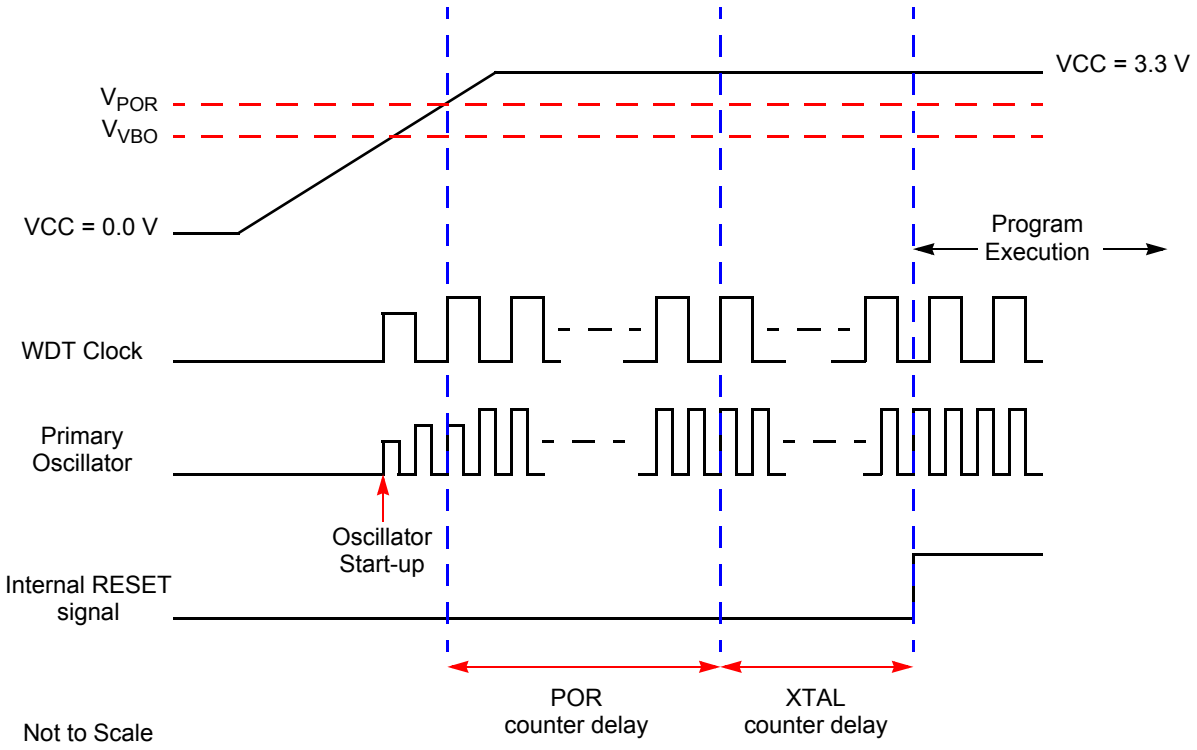


Figure 8. Power-On Reset Operation

Voltage Brownout Reset

The devices in the 64K Series provide low Voltage Brownout protection. The VBO circuit senses when the supply voltage drops to an unsafe level (below the VBO threshold voltage) and forces the device into the Reset state. While the supply voltage remains below the Power-On Reset voltage threshold (V_{POR}), the VBO block holds the device in the Reset state.

After the supply voltage again exceeds the Power-On Reset voltage threshold, the devices progress through a full system reset sequence, as described in the Power-On Reset section. Following Power-On Reset, the POR status bit in the Watchdog Timer Control (WDTCTL) register is set to 1. Figure 9 displays Voltage Brownout operation. For the VBO and POR threshold voltages (V_{VBO} and V_{POR}), see Electrical Characteristics on page 215.

The Voltage Brownout circuit can be either enabled or disabled during STOP mode. Operation during STOP mode is set by the VBO_A0 Option Bit. For information on configuring VBO_A0, see Option Bits page 195.

PAD*x*I—Port A or Port D Pin *x* Interrupt Request
0 = No interrupt request is pending for GPIO Port A or Port D pin *x*.
1 = An interrupt request from GPIO Port A or Port D pin *x* is awaiting service.

where *x* indicates the specific GPIO Port pin number (0 through 7). For each pin, only 1 of either Port A or Port D can be enabled for interrupts at any one time. Port selection (A or D) is determined by the values in the Interrupt Port Select Register.

Interrupt Request 2 Register

The Interrupt Request 2 (IRQ2) register (Table 26) stores interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ2 register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 1 register to determine if any interrupt requests are pending.

Table 26. Interrupt Request 2 Register (IRQ2)

BITS	7	6	5	4	3	2	1	0
FIELD	T3I	U1RXI	U1TXI	DMAI	PC3I	PC2I	PC1I	PC0I
RESET	0							
R/W	R/W							
ADDR	FC6H							

T3I—Timer 3 Interrupt Request
0 = No interrupt request is pending for Timer 3.
1 = An interrupt request from Timer 3 is awaiting service.

U1RXI—UART 1 Receive Interrupt Request
0 = No interrupt request is pending for the UART1 receiver.
1 = An interrupt request from UART1 receiver is awaiting service.

U1TXI—UART 1 Transmit Interrupt Request
0 = No interrupt request is pending for the UART 1 transmitter.
1 = An interrupt request from the UART 1 transmitter is awaiting service.

DMAI—DMA Interrupt Request
0 = No interrupt request is pending for the DMA.
1 = An interrupt request from the DMA is awaiting service.

PC*x*I—Port C Pin *x* Interrupt Request
0 = No interrupt request is pending for GPIO Port C pin *x*.
1 = An interrupt request from GPIO Port C pin *x* is awaiting service.

One-Shot time-out, first set the TPOL bit in the Timer Control 1 Register to the start value before beginning ONE-SHOT mode. Then, after starting the timer, set TPOL to the opposite bit value.

Follow the steps below for configuring a timer for ONE-SHOT mode and initiating the count:

1. Write to the Timer Control 1 register to:
   – Disable the timer
   – Configure the timer for ONE-SHOT mode
   – Set the prescale value
   – If using the Timer Output alternate function, set the initial output level (High or Low)
2. Write to the Timer High and Low Byte registers to set the starting count value
3. Write to the Timer Reload High and Low Byte registers to set the Reload value
4. If desired, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers
5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function
6. Write to the Timer Control 1 register to enable the timer and initiate counting

In ONE-SHOT mode, the system clock always provides the timer input. The timer period is given by the following equation:

$$\text{ONE-SHOT Mode Time-Out Period (s)} = \frac{(\text{Reload Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

CONTINUOUS Mode

In CONTINUOUS mode, the timer counts up to the 16-bit Reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) upon timer Reload.

Follow the steps below for configuring a timer for CONTINUOUS mode and initiating the count:

1. Write to the Timer Control 1 register to:
   – Disable the timer
   – Configure the timer for CONTINUOUS mode
   – Set the prescale value
   – If using the Timer Output alternate function, set the initial output level (High or Low)

Follow the steps below for configuring a timer for PWM mode and initiating the PWM operation:

1. Write to the Timer Control 1 register to:
   - Disable the timer
   - Configure the timer for PWM mode
   - Set the prescale value
   - Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of 0001H.
3. Write to the PWM High and Low Byte registers to set the PWM value.
4. Write to the Timer Reload High and Low Byte registers to set the Reload value (PWM period). The Reload value must be greater than the PWM value.
5. If desired, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
6. Configure the associated GPIO port pin for the Timer Output alternate function.
7. Write to the Timer Control 1 register to enable the timer and initiate counting.

The PWM period is given by the following equation:

$$\text{PWM Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, the ONE-SHOT mode equation must be used to determine the first PWM time-out period.

If TPOL is set to 0, the ratio of the PWM output High time to the total period is given by:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is given by:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{PWM Value}}{\text{Reload Value}} \times 100$$

CAPTURE Mode

In CAPTURE mode, the current timer count value is recorded when the desired external Timer Input transition occurs. The Capture count value is written to the Timer PWM High and Low Byte Registers. The timer input is the system clock. The TPOL bit in the Timer Control 1 register determines if the Capture occurs on a rising edge or a falling edge of the Timer Input signal. When the Capture event occurs, an interrupt is generated and the timer continues counting.

110 = Divide by 64
111 = Divide by 128

TMODE—TIMER mode
000 = ONE-SHOT mode
001 = CONTINUOUS mode
010 = COUNTER mode
011 = PWM mode
100 = CAPTURE mode
101 = COMPARE mode
110 = GATED mode
111 = CAPTURE/COMPARE mode

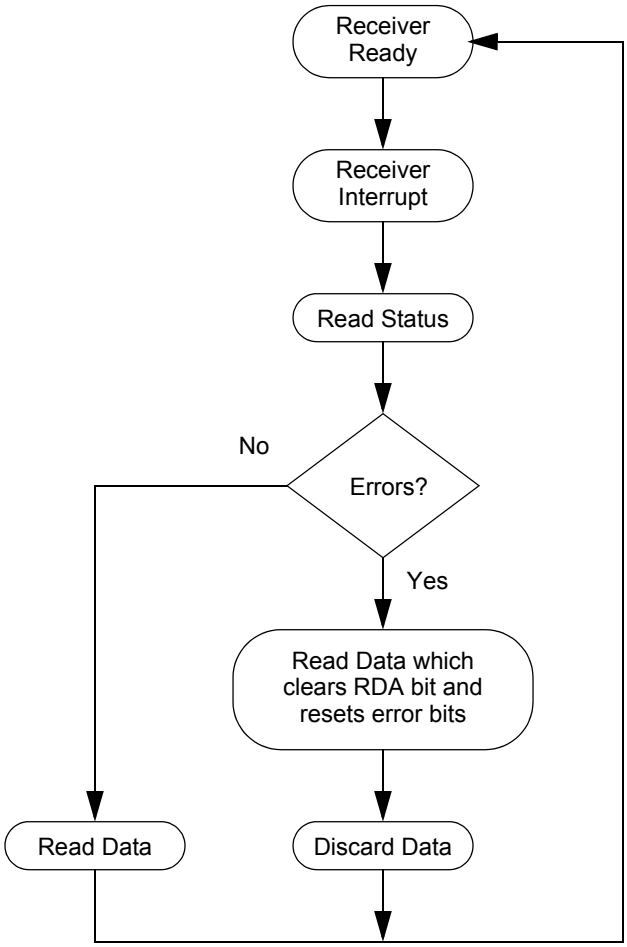


Figure 18. UART Receiver Interrupt Service Routine Flow

Baud Rate Generator Interrupts

If the Baud Rate Generator interrupt enable is set, the UART Receiver interrupt asserts when the UART Baud Rate Generator reloads. This action allows the Baud Rate Generator to function as an additional counter if the UART functionality is not employed.

UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value

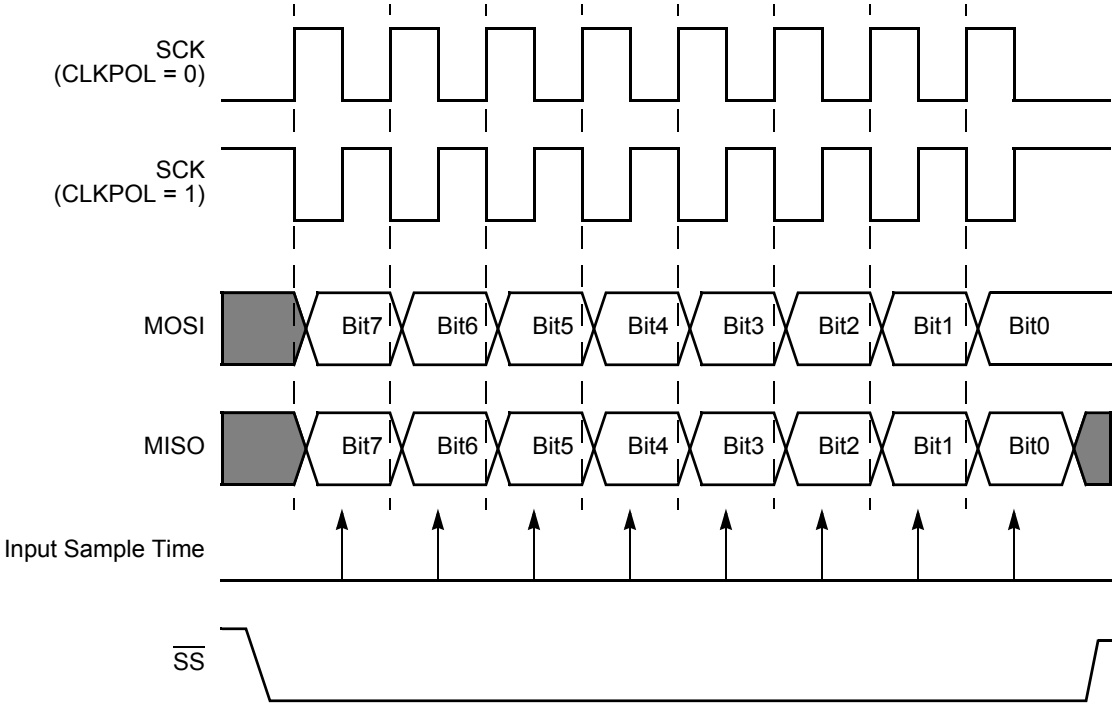


Figure 26. SPI Timing When PHASE **is 1**

Multi-Master Operation

In a multi-master SPI system, all SCK pins are tied together, all MOSI pins are tied together and all MISO pins are tied together. All SPI pins must then be configured in OPEN-DRAIN mode to prevent bus contention. At any one time, only one SPI device is configured as the Master and all other SPI devices on the bus are configured as Slaves. The Master enables a single Slave by asserting the $\overline{SS}$ pin on that Slave only. Then, the single Master drives data out its SCK and MOSI pins to the SCK and MOSI pins on the Slaves (including those which are not enabled). The enabled Slave drives data out its MISO pin to the MISO Master pin.

For a Master device operating in a multi-master system, if the $\overline{SS}$ pin is configured as an input and is driven Low by another Master, the COL bit is set to 1 in the SPI Status Register. The COL bit indicates the occurrence of a multi-master collision (mode fault error condition).

Slave Operation

The SPI block is configured for SLAVE mode operation by setting the SPIEN bit to 1 and the MMEN bit to 0 in the SPICTL register and setting the SSIO bit to 0 in the SPIMODE

register. The IRQE, PHASE, CLKPOL, WOR bits in the SPICTL register and the NUMBITS field in the SPIMODE register must be set to be consistent with the other SPI devices. The STR bit in the SPICTL register may be used if desired to force a "startup" interrupt. The BIRQ bit in the SPICTL register and the SSV bit in the SPIMODE register are not used in SLAVE mode. The SPI baud rate generator is not used in SLAVE mode so the SPIBRH and SPIBRL registers need not be initialized.

If the slave has data to send to the master, the data must be written to the SPIDAT register before the transaction starts (first edge of SCK when $\overline{SS}$ is asserted). If the SPIDAT register is not written prior to the slave transaction, the MISO pin outputs whatever value is currently in the SPIDAT register.

Due to the delay resulting from synchronization of the SPI input signals to the internal system clock, the maximum SPICLK baud rate that can be supported in SLAVE mode is the system clock frequency (XIN) divided by 8. This rate is controlled by the SPI master.

Error Detection

The SPI contains error detection logic to support SPI communication protocols and recognize when communication errors have occurred. The SPI Status register indicates when a data transmission error has been detected.

Overrun (Write Collision)

An overrun error (write collision) indicates a write to the SPI Data register was attempted while a data transfer is in progress (in either MASTER or SLAVE modes). An overrun sets the OVR bit in the SPI Status register to 1. Writing a 1 to OVR clears this error Flag. The data register is not altered when a write occurs while data transfer is in progress.

Mode Fault (Multi-Master Collision)

A mode fault indicates when more than one Master is trying to communicate at the same time (a multi-master collision). The mode fault is detected when the enabled Master's $\overline{SS}$ pin is asserted. A mode fault sets the COL bit in the SPI Status register to 1. Writing a 1 to COL clears this error Flag.

Slave Mode Abort

In SLAVE mode of operation if the $\overline{SS}$ pin deasserts before all bits in a character have been transferred, the transaction is aborted. When this condition occurs the ABT bit is set in the SPISTAT register as well as the IRQ bit (indicating the transaction is complete). The next time $\overline{SS}$ asserts, the MISO pin outputs SPIDAT[7], regardless of where the previous transaction left off. Writing a 1 to ABT clears this error Flag.

SPI Interrupts

When SPI interrupts are enabled, the SPI generates an interrupt after character transmission/reception completes in both MASTER and SLAVE modes. A character can be

DMA_ADC Address Register

The DMA_ADC Address register (Table 83) points to a block of the Register File to store ADC conversion values as displayed in Table 82. This register contains the seven most-significant bits of the 12-bit Register File addresses. The five least-significant bits are calculated from the ADC Analog Input number (5-bit base address is equal to twice the ADC Analog Input number). The 10-bit ADC conversion data is stored as two bytes with the most significant byte of the ADC data stored at the even numbered Register File address.

Table 82 provides an example of the Register File addresses if the DMA_ADC Address register contains the value 72H.

Table 82. DMA_ADC Register File Address Example

ADC Analog Input	Register File Address (Hex)[1]
0	720H-721H
1	722H-723H
2	724H-725H
3	726H-727H
4	728H-729H
5	72AH-72BH
6	72CH-72DH
7	72EH-72FH
8	730H-731H
9	732H-733H
10	734H-735H
11	736H-737H

[1]DMAA_ADDR set to 72H.

Table 83. DMA_ADC Address Register (DMAA_ADDR)

BITS	7	6	5	4	3	2	1	0
FIELD	DMAA_ADDR							Reserved
RESET	X							
R/W	R/W							
ADDR	FBDH							

Table 123. Additional Symbols

Symbol	Definition
dst	Destination Operand
src	Source Operand
@	Indirect Address Prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flags Register
RP	Register Pointer
#	Immediate Operand Prefix
B	Binary Number Suffix
%	Hexadecimal Number Prefix
H	Hexadecimal Number Suffix

Assignment of a value is indicated by an arrow. For example,

dst ← dst + src

indicates the source data is added to the destination data and the result is stored in the destination location.

Condition Codes

The C, Z, S and V Flags control the operation of the conditional jump (JP cc and JR cc) instructions. Sixteen frequently useful functions of the Flag settings are encoded in a 4-bit field called the condition code (cc), which forms Bits 7:4 of the conditional jump instructions. The condition codes are summarized in Table 124. Some binary condition codes can be created using more than one assembly code mnemonic. The result of the Flag test operation decides if the conditional jump is executed.

Table 124. Condition Codes

Binary	Hex	Assembly Mnemonic	Definition	Flag Test Operation
0000	0	F	Always False	–
0001	1	LT	Less Than	(S XOR V) = 1
0010	2	LE	Less Than or Equal	(Z OR (S XOR V)) = 1

Opcode Maps

A description of the opcode map data and the abbreviations are provided in Figure 59 and Table 134 on page 262. Figure 60 on page 263 and Figure 61 on page 264 provide information on each of the eZ8™ CPU instructions.

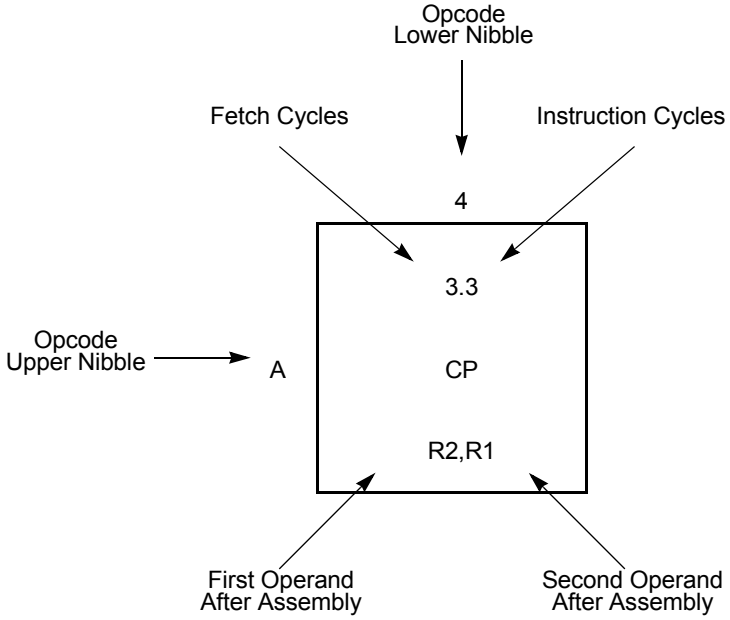


Figure 59. Opcode Map Cell Description

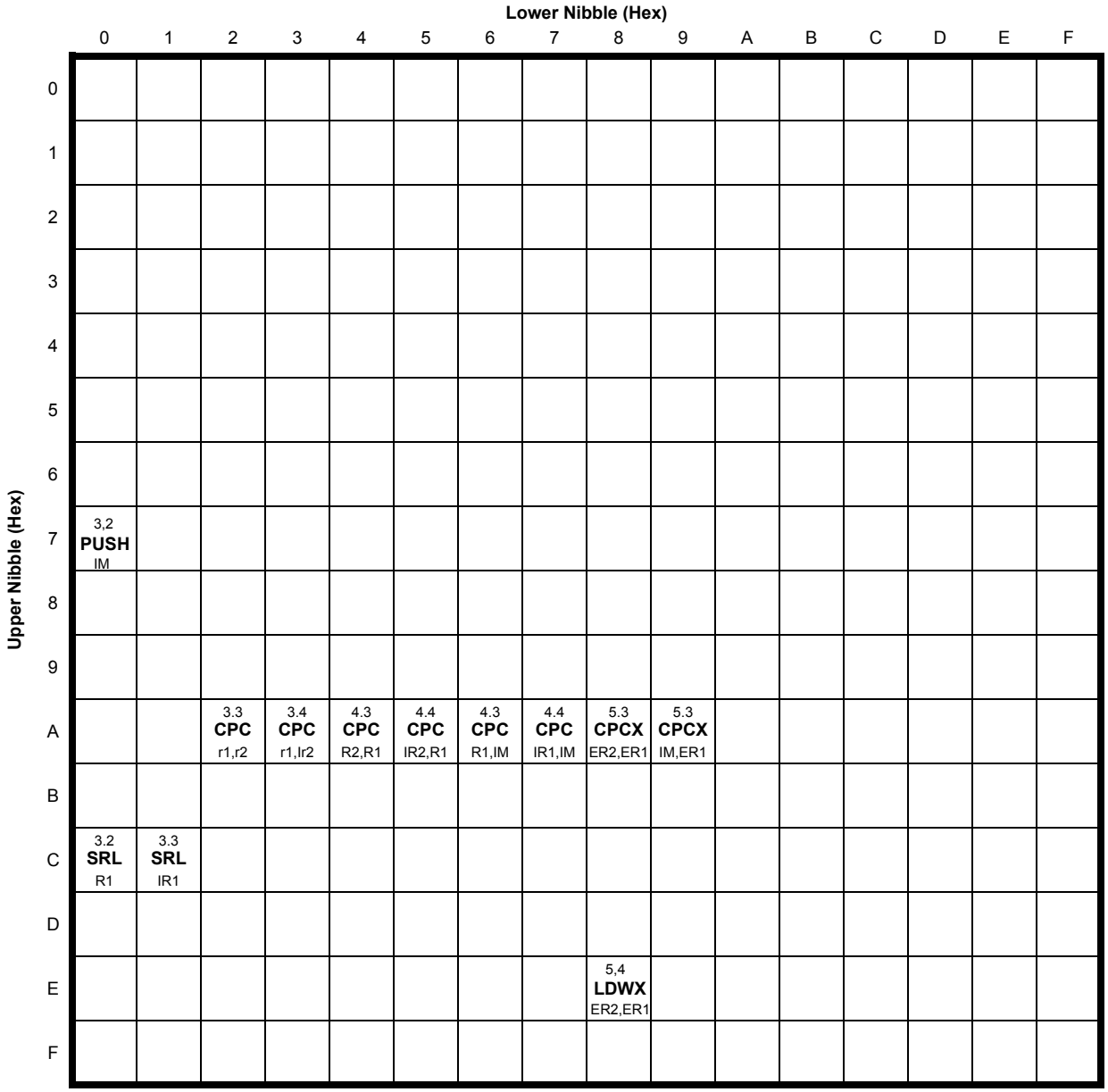


Figure 61. Second Opcode Map after 1FH

F

G

H

I