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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Detail	s
--------	---

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	46
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f3222vs020ec00tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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# Figure 5. Z8 Encore! XP 64K Series Flash Microcontrollers in 64-Pin Low-Profile Quad Flat Package (LQFP)





Figure 7. Z8 Encore! XP 64K Series Flash Microcontrollers in 80-Pin Quad Flat Package (QFP)

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#### SPI Baud Rate Generator Low Byte SPIBRL (F67H - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0

\_\_\_\_\_ SPI Baud Rate divisor [7:0]

ADCD\_L (F73H - Read Only) D7D6D5D4D3D2D1D0 \_\_\_\_\_

Reserved

\_\_\_\_\_ ADC Data [1:0]



#### **Operating Mode Reset Source Reset Type** NORMAL or HALT Power-On Reset/Voltage system reset modes Brownout Watchdog Timer time-out system reset when configured for Reset RESET pin assertion system reset On-Chip Debugger initiated Reset system reset except the On-Chip Debugger is (OCDCTL[0] set to 1) unaffected by the reset Power-On Reset/Voltage STOP mode system reset Brownout **RESET** pin assertion system reset DBG pin driven Low system reset

#### Table 9. Reset Sources and Resulting Reset Type

### **Power-On Reset**

Each device in the 64K Series contains an internal Power-On Reset circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold ( $V_{POR}$ ), the POR Counter is enabled and counts 66 cycles of the Watchdog Timer oscillator. After the POR counter times out, the XTAL Counter is enabled to count a total of 16 system clock pulses. The devices are held in the Reset state until both the POR Counter and XTAL counter have timed out. After the 64K Series devices exit the Power-On Reset state, the eZ8 CPU fetches the Reset vector. Following Power-On Reset, the POR status bit in the Watchdog Timer Control (WDTCTL) register is set to 1.

Figure 8 displays Power-On Reset operation. For the POR threshold voltage ( $V_{POR}$ ), see Electrical Characteristics on page 215.



T1I—Timer 1 Interrupt Request

0 = No interrupt request is pending for Timer 1.

1 = An interrupt request from Timer 1 is awaiting service.

T0I—Timer 0 Interrupt Request

0 = No interrupt request is pending for Timer 0.

1 = An interrupt request from Timer 0 is awaiting service.

U0RXI—UART 0 Receiver Interrupt Request

0 = No interrupt request is pending for the UART 0 receiver.

1 = An interrupt request from the UART 0 receiver is awaiting service.

U0TXI-UART 0 Transmitter Interrupt Request

0 = No interrupt request is pending for the UART 0 transmitter.

1 = An interrupt request from the UART 0 transmitter is awaiting service.

I<sup>2</sup>CI— I<sup>2</sup>C Interrupt Request

0 = No interrupt request is pending for the I<sup>2</sup>C.

1 = An interrupt request from the I<sup>2</sup>C is awaiting service.

SPII—SPI Interrupt Request

0 = No interrupt request is pending for the SPI.

1 = An interrupt request from the SPI is awaiting service.

ADCI—ADC Interrupt Request

0 = No interrupt request is pending for the Analog-to-Digital Converter.

1 = An interrupt request from the Analog-to-Digital Converter is awaiting service.

# Interrupt Request 1 Register

The Interrupt Request 1 (IRQ1) register (Table 25) stores interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ1 register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 1 register to determine if any interrupt requests are pending.

BITS	7	6	5	4	3	2	1	0	
FIELD	PAD7I	PAD6I	PAD5I	PAD4I	PAD3I	PAD2I	PAD1I	PAD0I	
RESET	0								
R/W		R/W							
ADDR	FC3H								

Table 25.	Interrupt	<b>Request 1</b>	Register	(IRQ1)
-----------	-----------	------------------	----------	--------

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5. Write the Watchdog Timer Reload Low Byte register (WDTL).

All steps of the Watchdog Timer Reload Unlock sequence must be written in the order just listed. There must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur, unless the sequence is restarted. The value in the Watchdog Timer Reload registers is loaded into the counter when the Watchdog Timer is first enabled and every time a WDT instruction is executed.

# Watchdog Timer Control Register Definitions

# Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) register (Table 48) is a Read-Only register that indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event, and indicates a Watchdog Timer time-out. Reading this register resets the upper four bits to 0.

Writing the 55H, AAH unlock sequence to the Watchdog Timer Control (WDTCTL) register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers.

BITS	7	6	5	4	3	2	1	0		
FIELD	POR	STOP	WDT	EXT		Reserved				
RESET	See c	lescriptions	below							
R/W		R								
ADDR				FF	0H					

Table 48. Watc	hdog Timer Con	trol Register (WDTCTL)	)
----------------	----------------	------------------------	---

Reset or Stop Mode Recovery Event	POR	STOP	WDT	EXT
Power-On Reset	1	0	0	0
Reset using RESET pin assertion	0	0	0	1
Reset using Watchdog Timer time-out	0	0	1	0
Reset using the On-Chip Debugger (OCDCTL[1] set to 1)	1	0	0	0
Reset from STOP Mode using DBG Pin driven Low	1	0	0	0
Stop Mode Recovery using GPIO pin transition	0	1	0	0
Stop Mode Recovery using Watchdog Timer time-out	0	1	1	0

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# Table 59. UART Baud Rate High Byte Register (UxBRH)

BITS	7	6	5	4	3	2	1	0		
FIELD	BRH									
RESET		1								
R/W		R/W								
ADDR		F46H and F4EH								

# Table 60. UART Baud Rate Low Byte Register (UxBRL)

BITS	7	6	5	4	3	2	1	0		
FIELD	BRL									
RESET	1									
R/W		R/W								
ADDR				F47H ar	nd F4FH					

For a given UART data rate, the integer baud rate divisor value is calculated using the following equation:

UART Baud Rate Divisor Value (BRG) =  $Round\left(\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Data Rate (bits/s)}}\right)$ 

The baud rate error relative to the desired baud rate is calculated using the following equation:

UART Baud Rate Error (%) =  $100 \times \left(\frac{\text{Actual Data Rate} - \text{Desired Data Rate}}{\text{Desired Data Rate}}\right)$ 

For reliable communication, the UART baud rate error must never exceed 5 percent. Table 61 provides information on data rate errors for popular baud rates and commonly used crystal oscillator frequencies.



# Operation

When the Infrared Endec is enabled, the transmit data from the associated on-chip UART is encoded as digital signals in accordance with the IrDA standard and output to the infrared transceiver via the TXD pin. Likewise, data received from the infrared transceiver is passed to the Infrared Endec via the RXD pin, decoded by the Infrared Endec, and then passed to the UART. Communication is half-duplex, which means simultaneous data transmission and reception is not allowed.

The baud rate is set by the UART's Baud Rate Generator and supports IrDA standard baud rates from 9600 baud to 115.2 Kbaud. Higher baud rates are possible, but do not meet IrDA specifications. The UART must be enabled to use the Infrared Endec. The Infrared Endec data rate is calculated using the following equation:

frared Data Rate (hite/s)	_	System Clock Frequency (Hz)
Initiated Data Rate (bits/s)	_	16 × UART Baud Rate Divisor Value

# **Transmitting IrDA Data**

The data to be transmitted using the infrared transceiver is first sent to the UART. The UART's transmit signal (TXD) and baud rate clock are used by the IrDA to generate the modulation signal (IR\_TXD) that drives the infrared transceiver. Each UART/Infrared data bit is 16-clock wide. If the data to be transmitted is 1, the IR\_TXD signal remains low for the full 16-clock period. If the data to be transmitted is 0, a 3-clock high pulse is output following a 7-clock low period. After the 3-clock high pulse, a 6-clock low pulse is output to complete the full 16-clock data period. Figure 20 displays IrDA data transmission. When the Infrared Endec is enabled, the UART's TXD signal is internal to the 64K Series products while the IR\_TXD signal is output through the TXD pin.







Table 64. SPI Control Register (SPICTL)

BITS	7	6	5	4	3	2	1	0			
FIELD	IRQE	STR	BIRQ	PHASE	CLKPOL	WOR	MMEN	SPIEN			
RESET		0									
R/W		R/W									
ADDR				F6	1H						

IRQE—Interrupt Request Enable

0 = SPI interrupts are disabled. No interrupt requests are sent to the Interrupt Controller.

1 = SPI interrupts are enabled. Interrupt requests are sent to the Interrupt Controller.

STR—Start an SPI Interrupt Request

0 = No effect.

1 = Setting this bit to 1 also sets the IRQ bit in the SPI Status register to 1. Setting this bit forces the SPI to send an interrupt request to the Interrupt Control. This bit can be used by software for a function similar to transmit buffer empty in a UART. Writing a 1 to the IRQ bit in the SPI Status register clears this bit to 0.

BIRQ-BRG Timer Interrupt Request

If the SPI is enabled, this bit has no effect. If the SPI is disabled:

0 = The Baud Rate Generator timer function is disabled.

1 = The Baud Rate Generator timer function and time-out interrupt are enabled.

PHASE—Phase Select

Sets the phase relationship of the data to the clock. For more information on operation of the PHASE bit, see SPI Clock Phase and Polarity Control on page 132.

CLKPOL—Clock Polarity

0 = SCK idles Low (0).

1 = SCK idle High (1).

WOR-Wire-OR (OPEN-DRAIN) Mode Enabled

0 = SPI signal pins not configured for open-drain.

 $1 = \text{All four SPI signal pins (SCK, \overline{SS}, MISO, MOSI)}$  configured for open-drain function. This setting is typically used for multi-master and/or multi-slave configurations.

MMEN—SPI Master Mode Enable

0 = SPI configured in Slave mode.

1 = SPI configured in Master mode.

SPIEN—SPI Enable

0 = SPI disabled.

1 = SPI enabled.



Transmit interrupts occur when the TDRE bit of the  $I^2C$  Status register sets and the TXI bit in the  $I^2C$  Control register is set. Transmit interrupts occur under the following conditions when the transmit data register is empty:

- The I<sup>2</sup>C Controller is enabled.
- The first bit of the byte of an address is shifting out and the RD bit of the I<sup>2</sup>C Status register is deasserted.
- The first bit of a 10-bit address shifts out.
- The first bit of write data shifts out.

**Note:** Writing to the  $l^2C$  Data register always clears the TRDE bit to 0. When TDRE is asserted, the  $l^2C$  Controller pauses at the beginning of the Acknowledge cycle of the byte currently shifting out until the Data register is written with the next value to send or the STOP or START bits are set indicating the current byte is the last one to send.

The fourth interrupt source is the baud rate generator. If the I<sup>2</sup>C Controller is disabled (IEN bit in the I2CCTL register = 0) and the BIRQ bit in the I2CCTL register = 1, an interrupt is generated when the baud rate generator counts down to 1. This allows the I<sup>2</sup>C baud rate generator to be used by software as a general purpose timer when IEN = 0.

# Software Control of I<sup>2</sup>C Transactions

Software can control  $I^2C$  transactions by using the  $I^2C$  Controller interrupt, by polling the  $I^2C$  Status register or by DMA. Note that not all products include a DMA Controller.

To use interrupts, the  $I^2C$  interrupt must be enabled in the Interrupt Controller. The TXI bit in the  $I^2C$  Control register must be set to enable transmit interrupts.

To control transactions by polling, the interrupt bits (TDRE, RDRF and NCKI) in the I<sup>2</sup>C Status register should be polled. The TDRE bit asserts regardless of the state of the TXI bit.

Either or both transmit and receive data movement can be controlled by the DMA Controller. The DMA Controller channel(s) must be initialized to select the I<sup>2</sup>C transmit and receive requests. Transmit DMA requests require that the TXI bit in the I<sup>2</sup>C Control register be set.



**Caution:** A transmit (write) DMA operation hangs if the slave responds with a Not Acknowledge before the last byte has been sent. After receiving the Not Acknowledge, the I<sup>2</sup>C Controller sets the NCKI bit in the Status register and pauses until either the STOP or START bits in the Control register are set.



# Table 70. I<sup>2</sup>C Data Register (I2CDATA)

BITS	7	6	5 4 3 2 1 0										
FIELD				DA	TA								
RESET	0												
R/W		R/W											
ADDR		F50H											

# I<sup>2</sup>C Status Register

The Read-only I<sup>2</sup>C Status register (Table 71) indicates the status of the I<sup>2</sup>C Controller.

Table 71	. I <sup>2</sup> C	Status	Register	(I2CSTAT)	)
----------	--------------------	--------	----------	-----------	---

BITS	7	6	5	4	3	2	1	0		
FIELD	TDRE	RDRF	ACK	10B	RD	TAS	DSS	NCKI		
RESET	1	0								
R/W		R								
ADDR				F5	1H					

### TDRE—Transmit Data Register Empty

When the I<sup>2</sup>C Controller is enabled, this bit is 1 when the I<sup>2</sup>C Data register is empty. When this bit is set, an interrupt is generated if the TXI bit is set, except when the I<sup>2</sup>C Controller is shifting in data during the reception of a byte or when shifting an address and the RD bit is set. This bit is cleared by writing to the I2CDATA register.

#### RDRF—Receive Data Register Full

This bit is set = 1 when the I<sup>2</sup>C Controller is enabled and the I<sup>2</sup>C Controller has received a byte of data. When asserted, this bit causes the I<sup>2</sup>C Controller to generate an interrupt. This bit is cleared by reading the I<sup>2</sup>C Data register (unless the read is performed using execution of the On-Chip Debugger's Read Register command).

#### ACK—Acknowledge

This bit indicates the status of the Acknowledge for the last byte transmitted or received. When set, this bit indicates that an Acknowledge occurred for the last byte transmitted or received. This bit is cleared when IEN = 0 or when a Not Acknowledge occurred for the last byte transmitted or received. It is not reset at the beginning of each transaction and is not reset when this register is read.



# **On-Chip Debugger Control Register Definitions**

# **OCD Control Register**

The OCD Control register (Table 102) controls the state of the On-Chip Debugger. This register enters or exits DEBUG mode and enables the BRK instruction. It can also reset the Z8F642x family, Z8R642x family device.

A 'reset and stop' function can be achieved by writing 81H to this register. A 'reset and go' function can be achieved by writing 41H to this register. If the device is in DEBUG mode, a 'run' function can be implemented by writing 40H to this register.

Table 102. OCD Control Register (OCDCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	DBGMODE	BRKEN	DBGACK	BRKLOOP			Reserved	RST
RESET	0							
R/W		R/W			R			R/W

#### DBGMODE—DEBUG Mode

Setting this bit to 1 causes the device to enter DEBUG mode. When in DEBUG mode, the eZ8 CPU stops fetching new instructions. Clearing this bit causes the eZ8 CPU to start running again. This bit is automatically set when a BRK instruction is decoded and Breakpoints are enabled. If the Read Protect Option Bit is enabled, this bit can only be cleared by resetting the device, it cannot be written to 0.

0 = The 64K Series device is operating in NORMAL mode.

1 = The 64K Series device is in DEBUG mode.

#### BRKEN-Breakpoint Enable

This bit controls the behavior of the BRK instruction (opcode 00H). By default, Breakpoints are disabled and the BRK instruction behaves like a NOP. If this bit is set to 1 and a BRK instruction is decoded, the OCD takes action dependent upon the BRKLOOP bit.

- 0 = BRK instruction is disabled.
- 1 = BRK instruction is enabled.

#### DBGACK—Debug Acknowledge

This bit enables the debug acknowledge feature. If this bit is set to 1, then the OCD sends an Debug Acknowledge character (FFH) to the host when a Breakpoint occurs.

0 = Debug Acknowledge is disabled.

1 = Debug Acknowledge is enabled.

#### BRKLOOP—Breakpoint Loop

This bit determines what action the OCD takes when a BRK instruction is decoded if breakpoints are enabled (BRKEN is 1). If this bit is 0, then the DBGMODE bit is automatically set to 1 and the OCD entered DEBUG mode. If BRKLOOP is set to 1, then the

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Figure 43 displays the typical active mode current consumption while operating at 25 °C versus the system clock frequency. All GPIO pins are configured as outputs and driven High.



Figure 43. Typical Active Mode Idd Versus System Clock Frequency





# ADC Magnitude Transfer Function (Linear Scale)

Figure 49. Analog-to-Digital Converter Frequency Response



### Table 122. Notational Shorthand

Notation	Description	Operand	Range
b	Bit	b	b represents a value from 0 to 7 (000B to 111B).
СС	Condition Code	—	Refer to Condition Codes overview in the eZ8 CPU User Manual.
DA	Direct Address	Addrs	Addrs. represents a number in the range of 0000H to FFFFH
ER	Extended Addressing Register	Reg	Reg. represents a number in the range of 000H to FFFH
IM	Immediate Data	#Data	Data is a number between 00H to FFH
lr	Indirect Working Register	@Rn	n = 0 –15
IR	Indirect Register	@Reg	Reg. represents a number in the range of 00H to FFH
Irr	Indirect Working Register Pair	@RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14
IRR	Indirect Register Pair	@Reg	Reg. represents an even number in the range 00H to FEH
р	Polarity	р	Polarity is a single bit binary value of either 0B or 1B.
r	Working Register	Rn	n = 0 – 15
R	Register	Reg	Reg. represents a number in the range of 00H to FFH
RA	Relative Address	Х	X represents an index in the range of +127 to -128 which is an offset relative to the address of the next instruction
rr	Working Register Pair	RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14
RR	Register Pair	Reg	Reg. represents an even number in the range of 00H to FEH
Vector	Vector Address	Vector	Vector represents a number in the range of 00H to FFH
X	Indexed	#Index	The register or register pair to be indexed is offset by the signed Index value (#Index) in a +127 to -128 range.

Table 123 contains additional symbols that are used throughout the Instruction Summary and Instruction Set Description sections.



#### Table 123. Additional Symbols

Symbol	Definition
dst	Destination Operand
src	Source Operand
@	Indirect Address Prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flags Register
RP	Register Pointer
#	Immediate Operand Prefix
В	Binary Number Suffix
%	Hexadecimal Number Prefix
Н	Hexadecimal Number Suffix

Assignment of a value is indicated by an arrow. For example,

 $dst \leftarrow dst + src$ 

indicates the source data is added to the destination data and the result is stored in the destination location.

# **Condition Codes**

The C, Z, S and V Flags control the operation of the conditional jump (JP cc and JR cc) instructions. Sixteen frequently useful functions of the Flag settings are encoded in a 4-bit field called the condition code (cc), which forms Bits 7:4 of the conditional jump instructions. The condition codes are summarized in Table 124. Some binary condition codes can be created using more than one assembly code mnemonic. The result of the Flag test operation decides if the conditional jump is executed.

Binary	Hex	Assembly Mnemonic	Definition	Flag Test Operation
0000	0	F	Always False	-
0001	1	LT	Less Than	(S XOR V) = 1
0010	2	LE	Less Than or Equal	(Z OR (S XOR V)) = 1

#### Table 124. Condition Codes



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	-

Binary	Hex	Assembly Mnemonic	Definition	Flag Test Operation
0011	3	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0100	4	OV	Overflow	V = 1
0101	5	MI	Minus	S = 1
0110	6	Z	Zero	Z = 1
0110	6	EQ	Equal	Z = 1
0111	7	С	Carry	C = 1
0111	7	ULT	Unsigned Less Than	C = 1
1000	8	T (or blank)	Always True	-
1001	9	GE	Greater Than or Equal	(S XOR V) = 0
1010	А	GT	Greater Than	(Z OR (S XOR V)) = 0
1011	В	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
1100	С	NOV	No Overflow	V = 0
1101	D	PL	Plus	S = 0
1110	Е	NZ	Non-Zero	Z = 0
1110	Е	NE	Not Equal	Z = 0
1111	F	NC	No Carry	C = 0
1111	F	UGE	Unsigned Greater Than or Equal	C = 0

# Table 124. Condition Codes (Continued)

# eZ8 CPU Instruction Classes

eZ8 CPU instructions can be divided functionally into the following groups:

- Arithmetic
- Bit Manipulation
- Block Transfer
- CPU Control
- Load
- Logical
- Program Control
- Rotate and Shift



Assembly		Address Mode		- Opcode(s)	Flags						- Fetch	Instr
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	н	Cycles	Cycles
SWAP dst	$dst[7:4] \leftrightarrow dst[3:0]$	R		F0	Х	*	*	Х	-	-	2	2
		IR		F1	•						2	3
TCM dst, src	(NOT dst) AND src	r	r	62	-	*	*	0	-	-	2	3
	-	r	lr	63	•						2	4
	-	R	R	64	•						3	3
	-	R	IR	65	•						3	4
	-	R	IM	66	•						3	3
	-	IR	IM	67	•						3	4
TCMX dst, src	(NOT dst) AND src	ER	ER	68	-	*	*	0	-	-	4	3
	-	ER	IM	69	•						4	3
TM dst, src	dst AND src	r	r	72	-	*	*	0	-	-	2	3
		r	lr	73	•						2	4
	-	R	R	74	•						3	3
	-	R	IR	75	•						3	4
	-	R	IM	76	•						3	3
		IR	IM	77	•						3	4
TMX dst, src	dst AND src	ER	ER	78	-	*	*	0	-	-	4	3
	-	ER	IM	79	•						4	3
TRAP Vector	$SP \leftarrow SP - 2$ @SP \leftarrow PC SP \leftarrow SP - 1 @SP \leftarrow FLAGS PC \leftarrow @Vector		Vector	F2	-	-	-	-	-	-	2	6
WDT				5F	-	-	-	-	-	-	1	2

# Table 133. eZ8 CPU Instruction Summary (Continued)

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	Δ'	7	2

Lag Triped 725162x with 16 KB Elect	Flash Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	1 <sup>2</sup> C	SPI	UARTs with IrDA	Description
Standard Temperature: 0 °C	$\sim$ to 70 °C		-10-D	iyita		nven	lei			
78E1621PM020SC	16 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-nin nackade
Z8F1621ANI020SC	16 KB	2 KB	23	23	3	8	1	1	2	
Z01 102 TAIN020SC		2 10	21	20	3	0	1	1	2	PLCC 44 pin package
Z0F1021VIN0203C			31	23	3	10	1	1	2	
Z8F1622AR020SC			40	24	4	12		1	2	LQFP 64-pin package
28F1622VS020SC	16 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Extended lemperature: -4	0 °C to +	105 °C								
Z8F1621PM020EC	16 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F1621AN020EC	16 KB	2 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F1621VN020EC	16 KB	2 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F1622AR020EC	16 KB	2 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F1622VS020EC	16 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Automotive/Industrial Temp	erature:	–40 °C t	o +1	25 °C	2					
Z8F1621PM020AC	16 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F1621AN020AC	16 KB	2 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F1621VN020AC	16 KB	2 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F1622AR020AC	16 KB	2 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F1622VS020AC	16 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F64200100KITG										Development Kit
ZUSBSC00100ZACG										USB Smart Cable Accessory Kit
ZUSBOPTSC01ZACG										Opto-Isolated USB Smart Cable Accessory Kit
Note: Replace C with G for least	ad-free pa	ckaging.								