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Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f6421pm020ec

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Figure 6. Z8 Encore! XP 64K Series Flash Microcontrollers in 68-Pin Plastic Leaded Chip Carrier (PLCC)



Signal Descriptions

Table 3 describes the Z8 Encore! XP signals. To determine the signals available for the specific package styles, see Pin Configurations on page 8.

Table 3. Signal Descriptions

Signal Mnemonic	I/O	Description
General-Purpos	se I/O Port	s A-H
PA[7:0]	I/O	Port A[7:0]. These pins are used for general-purpose I/O and support 5 V-tolerant inputs.
PB[7:0]	I/O	Port B[7:0]. These pins are used for general-purpose I/O.
PC[7:0]	I/O	Port C[7:0]. These pins are used for general-purpose I/O. These pins are used for general-purpose I/O and support 5 V-tolerant inputs
PD[7:0]	I/O	Port D[7:0]. These pins are used for general-purpose I/O. These pins are used for general-purpose I/O and support 5 V-tolerant inputs
PE[7:0]	I/O	Port E[7:0]. These pins are used for general-purpose I/O. These pins are used for general-purpose I/O and support 5 V-tolerant inputs.
PF[7:0]	I/O	Port F[7:0]. These pins are used for general-purpose I/O. These pins are used for general-purpose I/O and support 5 V-tolerant inputs.
PG[7:0]	I/O	Port G[7:0]. These pins are used for general-purpose I/O. These pins are used for general-purpose I/O and support 5 V-tolerant inputs.
PH[3:0]	I/O	Port H[3:0]. These pins are used for general-purpose I/O.
I ² C Controller		
SCL	0	Serial Clock. This is the output clock for the I ² C. This pin is multiplexed with a general-purpose I/O pin. When the general-purpose I/O pin is configured for alternate function to enable the SCL function, this pin is open-drain.
SDA	I/O	Serial Data. This open-drain pin transfers data between the I^2C and a slave. This pin is multiplexed with a general-purpose I/O pin. When the general-purpose I/O pin is configured for alternate function to enable the SDA function, this pin is open-drain.
SPI Controller		
SS	I/O	Slave Select. This signal can be an output or an input. If the Z8 Encore! XP 64K Series Flash Microcontrollers is the SPI master, this pin may be configured as the Slave Select output. If the Z8 Encore! XP 64K Series Flash Microcontrollers is the SPI slave, this pin is the input slave select. It is multiplexed with a general-purpose I/O pin.

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Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tri-State Output	Internal Pull-up or Pull-down	Schmitt- Trigger Input	Open Drain Output
AVSS	N/A	N/A	N/A	N/A	No	No	N/A
AVDD	N/A	N/A	N/A	N/A	No	No	N/A
DBG	I/O	l	N/A	Yes	No	Yes	Yes
VSS	N/A	N/A	N/A	N/A	No	No	N/A
PA[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PB[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PC[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PD[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PE7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PF[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PG[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PH[3:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
RESET	I	I	Low	N/A	Pull-up	Yes	N/A
VDD	N/A	N/A	N/A	N/A	No	No	N/A
XIN	I	I	N/A	N/A	No	No	N/A
XOUT	0	0	N/A	Yes, in STOP mode	No	No	No

Table 4. Pin Characteristics of the Z8 Encore! XP 64K Series Flash Microcontrollers

Note: *x* represents integer 0, 1,... to indicate multiple pins with symbol mnemonics that differ only by the integer.



Program Memory Address (Hex)	Function				
0000-0001	Option Bits				
0002-0003	Reset Vector				
0004-0005	WDT Interrupt Vector				
0006-0007	Illegal Instruction Trap				
0008-0037	Interrupt Vectors*				
0038-BFFF	Program Memory				
Z8F642x Products					
0000-0001	Option Bits				
0002-0003	Reset Vector				
0004-0005	WDT Interrupt Vector				
0006-0007	Illegal Instruction Trap				
0008-0037	Interrupt Vectors*				
0038-FFFF	Program Memory				
*See Table 23 on page 68 for a list of th	ne interrupt vectors.				

Table 5. Z8 Encore! XP 64K Series Flash Microcontrollers Program Memory Maps (Continued)

Data Memory

The Z8 Encore! XP 64K Series Flash Microcontrollers does not use the eZ8 CPU's 64 KB Data Memory address space.

Information Area

Table 6 on page 22 describes the Z8 Encore! XP 64K Series Flash Microcontrollers Information Area. This 512 byte Information Area is accessed by setting bit 7 of the Page Select Register to 1. When access is enabled, the Information Area is mapped into the Program Memory and overlays the 512 bytes at addresses FE00H to FFFFH. When the Information Area access is enabled, execution of LDC and LDCI instruction from these Program Memory addresses return the Information Area data rather than the Program Memory data. Reads of these addresses through the On-Chip Debugger also returns the Information Area data. Execution of code from these addresses continues to correctly use the Program Memory. Access to the Information Area is read-only.

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Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
F61	SPI Control	SPICTL	00	137
F62	SPI Status	SPISTAT	01	139
F63	SPI Mode	SPIMODE	00	140
F64	SPI Diagnostic State	SPIDST	00	141
F65	Reserved	_	XX	
F66	SPI Baud Rate High Byte	SPIBRH	FF	142
F67	SPI Baud Rate Low Byte	SPIBRL	FF	142
F68-F6F	Reserved		XX	
Analog-to-Digit	al Converter			
F70	ADC Control	ADCCTL	20	179
F71	Reserved		XX	
F72	ADC Data High Byte	ADCD_H	XX	180
F73	ADC Data Low Bits	ADCD_L	XX	180
F74-FAF	Reserved		XX	
DMA 0				
FB0	DMA0 Control	DMA0CTL	00	167
FB1	DMA0 I/O Address	DMA0IO	XX	169
FB2	DMA0 End/Start Address High Nibble	DMA0H	XX	169
FB3	DMA0 Start Address Low Byte	DMA0START	XX	170
FB4	DMA0 End Address Low Byte	DMA0END	XX	170
DMA 1				
FB8	DMA1 Control	DMA1CTL	00	167
FB9	DMA1 I/O Address	DMA1IO	XX	169
FBA	DMA1 End/Start Address High Nibble	DMA1H	XX	169
FBB	DMA1 Start Address Low Byte	DMA1START	XX	170
FBC	DMA1 End Address Low Byte	DMA1END	XX	170
DMA ADC				
FBD	DMA_ADC Address	DMAA_ADDR	XX	171
FBE	DMA_ADC Control	DMAACTL	00	172
FBF	DMA_ADC Status	DMAASTAT	00	173
Interrupt Control	oller			
FC0	Interrupt Request 0	IRQ0	00	71
FC1	IRQ0 Enable High Bit	IRQ0ENH	00	74
FC2	IRQ0 Enable Low Bit	IRQ0ENL	00	74
FC3	Interrupt Request 1	IRQ1	00	72
FC4	IRQ1 Enable High Bit	IRQ1ENH	00	75
FC5	IRQ1 Enable Low Bit	IRQ1ENL	00	75
FC6	Interrupt Request 2	IRQ2	00	73
FC7	IRQ2 Enable High Bit	IRQ2ENH	00	76
FC8	IRQ2 Enable Low Bit	IRQ2ENL	00	76
FC9-FCC	Reserved	_	XX	

Table 7. Z8 Encore! XP 64K Series Flash Microcontrollers Register File Address Map (Continued)



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- Executing a Trap instruction.
- Illegal Instruction trap.

Interrupt Vectors and Priority

The interrupt controller supports three levels of interrupt priority. Level 3 is the highest priority, Level 2 is the second highest priority, and Level 1 is the lowest priority. If all of the interrupts were enabled with identical interrupt priority (all as Level 2 interrupts, for example), then interrupt priority would be assigned from highest to lowest as specified in Table 23 on page 68. Level 3 interrupts always have higher priority than Level 2 interrupts which, in turn, always have higher priority than Level 1 interrupts. Within each interrupt priority level (Level 1, Level 2, or Level 3), priority is assigned as specified in Table 23 on page 68. Reset, Watchdog Timer interrupt (if enabled), and Illegal Instruction Trap always have highest priority.

Interrupt Assertion

Interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the Interrupt Request register is cleared until the next interrupt occurs. Writing a 0 to the corresponding bit in the Interrupt Request register likewise clears the interrupt request.



Caution: The following style of coding to clear bits in the Interrupt Request registers is NOT recommended. All incoming interrupts that are received between execution of the first LDX command and the last LDX command are lost.

Poor coding style that can result in lost interrupt requests:

LDX r0, IRQ0 AND r0, MASK LDX IRQ0, r0

To avoid missing interrupts, the following style of coding to clear bits in the Interrupt Request 0 register is recommended:

Good coding style that avoids lost interrupt requests:

ANDX IRQ0, MASK

Software Interrupt Assertion

Program code can generate interrupts directly. Writing a 1 to the desired bit in the Interrupt Request register triggers an interrupt (assuming that interrupt is enabled). When the interrupt request is acknowledged by the eZ8 CPU, the bit in the Interrupt Request register is automatically cleared to 0.





Table 39. Timer 0-3 High Byte Register (TxH)

BITS	7	6	5	4	3	2	1	0					
FIELD	ТН												
RESET	0												
R/W	R/W												
ADDR			F	F00H, F08H,	F10H, F18H	4							

Table 40. Timer 0-3 Low Byte Register (TxL)

BITS	7	6	5	4	3	2	1	0				
FIELD	TL											
RESET	0											
R/W	R/W											
ADDR			F	F01H, F09H,	, F11H, F19H	4						

TH and TL-Timer High and Low Bytes

These 2 bytes, {TMRH[7:0], TMRL[7:0]}, contain the current 16-bit timer count value.

Timer Reload High and Low Byte Registers

The Timer 0-3 Reload High and Low Byte (TxRH and TxRL) registers (see Table 41and Table 42 on page 92) store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte register are stored in a temporary holding register. When a write to the Timer Reload Low Byte register occurs, the temporary holding register value is written to the Timer High Byte register. This operation allows simultaneous updates of the 16-bit Timer Reload value.

In COMPARE mode, the Timer Reload High and Low Byte registers store the 16-bit Compare value.

BITS	7	6	5	4	3	2	1	0				
FIELD	TRH											
RESET	1											
R/W	R/W											
ADDR			F	02H, F0AH,	F12H, F1A	1						

Table 44	T:	Delead		Durte	Deviater	(T. DII)
Table 41.	Timer 0-3	Reload	High E	Byte	Register	(IXKH)



WDT Reload Value	WDT Reload Value	Approximato (with 10 kHz typical \	e Time-Out Delay NDT oscillator frequency)
(Hex)	(Decimal)	Typical	Description
000004	4	400 μs	Minimum time-out delay
FFFFF	16,777,215	1677.5 s	Maximum time-out delay

Table 47. Watchdog Timer Approximate Time-Out Delays

Watchdog Timer Refresh

When first enabled, the Watchdog Timer is loaded with the value in the Watchdog Timer Reload registers. The Watchdog Timer then counts down to 000000H unless a WDT instruction is executed by the eZ8TM CPU. Execution of the WDT instruction causes the downcounter to be reloaded with the WDT Reload value stored in the Watchdog Timer Reload registers. Counting resumes following the reload operation.

When the 64K Series devices are operating in DEBUG Mode (through the On-Chip Debugger), the Watchdog Timer is continuously refreshed to prevent spurious Watchdog Timer time-outs.

Watchdog Timer Time-Out Response

The Watchdog Timer times out when the counter reaches 000000H. A time-out of the Watchdog Timer generates either an interrupt or a Reset. The WDT_RES Option Bit determines the time-out response of the Watchdog Timer. For information on programming of the WDT_RES Option Bit, see Option Bits on page 195.

WDT Interrupt in Normal Operation

If configured to generate an interrupt when a time-out occurs, the Watchdog Timer issues an interrupt request to the interrupt controller and sets the WDT status bit in the Watchdog Timer Control register. If interrupts are enabled, the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address. After time-out and interrupt generation, the Watchdog Timer counter rolls over to its maximum value of FFFFFH and continues counting. The Watchdog Timer counter is not automatically returned to its Reload Value.

WDT Interrupt in STOP Mode

If configured to generate an interrupt when a time-out occurs and the 64K Series devices are in STOP mode, the Watchdog Timer automatically initiates a Stop Mode Recovery and generates an interrupt request. Both the WDT status bit and the STOP bit in the Watchdog Timer Control register are set to 1 following WDT time-out in STOP mode. For more information on Stop Mode Recovery, see Reset and Stop Mode Recovery on page 47.

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- Set or clear the CTSE bit to enable or disable control from the remote receiver using the $\overline{\text{CTS}}$ pin.
- 5. Check the TDRE bit in the UART Status 0 register to determine if the Transmit Data register is empty (indicated by a 1). If empty, continue to step 6. If the Transmit Data register is full (indicated by a 0), continue to monitor the TDRE bit until the Transmit Data register becomes available to receive new data.
- 6. Write the UART Control 1 register to select the outgoing address bit.
- 7. Set the MULTIPROCESSOR Bit Transmitter (MPBT) if sending an address byte, clear it if sending a data byte.
- 8. Write the data byte to the UART Transmit Data register. The transmitter automatically transfers the data to the Transmit Shift register and transmits the data.
- 9. If desired and MULTIPROCESSOR mode is enabled, make any changes to the MULTIPROCESSOR Bit Transmitter (MPBT) value.
- 10. To transmit additional bytes, return to step 5.

Transmitting Data using the Interrupt-Driven Method

The UART transmitter interrupt indicates the availability of the Transmit Data register to accept new data for transmission. Follow the steps below to configure the UART for interrupt-driven data transmission:

- 1. Write to the UART Baud Rate High and Low Byte registers to set the desired baud rate.
- 2. Enable the UART pin functions by configuring the associated GPIO Port pins for alternate function operation.
- 3. Execute a DI instruction to disable interrupts.
- 4. Write to the Interrupt control registers to enable the UART Transmitter interrupt and set the desired priority.
- 5. If MULTIPROCESSOR mode is desired, write to the UART Control 1 register to enable MULTIPROCESSOR (9-bit) mode functions.
- 6. Set the MULTIPROCESSOR Mode Select (MPEN) to Enable MULTIPROCESSOR mode.
- 7. Write to the UART Control 0 register to:
 - Set the transmit enable bit (TEN) to enable the UART for data transmission.
 - Enable parity, if desired and if MULTIPROCESSOR mode is not enabled, and select either even or odd parity.
 - Set or clear the CTSE bit to enable or disable control from the remote receiver via the $\overline{\text{CTS}}$ pin.



Operation

When the Infrared Endec is enabled, the transmit data from the associated on-chip UART is encoded as digital signals in accordance with the IrDA standard and output to the infrared transceiver via the TXD pin. Likewise, data received from the infrared transceiver is passed to the Infrared Endec via the RXD pin, decoded by the Infrared Endec, and then passed to the UART. Communication is half-duplex, which means simultaneous data transmission and reception is not allowed.

The baud rate is set by the UART's Baud Rate Generator and supports IrDA standard baud rates from 9600 baud to 115.2 Kbaud. Higher baud rates are possible, but do not meet IrDA specifications. The UART must be enabled to use the Infrared Endec. The Infrared Endec data rate is calculated using the following equation:

nfrared Data Rate (hits/s)	_	System Clock Frequency (Hz)
Initiated Data Rate (bits/s)	_	16 × UART Baud Rate Divisor Value

Transmitting IrDA Data

The data to be transmitted using the infrared transceiver is first sent to the UART. The UART's transmit signal (TXD) and baud rate clock are used by the IrDA to generate the modulation signal (IR_TXD) that drives the infrared transceiver. Each UART/Infrared data bit is 16-clock wide. If the data to be transmitted is 1, the IR_TXD signal remains low for the full 16-clock period. If the data to be transmitted is 0, a 3-clock high pulse is output following a 7-clock low period. After the 3-clock high pulse, a 6-clock low pulse is output to complete the full 16-clock data period. Figure 20 displays IrDA data transmission. When the Infrared Endec is enabled, the UART's TXD signal is internal to the 64K Series products while the IR_TXD signal is output through the TXD pin.







Architecture

Figure 27 displays the architecture of the I²C Controller.





Operation

The I²C Controller operates in MASTER mode to transmit and receive data. Only a single master is supported. Arbitration between two masters must be accomplished in software. I²C supports the following operations:

- Master transmits to a 7-bit slave •
- Master transmits to a 10-bit slave •



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Direct Memory Access Controller

Overview

The 64K Series Direct Memory Access (DMA) Controller provides three independent Direct Memory Access channels. Two of the channels (DMA0 and DMA1) transfer data between the on-chip peripherals and the Register File. The third channel (DMA_ADC) controls the ADC operation and transfers SINGLE-SHOT mode ADC output data to the Register File.

Operation

DMA0 and DMA1 Operation

DMA0 and DMA1, referred to collectively as DMAx, transfer data either from the on-chip peripheral control registers to the Register File, or from the Register File to the on-chip peripheral control registers. The sequence of operations in a DMAx data transfer is:

- 1. DMAx trigger source requests a DMA data transfer.
- 2. DMAx requests control of the system bus (address and data) from the eZ8 CPU.
- 3. After the eZ8 CPU acknowledges the bus request, DMAx transfers either a single byte or a two-byte word (depending upon configuration) and then returns system bus control back to the eZ8 CPU.
- 4. If Current Address equals End Address:
 - DMAx reloads the original Start Address
 - If configured to generate an interrupt, DMAx sends an interrupt request to the Interrupt Controller
 - If configured for single-pass operation, DMAx resets the DEN bit in the DMAx Control register to 0 and the DMA is disabled.

If Current Address does not equal End Address, the Current Address increments by 1 (single-byte transfer) or 2 (two-byte word transfer).



- Asserting the $\overline{\text{RESET}}$ pin Low to initiate a Reset.
- Driving the DBG pin Low while the device is in STOP mode initiates a system reset.

OCD Data Format

The OCD interface uses the asynchronous data format defined for RS-232. Each character is transmitted as 1 Start bit, 8 data bits (least-significant bit first), and 1 Stop bit (see Figure 39).

-											_
	START	D0	D1	D2	D3	D4	D5	D6	D7	STOP	

Figure 39. OCD Data Format

OCD Auto-Baud Detector/Generator

To run over a range of baud rates (bits per second) with various system clock frequencies, the On-Chip Debugger has an Auto-Baud Detector/Generator. After a reset, the OCD is idle until it receives data. The OCD requires that the first character sent from the host is the character 80H. The character 80H has eight continuous bits Low (one Start bit plus 7 data bits). The Auto-Baud Detector measures this period and sets the OCD Baud Rate Generator accordingly.

The Auto-Baud Detector/Generator is clocked by the system clock. The minimum baud rate is the system clock frequency divided by 512. For optimal operation, the maximum recommended baud rate is the system clock frequency divided by 8. The theoretical maximum baud rate is the system clock frequency divided by 4. This theoretical maximum is possible for low noise designs with clean signals. Table 100 lists minimum and recommended maximum baud rates for sample crystal frequencies.

System Clock Frequency (MHz)	Recommended Maximum Baud Rate (kbits/s)	Minimum Baud Rate (kbits/s)				
20.0	2500	39.1				
1.0	125.0	1.96				
0.032768 (32 kHz)	4.096	0.064				

Table 100. OCD Baud-Rate Limits

If the OCD receives a Serial Break (nine or more continuous bits Low) the Auto-Baud Detector/Generator resets. The Auto-Baud Detector/Generator can then be reconfigured by sending 80H.



Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than those listed in Table 105 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs must be tied to one of the supply voltages (V_{DD} or V_{SS}).

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	+125	С	
Storage temperature	-65	+150	С	
Voltage on any pin with respect to V _{SS}	-0.3	+5.5	V	1
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
80-Pin QFP Maximum Ratings at –40 °C to 70 °C				
Total power dissipation		550	mW	
Maximum current into V_{DD} or out of V_{SS}		150	mA	
80-Pin QFP Maximum Ratings at 70 °C to 125 °C				
Total power dissipation		200	mW	
Maximum current into V _{DD} or out of V _{SS}		56	mA	
68-Pin PLCC Maximum Ratings at –40 °C to 70 °C				
Total power dissipation		1000	mW	
Maximum current into V_{DD} or out of V_{SS}		275	mA	
68-Pin PLCC Maximum Ratings at 70 °C to 125 °C				
Total power dissipation		500	mW	

Table 105. Absolute Maximum Ratings

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Figure 57 and Table 121 provide timing information for UART pins for the case where the Clear To Send input signal ($\overline{\text{CTS}}$) is not used for flow control. In this example, it is assumed that the Driver Enable polarity has been configured to be Active Low and is represented here by $\overline{\text{DE}}$. $\overline{\text{DE}}$ asserts after the UART Transmit Data Register has been written. $\overline{\text{DE}}$ remains asserted for multiple characters as long as the Transmit Data register is written with the next character before the current character has completed.





Table 121. UAR1	' Timing	without	CTS
-----------------	----------	---------	-----

		Delay (ns)				
Parameter	Abbreviation	Minimum	Maximum			
T ₁	DE Assertion to TXD Falling Edge (Start) Delay	1 Bit period	1 Bit period + 1 * XIN period			
T ₂	End of Stop Bit(s) to $\overline{\text{DE}}$ Deassertion Delay	1 * XIN period	2 * XIN period			



Assombly		Address Mode		Opcodo(c)			Fla	ıgs			Fotob	luctu
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	V	D	Н	Cycles	Cycles
OR dst, src	$dst \gets dst \ OR \ src$	r	r	42	-	*	*	0	-	-	2	3
	-	r	lr	43							2	4
	-	R	R	44							3	3
	-	R	IR	45							3	4
	-	R	IM	46							3	3
	-	IR	IM	47							3	4
ORX dst, src	$dst \gets dst \ OR \ src$	ER	ER	48	-	*	*	0	-	-	4	3
	-	ER	IM	49							4	3
POP dst	dst ← @SP	R		50	-	-	-	-	-	-	2	2
	$SP \leftarrow SP + 1$	IR		51							2	3
POPX dst	dst \leftarrow @SP SP \leftarrow SP + 1	ER		D8	-	-	-	-	-	-	3	2
PUSH src	$SP \leftarrow SP - 1$ @SP \leftarrow src -	R		70	-	-	-	-	-	-	2	2
		IR		71	•						2	3
		IM		1F 70							3	2
PUSHX src	$SP \leftarrow SP - 1$ @SP ← src	ER		C8	-	-	-	-	-	-	3	2
RCF	C ← 0			CF	0	-	-	-	-	-	1	2
RET	$\begin{array}{l} PC \leftarrow @SP \\ SP \leftarrow SP + 2 \end{array}$			AF	-	-	-	-	-	-	1	4
RL dst	C	R		90	*	*	*	*	-	-	2	2
		IR		91							2	3
RLC dst	CD7D6D5D4D3D2D1D0 dst	R		10	*	*	*	*	-	-	2	2
		IR		11							2	3
RR dst		R		E0	*	*	*	*	-	-	2	2
	► D7 D6 D5 D4 D3 D2 D1 D0 dst C	IR		E1							2	3

Table 133. eZ8 CPU Instruction Summary (Continued)



Opcode Maps

A description of the opcode map data and the abbreviations are provided in Figure 59 and Table 134 on page 262. Figure 60 on page 263 and Figure 61 on page 264 provide information on each of the $eZ8^{TM}$ CPU instructions.



Figure 59. Opcode Map Cell Description





Figure 67 displays the 80-pin Quad Flat Package (QFP) available for the Z8X4823 and Z8X6423 devices.

Figure 67. 80-Lead Quad-Flat Package (QFP)