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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f6421pm020sc">https://www.e-xfl.com/product-detail/zilog/z8f6421pm020sc</a>

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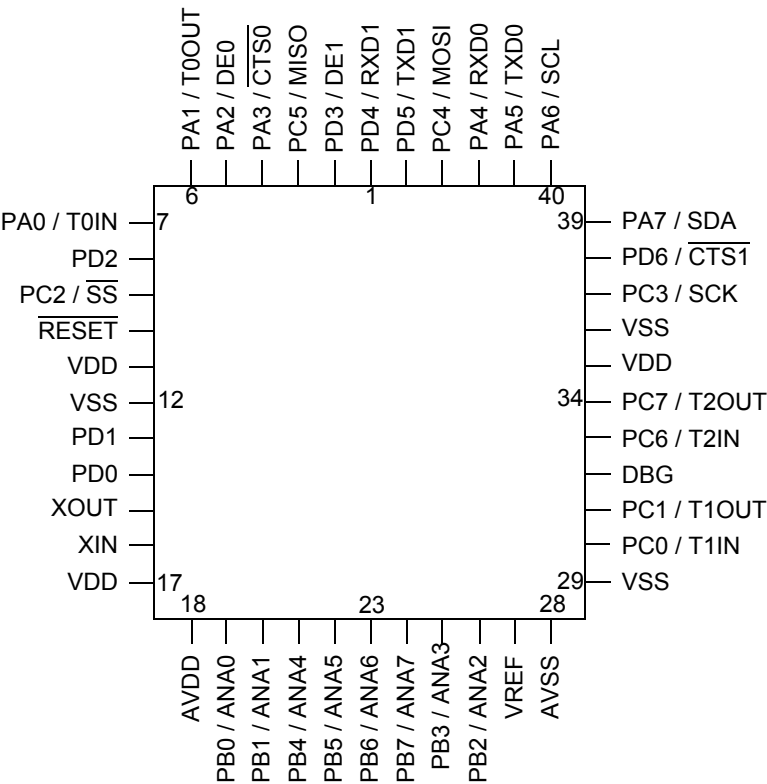


Figure 3. Z8 Encore! XP 64K Series Flash Microcontrollers in 44-Pin Plastic Leaded Chip Carrier (PLCC)

**Table 7. Z8 Encore! XP 64K Series Flash Microcontrollers Register File Address Map (Continued)**

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
<b>Timer 3 (unavailable in the 44-pin packages)</b>				
F18	Timer 3 High Byte	T3H	00	90
F19	Timer 3 Low Byte	T3L	01	90
F1A	Timer 3 Reload High Byte	T3RH	FF	91
F1B	Timer 3 Reload Low Byte	T3RL	FF	91
F1C	Timer 3 PWM High Byte	T3PWMH	00	92
F1D	Timer 3 PWM Low Byte	T3PWML	00	92
F1E	Timer 3 Control 0	T3CTL0	00	93
F1F	Timer 3 Control 1	T3CTL1	00	94
20-3F	Reserved	—	XX	
<b>UART 0</b>				
F40	UART0 Transmit Data	U0TXD	XX	114
	UART0 Receive Data	U0RXD	XX	115
F41	UART0 Status 0	U0STAT0	0000011Xb	115
F42	UART0 Control 0	U0CTL0	00	117
F43	UART0 Control 1	U0CTL1	00	117
F44	UART0 Status 1	U0STAT1	00	115
F45	UART0 Address Compare Register	U0ADDR	00	120
F46	UART0 Baud Rate High Byte	U0BRH	FF	120
F47	UART0 Baud Rate Low Byte	U0BRL	FF	120
<b>UART 1</b>				
F48	UART1 Transmit Data	U1TXD	XX	114
	UART1 Receive Data	U1RXD	XX	115
F49	UART1 Status 0	U1STAT0	0000011Xb	115
F4A	UART1 Control 0	U1CTL0	00	117
F4B	UART1 Control 1	U1CTL1	00	117
F4C	UART1 Status 1	U1STAT1	00	115
F4D	UART1 Address Compare Register	U1ADDR	00	120
F4E	UART1 Baud Rate High Byte	U1BRH	FF	120
F4F	UART1 Baud Rate Low Byte	U1BRL	FF	120
<b>I<sup>2</sup>C</b>				
F50	I <sup>2</sup> C Data	I2CDATA	00	156
F51	I <sup>2</sup> C Status	I2CSTAT	80	157
F52	I <sup>2</sup> C Control	I2CCTL	00	158
F53	I <sup>2</sup> C Baud Rate High Byte	I2CBRH	FF	160
F54	I <sup>2</sup> C Baud Rate Low Byte	I2CBRL	FF	160
F55	I <sup>2</sup> C Diagnostic State	I2CDST	C0	161
F56	I <sup>2</sup> C Diagnostic Control	I2CDIAG	00	163
F57-F5F	Reserved	—	XX	
<b>Serial Peripheral Interface (SPI)</b>				
F60	SPI Data	SPIDATA	XX	137

### DMA1 Control

DMA1CTL (FB8H - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0

- Request Trigger Source Select
  - 000 = Timer 0
  - 001 = Timer 1
  - 010 = Timer 2
  - 011 = Timer 3
  - 100 = UART0 Transmit Data register is empty
  - 101 = UART1 Transmit Data register is empty
  - 110 = I2C Transmit Data register is empty
  - 111 = Reserved
- Word Select
  - 0 = DMA transfers 1 byte per request
  - 1 = DMA transfers 2 bytes per request
- DMA1 Interrupt Enable
  - 0 = DMA1 does not generate interrupts
  - 1 = DMA1 generates an interrupt when End Address data is transferred
- DMA1 Data Transfer Direction
  - 0 = Register File to peripheral registers
  - 1 = Peripheral registers to Register File
- DMA1 Loop Enable
  - 0 = DMA disables after End Address
  - 1 = DMA reloads Start Address after End Address and continues to run
- DMA1 Enable
  - 0 = DMA1 is disabled
  - 1 = DMA1 is enabled

### DMA1 Address High Nibble

DMA1H (FBAH - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0

- DMA1 Start Address [11:8]
- DMA1 End Address [11:8]

### DMA1 Start/Current Address Low Byte

DMA1START (FBBH - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0

- DMA1 Start Address [7:0]

### DMA1 End Address Low Byte

DMA1END (FBCH - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0

- DMA1 End Address [7:0]

### DMA\_ADC Address

DMAA\_ADDR (FBDH - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0

- Reserved
- DMA\_ADC Address

### DMA1 I/O Address

DMA1IO (FB9H - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0

- DMA1 Peripheral Register Address
  - Low byte of on-chip peripheral control registers on Register File page FH

**Table 23. Interrupt Vectors in Order of Priority**

Priority	Program Memory Vector Address	Interrupt Source
Highest	0002H	Reset (not an interrupt)
	0004H	Watchdog Timer (see <a href="#">Watchdog Timer</a> on page 97)
	0006H	Illegal Instruction Trap (not an interrupt)
	0008H	Timer 2
	000AH	Timer 1
	000CH	Timer 0
	000EH	UART 0 receiver
	0010H	UART 0 transmitter
	0012H	I <sup>2</sup> C
	0014H	SPI
	0016H	ADC
	0018H	Port A7 or Port D7, rising or falling input edge
	001AH	Port A6 or Port D6, rising or falling input edge
	001CH	Port A5 or Port D5, rising or falling input edge
	001EH	Port A4 or Port D4, rising or falling input edge
	0020H	Port A3 or Port D3, rising or falling input edge
	0022H	Port A2 or Port D2, rising or falling input edge
	0024H	Port A1 or Port D1, rising or falling input edge
	0026H	Port A0 or Port D0, rising or falling input edge
	0028H	Timer 3 ( <i>not available in 44-pin packages</i> )
	002AH	UART 1 receiver
	002CH	UART 1 transmitter
	002EH	DMA
	0030H	Port C3, both input edges
	0032H	Port C2, both input edges
	0034H	Port C1, both input edges
Lowest	0036H	Port C0, both input edges

C1ENL—Port C1 Interrupt Request Enable Low Bit

C0ENL—Port C0 Interrupt Request Enable Low Bit

## Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) register ([Table 36](#)) determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port input pin. The Interrupt Port Select register selects between Port A and Port D for the individual interrupts.

**Table 36. Interrupt Edge Select Register (IRQES)**

BITS	7	6	5	4	3	2	1	0
FIELD	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0							
R/W	R/W							
ADDR	FCDH							

IES<sub>x</sub>—Interrupt Edge Select *x*

The minimum pulse width should be greater than 1 system clock to guarantee capture of the edge triggered interrupt. Shorter pulses may be captured but not guaranteed.

0 = An interrupt request is generated on the falling edge of the PA<sub>x</sub>/PD<sub>x</sub> input.

1 = An interrupt request is generated on the rising edge of the PA<sub>x</sub>/PD<sub>x</sub> input.

where *x* indicates the specific GPIO Port pin number (0 through 7).

## Interrupt Port Select Register

The Port Select (IRQPS) register ([Table 37](#)) determines the port pin that generates the PA<sub>x</sub>/PD<sub>x</sub> interrupts. This register allows either Port A or Port D pins to be used as interrupts. The Interrupt Edge Select register controls the active interrupt edge.

**Table 37. Interrupt Port Select Register (IRQPS)**

BITS	7	6	5	4	3	2	1	0
FIELD	PAD7S	PAD6S	PAD5S	PAD4S	PAD3S	PAD2S	PAD1S	PAD0S
RESET	0							
R/W	R/W							
ADDR	FCEH							



- Select either the rising edge or falling edge of the Timer Input signal for the count. This also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function does not have to be enabled
- 2. Write to the Timer High and Low Byte registers to set the starting count value. This only affects the first pass in COUNTER mode. After the first timer Reload in COUNTER mode, counting always begins at the reset value of 0001H. Generally, in COUNTER mode the Timer High and Low Byte registers must be written with the value 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. If desired, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 7. Write to the Timer Control 1 register to enable the timer.

In COUNTER mode, the number of Timer Input transitions since the timer start is given by the following equation:

$$\text{COUNTER Mode Timer Input Transitions} = \text{Current Count Value} - \text{Start Value}$$

### **PWM Mode**

In PWM mode, the timer outputs a Pulse-Width Modulator (PWM) output signal through a GPIO Port pin. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control 1 register is set to 1, the Timer Output signal begins as a High (1) and then transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the Reload value and is reset to 0001H.

If the TPOL bit in the Timer Control 1 register is set to 0, the Timer Output signal begins as a Low (0) and then transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the Reload value and is reset to 0001H.

Follow the steps below for configuring a timer for PWM mode and initiating the PWM operation:

1. Write to the Timer Control 1 register to:
  - Disable the timer
  - Configure the timer for PWM mode
  - Set the prescale value
  - Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of 0001H.
3. Write to the PWM High and Low Byte registers to set the PWM value.
4. Write to the Timer Reload High and Low Byte registers to set the Reload value (PWM period). The Reload value must be greater than the PWM value.
5. If desired, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
6. Configure the associated GPIO port pin for the Timer Output alternate function.
7. Write to the Timer Control 1 register to enable the timer and initiate counting.

The PWM period is given by the following equation:

$$\text{PWM Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, the ONE-SHOT mode equation must be used to determine the first PWM time-out period.

If TPOL is set to 0, the ratio of the PWM output High time to the total period is given by:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is given by:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{PWM Value}}{\text{Reload Value}} \times 100$$

### **CAPTURE Mode**

In CAPTURE mode, the current timer count value is recorded when the desired external Timer Input transition occurs. The Capture count value is written to the Timer PWM High and Low Byte Registers. The timer input is the system clock. The TPOL bit in the Timer Control 1 register determines if the Capture occurs on a rising edge or a falling edge of the Timer Input signal. When the Capture event occurs, an interrupt is generated and the timer continues counting.

**Table 39. Timer 0-3 High Byte Register (TxH)**

BITS	7	6	5	4	3	2	1	0
FIELD	TH							
RESET	0							
R/W	R/W							
ADDR	F00H, F08H, F10H, F18H							

**Table 40. Timer 0-3 Low Byte Register (TxL)**

BITS	7	6	5	4	3	2	1	0
FIELD	TL							
RESET	0							1
R/W	R/W							
ADDR	F01H, F09H, F11H, F19H							

TH and TL—Timer High and Low Bytes

These 2 bytes, {TMRH[7:0], TMRL[7:0]}, contain the current 16-bit timer count value.

### Timer Reload High and Low Byte Registers

The Timer 0-3 Reload High and Low Byte (TxRH and TxRL) registers (see [Table 41](#) and [Table 42](#) on page 92) store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte register are stored in a temporary holding register. When a write to the Timer Reload Low Byte register occurs, the temporary holding register value is written to the Timer High Byte register. This operation allows simultaneous updates of the 16-bit Timer Reload value.

In COMPARE mode, the Timer Reload High and Low Byte registers store the 16-bit Compare value.

**Table 41. Timer 0-3 Reload High Byte Register (TxRH)**

BITS	7	6	5	4	3	2	1	0
FIELD	TRH							
RESET	1							
R/W	R/W							
ADDR	F02H, F0AH, F12H, F1AH							

110 = Divide by 64

111 = Divide by 128

TMODE—TIMER mode

000 = ONE-SHOT mode

001 = CONTINUOUS mode

010 = COUNTER mode

011 = PWM mode

100 = CAPTURE mode

101 = COMPARE mode

110 = GATED mode

111 = CAPTURE/COMPARE mode

5. Write the Watchdog Timer Reload Low Byte register (WDTL).

All steps of the Watchdog Timer Reload Unlock sequence must be written in the order just listed. There must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur, unless the sequence is restarted. The value in the Watchdog Timer Reload registers is loaded into the counter when the Watchdog Timer is first enabled and every time a WDT instruction is executed.

## Watchdog Timer Control Register Definitions

### Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) register (Table 48) is a Read-Only register that indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event, and indicates a Watchdog Timer time-out. Reading this register resets the upper four bits to 0.

Writing the 55H, AAH unlock sequence to the Watchdog Timer Control (WDTCTL) register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTL, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers.

**Table 48. Watchdog Timer Control Register (WDTCTL)**

BITS	7	6	5	4	3	2	1	0
FIELD	POR	STOP	WDT	EXT	Reserved			SM
RESET	See descriptions below			0				
R/W	R							
ADDR	FF0H							

Reset or Stop Mode Recovery Event	POR	STOP	WDT	EXT
Power-On Reset	1	0	0	0
Reset using RESET pin assertion	0	0	0	1
Reset using Watchdog Timer time-out	0	0	1	0
Reset using the On-Chip Debugger (OCDCTL[1] set to 1)	1	0	0	0
Reset from STOP Mode using DBG Pin driven Low	1	0	0	0
Stop Mode Recovery using GPIO pin transition	0	1	0	0
Stop Mode Recovery using Watchdog Timer time-out	0	1	1	0

## Operation

When the Infrared Endec is enabled, the transmit data from the associated on-chip UART is encoded as digital signals in accordance with the IrDA standard and output to the infrared transceiver via the TXD pin. Likewise, data received from the infrared transceiver is passed to the Infrared Endec via the RXD pin, decoded by the Infrared Endec, and then passed to the UART. Communication is half-duplex, which means simultaneous data transmission and reception is not allowed.

The baud rate is set by the UART's Baud Rate Generator and supports IrDA standard baud rates from 9600 baud to 115.2 Kbaud. Higher baud rates are possible, but do not meet IrDA specifications. The UART must be enabled to use the Infrared Endec. The Infrared Endec data rate is calculated using the following equation:

$$\text{Infrared Data Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$$

### Transmitting IrDA Data

The data to be transmitted using the infrared transceiver is first sent to the UART. The UART's transmit signal (TXD) and baud rate clock are used by the IrDA to generate the modulation signal (IR\_TXD) that drives the infrared transceiver. Each UART/Infrared data bit is 16-clock wide. If the data to be transmitted is 1, the IR\_TXD signal remains low for the full 16-clock period. If the data to be transmitted is 0, a 3-clock high pulse is output following a 7-clock low period. After the 3-clock high pulse, a 6-clock low pulse is output to complete the full 16-clock data period. Figure 20 displays IrDA data transmission.

When the Infrared Endec is enabled, the UART's TXD signal is internal to the 64K Series products while the IR\_TXD signal is output through the TXD pin.

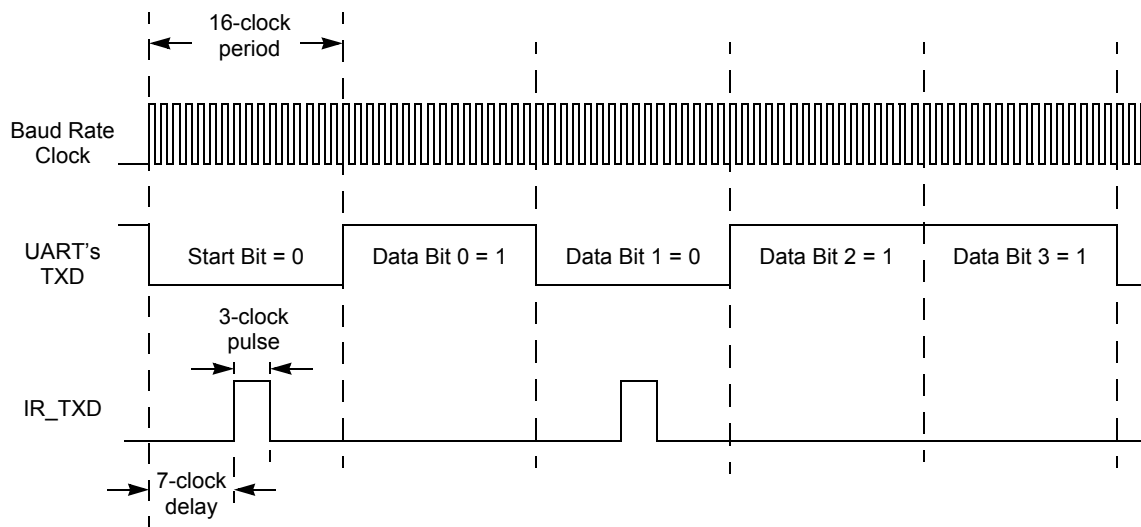


Figure 20. Infrared Data Transmission

7. The I<sup>2</sup>C Controller loads the I<sup>2</sup>C Shift register with the contents of the I<sup>2</sup>C Data register.
8. After one bit of address is shifted out by the SDA signal, the Transmit interrupt is asserted.
9. Software responds by writing the second byte of address into the contents of the I<sup>2</sup>C Data register.
10. The I<sup>2</sup>C Controller shifts the rest of the first byte of address and write bit out the SDA signal.
11. If the I<sup>2</sup>C slave sends an acknowledge by pulling the SDA signal low during the next high period of SCL the I<sup>2</sup>C Controller sets the ACK bit in the I<sup>2</sup>C Status register. Continue with [step 12](#).

If the slave does not acknowledge the first address byte, the I<sup>2</sup>C Controller sets the NCKI bit and clears the ACK bit in the I<sup>2</sup>C Status register. Software responds to the Not Acknowledge interrupt by setting the STOP and FLUSH bits and clearing the TXI bit. The I<sup>2</sup>C Controller sends the STOP condition on the bus and clears the STOP and NCKI bits. The transaction is complete (ignore following steps).

12. The I<sup>2</sup>C Controller loads the I<sup>2</sup>C Shift register with the contents of the I<sup>2</sup>C Data register (2nd byte of address).
13. The I<sup>2</sup>C Controller shifts the second address byte out the SDA signal. After the first bit has been sent, the Transmit interrupt is asserted.
14. Software responds by setting the STOP bit in the I<sup>2</sup>C Control register. The TXI bit can be cleared at the same time.
15. Software polls the STOP bit of the I<sup>2</sup>C Control register. Hardware deasserts the STOP bit when the transaction is completed (STOP condition has been sent).
16. Software checks the ACK bit of the I<sup>2</sup>C Status register. If the slave acknowledged, the ACK bit is = 1. If the slave does not acknowledge, the ACK bit is = 0. The NCKI interrupt do not occur because the STOP bit was set.

### Write Transaction with a 10-Bit Address

[Figure 31](#) displays the data transfer format for a 10-bit addressed slave. Shaded regions indicate data transferred from the I<sup>2</sup>C Controller to slaves and unshaded regions indicate data transferred from the slaves to the I<sup>2</sup>C Controller.

S	Slave Address 1st 7 bits	W = 0	A	Slave Address 2nd Byte	A	Data	A	Data	A/A	P/S
---	-----------------------------	-------	---	---------------------------	---	------	---	------	-----	-----

**Figure 31. 10-Bit Addressed Slave Data Transfer Format**

## I<sup>2</sup>C Baud Rate High and Low Byte Registers

The I<sup>2</sup>C Baud Rate High and Low Byte registers (Tables 73 and 73) combine to form a 16-bit reload value, BRG[15:0], for the I<sup>2</sup>C Baud Rate Generator.

When the I<sup>2</sup>C is disabled, the Baud Rate Generator can function as a basic 16-bit timer with interrupt on time-out. To configure the Baud Rate Generator as a timer with interrupt on time-out, complete the following procedure:

1. Disable the I<sup>2</sup>C by clearing the IEN bit in the I<sup>2</sup>C Control register to 0.
2. Load the desired 16-bit count value into the I<sup>2</sup>C Baud Rate High and Low Byte registers.
3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BIRQ bit in the I<sup>2</sup>C Control register to 1.

When configured as a general purpose timer, the interrupt interval is calculated using the following equation:

$$\text{Interrupt Interval (s)} = \text{System Clock Period (s)} \times \text{BRG}[15:0]$$

**Table 73. I<sup>2</sup>C Baud Rate High Byte Register (I2CBRH)**

BITS	7	6	5	4	3	2	1	0
FIELD	BRH							
RESET	FFH							
R/W	R/W							
ADDR	F53H							

BRH = I<sup>2</sup>C Baud Rate High Byte

Most significant byte, BRG[15:8], of the I<sup>2</sup>C Baud Rate Generator's reload value.

► **Note:** If the DIAG bit in the I<sup>2</sup>C Diagnostic Control Register is set to 1, a read of the I2CBRH register returns the current value of the I<sup>2</sup>C Baud Rate Counter[15:8].



**Table 96. Flash Frequency High Byte Register (FFREQH)**

BITS	7	6	5	4	3	2	1	0
FIELD	FFREQH							
RESET	0							
R/W	R/W							
ADDR	FFAH							

**Table 97. Flash Frequency Low Byte Register (FFREQL)**

BITS	7	6	5	4	3	2	1	0
FIELD	FFREQL							
RESET	0							
R/W	R/W							
ADDR	FFBH							

FFREQH and FFREQL—Flash Frequency High and Low Bytes  
These 2 bytes, {FFREQH[7:0], FFREQL[7:0]}, contain the 16-bit Flash Frequency value.

Figure 43 displays the typical active mode current consumption while operating at 25 °C versus the system clock frequency. All GPIO pins are configured as outputs and driven High.

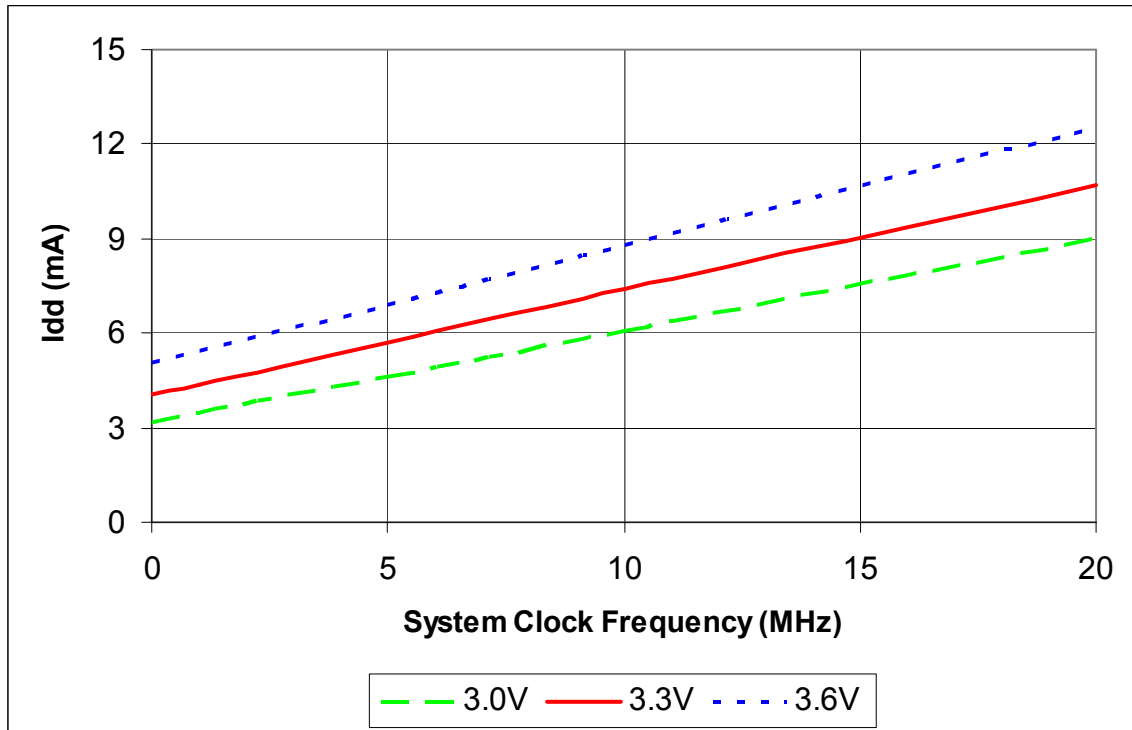


Figure 43. Typical Active Mode Idd Versus System Clock Frequency

Figure 45 displays the typical current consumption in HALT mode while operating at 25 °C versus the system clock frequency. All GPIO pins are configured as outputs and driven High.

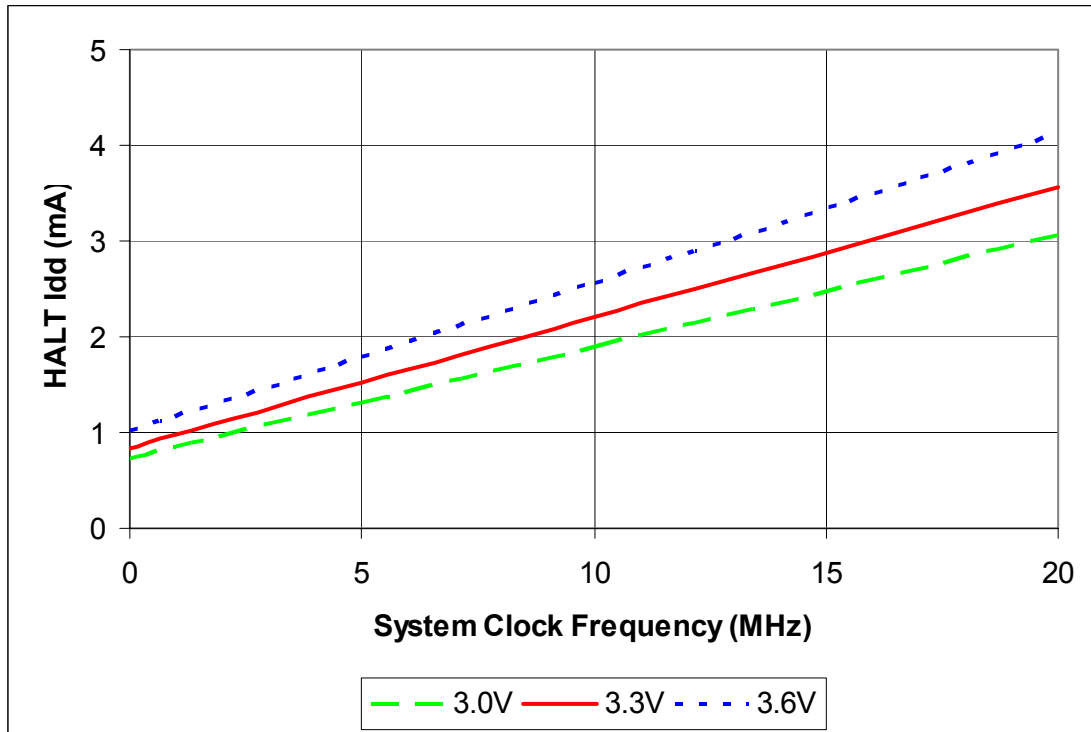


Figure 45. Typical HALT Mode Idd Versus System Clock Frequency

**Table 108. External RC Oscillator Electrical Characteristics and Timing**

Symbol	Parameter	T <sub>A</sub> = -40 °C to 125 °C			Units	Conditions
		Minimum	Typical <sup>1</sup>	Maximum		
V <sub>DD</sub>	Operating Voltage Range	2.70 <sup>1</sup>	–	–	V	
R <sub>EXT</sub>	External Resistance from XIN to VDD	40	45	200	kΩ	V <sub>DD</sub> = V <sub>VBO</sub>
C <sub>EXT</sub>	External Capacitance from XIN to VSS	0	20	1000	pF	
F <sub>OSC</sub>	External RC Oscillation Frequency	–	–	4	MHz	

<sup>1</sup>When using the external RC oscillator mode, the oscillator may stop oscillating if the power supply drops below 2.7 V, but before the power supply drops to the voltage brown-out threshold. The oscillator will resume oscillation as soon as the supply voltage exceeds 2.7 V.

**Table 109. Reset and Stop Mode Recovery Pin Timing**

Symbol	Parameter	T <sub>A</sub> = -40 °C to 125 °C			Units	Conditions
		Minimum	Typical	Maximum		
T <sub>RESET</sub>	RESET pin assertion to initiate a system reset.	4	–	–	T <sub>CLK</sub>	Not in STOP Mode. T <sub>CLK</sub> = System Clock period.
T <sub>SMR</sub>	Stop Mode Recovery pin Pulse Rejection Period	10	20	40	ns	RESET, DBG, and GPIO pins configured as SMR sources.

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