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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f6421vn020ec

Introduction

Zilog's Z8 Encore! XP MCU family of products are a line of Zilog[®] microcontroller products based upon the 8-bit eZ8 CPU. The Z8 Encore! XP[®] 64K Series Flash Microcontrollers, hereafter referred to collectively as the Z8 Encore! XP or the 64K Series adds Flash memory to Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8[™] CPU is upward compatible with existing Z8[®] instructions. The rich-peripheral set of the Z8 Encore! XP makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

Features

The features of Z8 Encore! XP 64K Series Flash Microcontrollers include:

- 20 MHz eZ8 CPU
- Up to 64 KB Flash with in-circuit programming capability
- Up to 4 KB register RAM
- 12-channel, 10-bit Analog-to-Digital Converter (ADC)
- Two full-duplex 9-bit UARTs with bus transceiver Driver Enable control
- Inter-integrated circuit (I²C)
- Serial Peripheral Interface (SPI)
- Two Infrared Data Association (IrDA)-compliant infrared encoder/decoders
- Up to four 16-bit timers with capture, compare, and PWM capability
- Watchdog Timer (WDT) with internal RC oscillator
- Three-channel DMA
- Up to 60 input/output (I/O) pins
- 24 interrupts with configurable priority
- On-Chip Debugger
- Voltage Brownout (VBO) Protection
- Power-On Reset (POR)
- Operating voltage of 3.0 V to 3.6 V with 5 V-tolerant inputs
- 0 °C to +70 °C, -40 °C to +105 °C, and -40 °C to +125 °C operating temperature ranges

UART0 Control 1

U0CTL1 (F43H - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0

- Infrared Encoder/Decoder Enable
0 = Infrared endec is disabled
1 = Infrared endec is enabled
- Received Data Interrupt Enable
0 = Received data and errors generate interrupt requests
1 = Only errors generate interrupt requests. Received data does not.
- Baud Rate Registers Control
Refer to UART chapter for operation
- Driver Enable Polarity
0 = DE signal is active High
1 = DE signal is active Low
- Multiprocessor Bit Transmit
0 = Send a 0 as the multiprocessor bit
1 = Send a 1 as the multiprocessor bit
- Multiprocessor Mode [0]
See Multiprocessor Mode [1] below
- Multiprocessor (9-bit) Enable
0 = Multiprocessor mode is disabled
1 = Multiprocessor mode is enabled
- Multiprocessor Mode [1]
with Multiprocess Mode bit 0:
00 = Interrupt on all received bytes
01 = Interrupt only on address bytes
10 = Interrupt on address match and following data
11 = Interrupt on data following an address match

UART0 Status 1

U0STAT1 (F44H - Read Only)

D7 D6 D5 D4 D3 D2 D1 D0

- Multiprocessor Receive
Returns value of last multiprocessor bit
- New Frame
0 = Current byte is not start of frame
1 = Current byte is start of new frame
- Reserved

UART0 Address Compare

U0ADDR (F45H - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0

UART0 Address Compare [7:0]

UART0 Baud Rate Generator High Byte

U0BRH (F46H - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0

UART0 Baud Rate divisor [15:8]

UART0 Baud Rate Generator Low Byte

U0BRL (F47H - Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0

UART0 Baud Rate divisor [7:0]

UART1 Transmit Data

U1TXD (F48H - Write Only)

D7 D6 D5 D4 D3 D2 D1 D0

UART1 transmitter data byte[7:0]

UART1 Receive Data

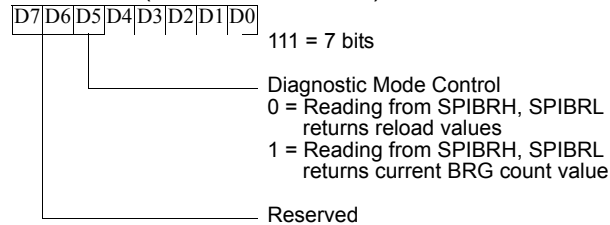
U1RXD (F48H - Read Only)

D7 D6 D5 D4 D3 D2 D1 D0

UART receiver data byte [7:0]

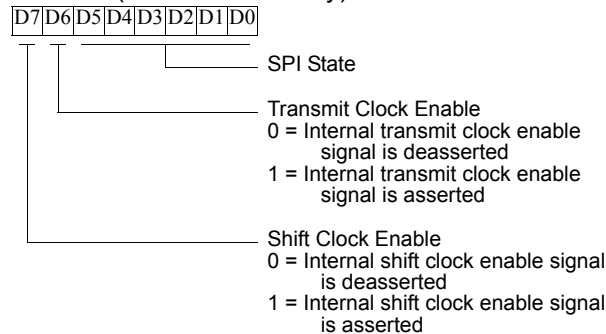
SPI Mode

SPIMODE (F63H - Read/Write)



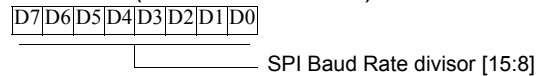
SPI Diagnostic State

SPIDST (F64H - Read Only)



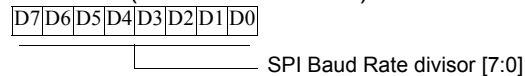
SPI Baud Rate Generator High Byte

SPIBRH (F66H - Read/Write)



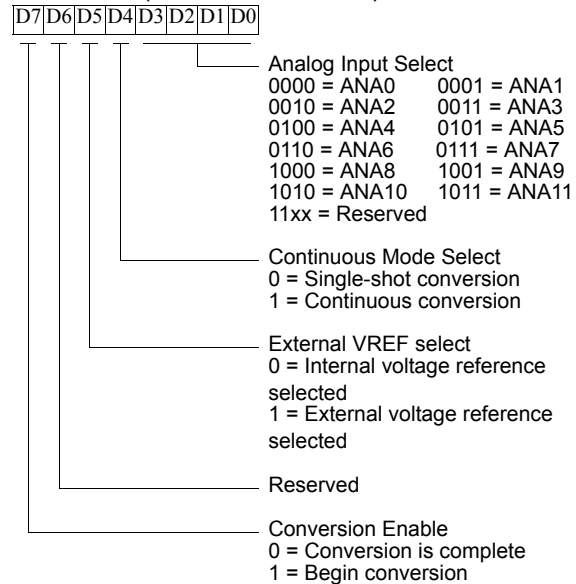
SPI Baud Rate Generator Low Byte

SPIBRL (F67H - Read/Write)



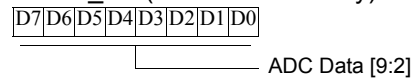
ADC Control

ADCCTL (F70H - Read/Write)



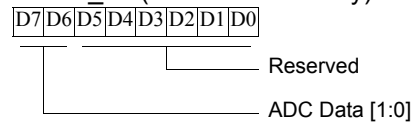
ADC Data High Byte

ADCD_H (F72H - Read Only)



ADC Data Low Bits

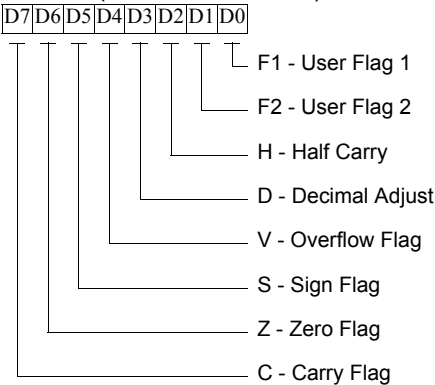
ADCD_L (F73H - Read Only)





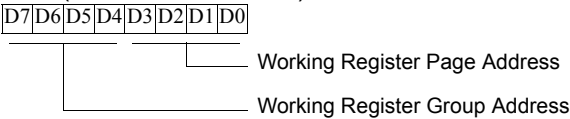
Flags

FLAGS (FFC - Read/Write)



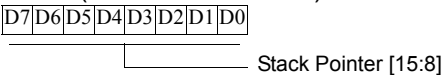
Register Pointer

RP (FFDH - Read/Write)



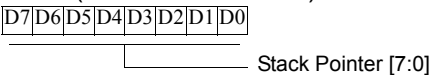
Stack Pointer High Byte

SPH (FFEH - Read/Write)



Stack Pointer Low Byte

SPL (FFFH - Read/Write)



Architecture

Figure 11 displays a block diagram of the interrupt controller.

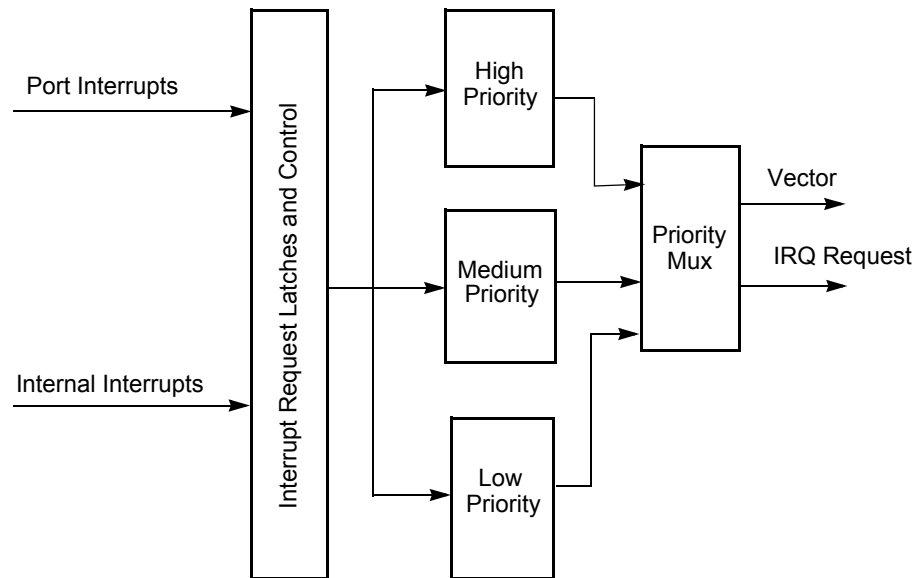


Figure 11. Interrupt Controller Block Diagram

Operation

Master Interrupt Enable

The master interrupt enable bit (IRQE) in the Interrupt Control register globally enables and disables interrupts.

Interrupts are globally enabled by any of the following actions:

- Executing an Enable Interrupt (EI) instruction.
- Executing an Return from Interrupt (IRET) instruction.
- Writing a 1 to the IRQE bit in the Interrupt Control register.

Interrupts are globally disabled by any of the following actions:

- Execution of a Disable Interrupt (DI) instruction.
- eZ8 CPU acknowledgement of an interrupt service request from the interrupt controller.
- Writing a 0 to the IRQE bit in the Interrupt Control register.
- Reset.

Table 31. IRQ1 Enable High Bit Register (IRQ1ENH)

BITS	7	6	5	4	3	2	1	0
FIELD	PAD7ENH	PAD6ENH	PAD5ENH	PAD4ENH	PAD3ENH	PAD2ENH	PAD1ENH	PAD0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FC4H							

PADxENH—Port A or Port D Bit[x] Interrupt Request Enable High Bit.
For selection of either Port A or Port D as the interrupt source, see [Interrupt Port Select Register](#) on page 78.

Table 32. IRQ1 Enable Low Bit Register (IRQ1ENL)

BITS	7	6	5	4	3	2	1	0
FIELD	PAD7ENL	PAD6ENL	PAD5ENL	PAD4ENL	PAD3ENL	PAD2ENL	PAD1ENL	PAD0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FC5H							

PADxENL—Port A or Port D Bit[x] Interrupt Request Enable Low Bit
For selection of either Port A or Port D as the interrupt source, see [Interrupt Port Select Register](#) on page 78.

IRQ2 Enable High and Low Bit Registers

The IRQ2 Enable High and Low Bit registers (see [Table 34](#) and [Table 35](#) on page 77) form a priority encoded enabling for interrupts in the Interrupt Request 2 register. Priority is generated by setting bits in each register. [Table 33](#) describes the priority control for IRQ2.

Table 33. IRQ2 Enable and Priority Encoding

IRQ2ENH[x]	IRQ2ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal

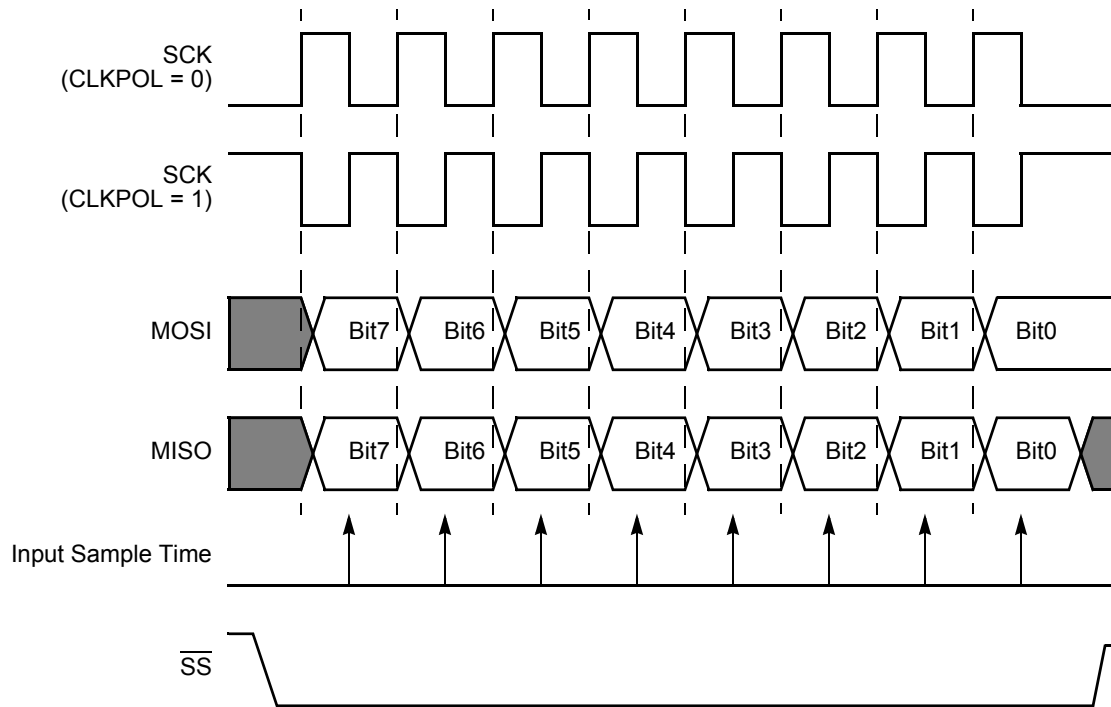


Figure 26. SPI Timing When PHASE is 1

Multi-Master Operation

In a multi-master SPI system, all SCK pins are tied together, all MOSI pins are tied together and all MISO pins are tied together. All SPI pins must then be configured in OPEN-DRAIN mode to prevent bus contention. At any one time, only one SPI device is configured as the Master and all other SPI devices on the bus are configured as Slaves. The Master enables a single Slave by asserting the \overline{SS} pin on that Slave only. Then, the single Master drives data out its SCK and MOSI pins to the SCK and MOSI pins on the Slaves (including those which are not enabled). The enabled Slave drives data out its MISO pin to the MISO Master pin.

For a Master device operating in a multi-master system, if the \overline{SS} pin is configured as an input and is driven Low by another Master, the COL bit is set to 1 in the SPI Status Register. The COL bit indicates the occurrence of a multi-master collision (mode fault error condition).

Slave Operation

The SPI block is configured for SLAVE mode operation by setting the SPIEN bit to 1 and the MMEN bit to 0 in the SPICTL register and setting the SSIO bit to 0 in the SPIMODE

defined to be 1 through 8 bits by the NUMBITS field in the SPI Mode register. In slave mode it is not necessary for \overline{SS} to deassert between characters to generate the interrupt. The SPI in Slave mode can also generate an interrupt if the \overline{SS} signal deasserts prior to transfer of all the bits in a character (see description of slave abort error above). Writing a 1 to the IRQ bit in the SPI Status Register clears the pending SPI interrupt request. The IRQ bit must be cleared to 0 by the Interrupt Service Routine to generate future interrupts. To start the transfer process, an SPI interrupt may be forced by software writing a 1 to the STR bit in the SPICTL register.

If the SPI is disabled, an SPI interrupt can be generated by a Baud Rate Generator time-out. This timer function must be enabled by setting the BIRQ bit in the SPICTL register. This Baud Rate Generator time-out does not set the IRQ bit in the SPISTAT register, just the SPI interrupt bit in the interrupt controller.

SPI Baud Rate Generator

In SPI Master mode, the Baud Rate Generator creates a lower frequency serial clock (SCK) for data transmission synchronization between the Master and the external Slave. The input to the Baud Rate Generator is the system clock. The SPI Baud Rate High and Low Byte registers combine to form a 16-bit reload value, BRG[15:0], for the SPI Baud Rate Generator. The SPI baud rate is calculated using the following equation:

$$\text{SPI Baud Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{2 \times \text{BRG}[15:0]}$$

Minimum baud rate is obtained by setting BRG[15:0] to 0000H for a clock divisor value of (2 X 65536 = 131072).

When the SPI is disabled, the Baud Rate Generator can function as a basic 16-bit timer with interrupt on time-out. Follow the steps below to configure the Baud Rate Generator as a timer with interrupt on time-out:

1. Disable the SPI by clearing the SPIEN bit in the SPI Control register to 0.
2. Load the desired 16-bit count value into the SPI Baud Rate High and Low Byte registers.
3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BIRQ bit in the SPI Control register to 1.

When configured as a general purpose timer, the interrupt interval is calculated using the following equation:

$$\text{Interrupt Interval (s)} = \text{System Clock Period (s)} \times \text{BRG}[15:0]$$

SPI Control Register Definitions

SPI Data Register

The SPI Data register ([Table 63](#)) stores both the outgoing (transmit) data and the incoming (receive) data. Reads from the SPI Data register always return the current contents of the 8-bit shift register. Data is shifted out starting with bit 7. The last bit received resides in bit position 0.

With the SPI configured as a Master, writing a data byte to this register initiates the data transmission. With the SPI configured as a Slave, writing a data byte to this register loads the shift register in preparation for the next data transfer with the external Master. In either the Master or Slave modes, if a transmission is already in progress, writes to this register are ignored and the Overrun error Flag, OVR, is set in the SPI Status register.

When the character length is less than 8 bits (as set by the NUMBITS field in the SPI Mode register), the transmit character must be left justified in the SPI Data register. A received character of less than 8 bits is right justified (last bit received is in bit position 0). For example, if the SPI is configured for 4-bit characters, the transmit characters must be written to SPIDATA[7:4] and the received characters are read from SPIDATA[3:0].

Table 63. SPI Data Register (SPIDATA)

BITS	7	6	5	4	3	2	1	0
FIELD	DATA							
RESET	X							
R/W	R/W							
ADDR	F60H							

DATA—Data
Transmit and/or receive data.

SPI Control Register

The SPI Control register (see [Table 64](#) on page 138) configures the SPI for transmit and receive operations.

Transmit interrupts occur when the TDRE bit of the I²C Status register sets and the TXI bit in the I²C Control register is set. Transmit interrupts occur under the following conditions when the transmit data register is empty:

- The I²C Controller is enabled.
- The first bit of the byte of an address is shifting out and the RD bit of the I²C Status register is deasserted.
- The first bit of a 10-bit address shifts out.
- The first bit of write data shifts out.

► **Note:** *Writing to the I²C Data register always clears the TRDE bit to 0. When TDRE is asserted, the I²C Controller pauses at the beginning of the Acknowledge cycle of the byte currently shifting out until the Data register is written with the next value to send or the STOP or START bits are set indicating the current byte is the last one to send.*

The fourth interrupt source is the baud rate generator. If the I²C Controller is disabled (IEN bit in the I2CCTL register = 0) and the BIRQ bit in the I2CCTL register = 1, an interrupt is generated when the baud rate generator counts down to 1. This allows the I²C baud rate generator to be used by software as a general purpose timer when IEN = 0.

Software Control of I²C Transactions

Software can control I²C transactions by using the I²C Controller interrupt, by polling the I²C Status register or by DMA. Note that not all products include a DMA Controller.

To use interrupts, the I²C interrupt must be enabled in the Interrupt Controller. The TXI bit in the I²C Control register must be set to enable transmit interrupts.

To control transactions by polling, the interrupt bits (TDRE, RDRF and NCKI) in the I²C Status register should be polled. The TDRE bit asserts regardless of the state of the TXI bit.

Either or both transmit and receive data movement can be controlled by the DMA Controller. The DMA Controller channel(s) must be initialized to select the I²C transmit and receive requests. Transmit DMA requests require that the TXI bit in the I²C Control register be set.



Caution: *A transmit (write) DMA operation hangs if the slave responds with a Not Acknowledge before the last byte has been sent. After receiving the Not Acknowledge, the I²C Controller sets the NCKI bit in the Status register and pauses until either the STOP or START bits in the Control register are set.*

Analog-to-Digital Converter

Overview

The Analog-to-Digital Converter (ADC) converts an analog input signal to a 10-bit binary number. The features of the sigma-delta ADC include:

- 12 analog input sources are multiplexed with general-purpose I/O ports
- Interrupt upon conversion complete
- Internal voltage reference generator
- Direct Memory Access (DMA) controller can automatically initiate data conversion and transfer of the data from 1 to 12 of the analog inputs

Architecture

[Figure 34](#) displays the three major functional blocks (converter, analog multiplexer, and voltage reference generator) of the ADC. The ADC converts an analog input signal to its digital representation. The 12-input analog multiplexer selects one of the 12 analog input sources. The ADC requires an input reference voltage for the conversion. The voltage reference for the conversion may be input through the external VREF pin or generated internally by the voltage reference generator.

Figure 44 displays the maximum active mode current consumption across the full operating temperature range of the device and versus the system clock frequency. All GPIO pins are configured as outputs and driven High.

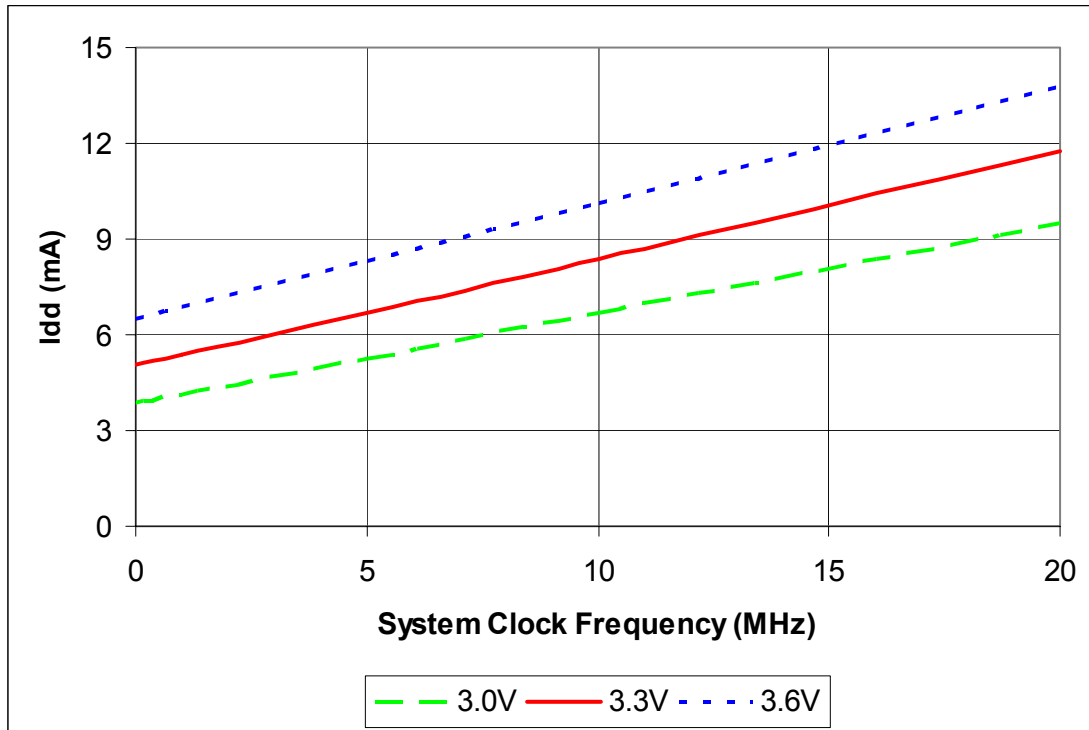


Figure 44. Maximum Active Mode I_{dd} Versus System Clock Frequency

UART Timing

Figure 56 and Table 120 provide timing information for UART pins for the case where the Clear To Send input pin ($\overline{\text{CTS}}$) is used for flow control. In this example, it is assumed that the Driver Enable polarity has been configured to be Active Low and is represented here by $\overline{\text{DE}}$. The $\overline{\text{CTS}}$ to $\overline{\text{DE}}$ assertion delay (T_1) assumes the UART Transmit Data register has been loaded with data prior to $\overline{\text{CTS}}$ assertion.

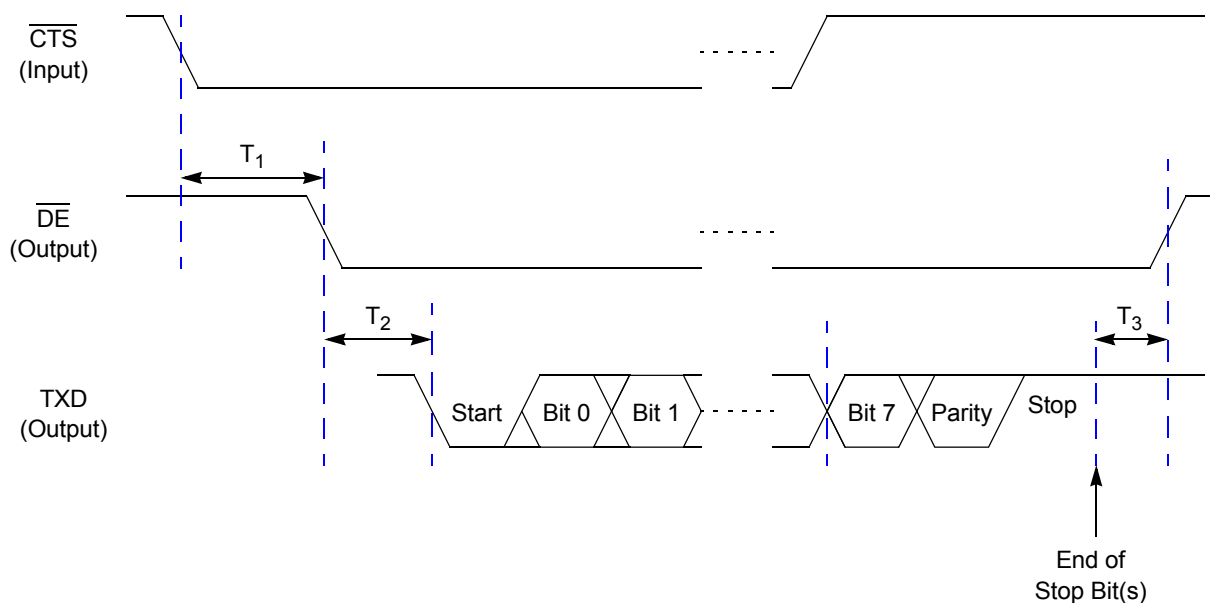


Figure 56. UART Timing with $\overline{\text{CTS}}$

Table 120. UART Timing with $\overline{\text{CTS}}$

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
T_1	$\overline{\text{CTS}}$ Fall to $\overline{\text{DE}}$ Assertion Delay	2 * XIN period	2 * XIN period + 1 Bit period
T_2	$\overline{\text{DE}}$ Assertion to TXD Falling Edge (Start) Delay	1 Bit period	1 Bit period + 1 * XIN period
T_3	End of Stop Bit(s) to $\overline{\text{DE}}$ Deassertion Delay	1 * XIN period	2 * XIN period

Table 128. CPU Control Instructions

Mnemonic	Operands	Instruction
STOP	—	STOP Mode
WDT	—	Watchdog Timer Refresh

Table 129. Load Instructions

Mnemonic	Operands	Instruction
CLR	dst	Clear
LD	dst, src	Load
LDC	dst, src	Load Constant to/from Program Memory
LDCI	dst, src	Load Constant to/from Program Memory and Auto-Increment Addresses
LDE	dst, src	Load External Data to/from Data Memory
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses
LDWX	dst, src	Load Word using Extended Addressing
LDX	dst, src	Load using Extended Addressing
LEA	dst, X(src)	Load Effective Address
POP	dst	Pop
POPX	dst	Pop using Extended Addressing
PUSH	src	Push
PUSHX	src	Push using Extended Addressing

Table 130. Logical Instructions

Mnemonic	Operands	Instruction
AND	dst, src	Logical AND
ANDX	dst, src	Logical AND using Extended Addressing
COM	dst	Complement
OR	dst, src	Logical OR
ORX	dst, src	Logical OR using Extended Addressing

Table 133. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
LDC dst, src	$\text{dst} \leftarrow \text{src}$	r	lrr	C2	-	-	-	-	-	-	2	5
		lr	lrr	C5							2	9
		lrr	r	D2							2	5
LDCI dst, src	$\text{dst} \leftarrow \text{src}$ $\text{r} \leftarrow \text{r} + 1$ $\text{rr} \leftarrow \text{rr} + 1$	lr	lrr	C3	-	-	-	-	-	-	2	9
		lrr	lr	D3							2	9
LDE dst, src	$\text{dst} \leftarrow \text{src}$	r	lrr	82	-	-	-	-	-	-	2	5
		lrr	r	92							2	5
LDEI dst, src	$\text{dst} \leftarrow \text{src}$ $\text{r} \leftarrow \text{r} + 1$ $\text{rr} \leftarrow \text{rr} + 1$	lr	lrr	83	-	-	-	-	-	-	2	9
		lrr	lr	93							2	9
LDWX dst, src	$\text{dst} \leftarrow \text{src}$	ER	ER	1F E8	-	-	-	-	-	-	5	4
LDX dst, src	$\text{dst} \leftarrow \text{src}$	r	ER	84	-	-	-	-	-	-	3	2
		lr	ER	85							3	3
		R	IRR	86							3	4
		IR	IRR	87							3	5
		r	X(rr)	88							3	4
		X(rr)	r	89							3	4
		ER	r	94							3	2
		ER	lr	95							3	3
		IRR	R	96							3	4
		IRR	IR	97							3	5
		ER	ER	E8							4	2
		ER	IM	E9							4	2
LEA dst, X(src)	$\text{dst} \leftarrow \text{src} + \text{X}$	r	X(r)	98	-	-	-	-	-	-	3	3
		rr	X(rr)	99							3	5
MULT dst	$\text{dst}[15:0] \leftarrow \text{dst}[15:8] * \text{dst}[7:0]$	RR		F4	-	-	-	-	-	-	2	8
NOP	No operation			0F	-	-	-	-	-	-	1	2

Figure 64 displays the 44-pin Plastic Lead Chip Carrier (PLCC) package available for the Z8X1621, Z8X2421, Z8X3221, Z8X4821, and Z8X6421 devices.

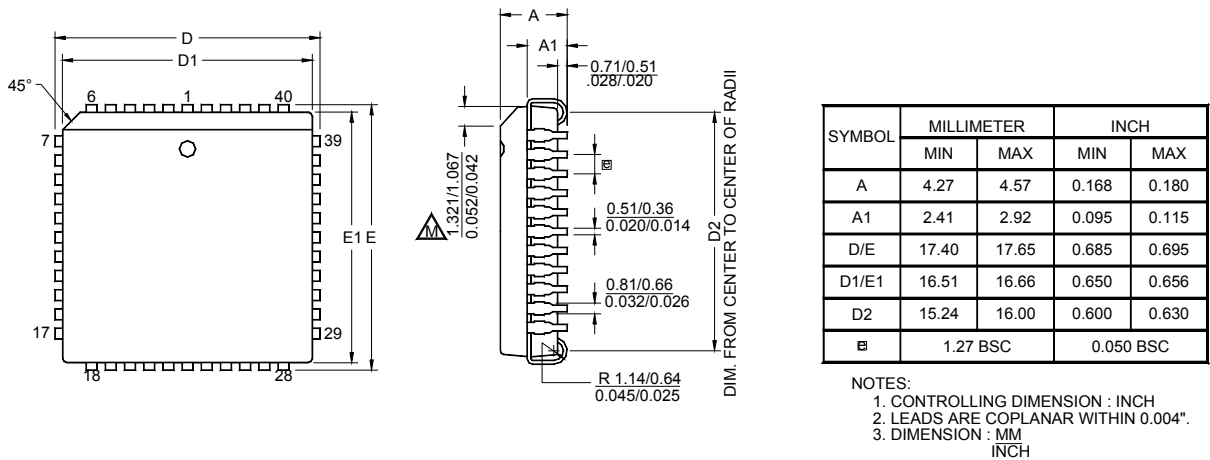


Figure 64. 44-Lead Plastic Lead Chip Carrier Package (PLCC)

Figure 64 displays the 64-pin Low-Profile Quad Flat Package (LQFP) available for the Z8X1622, Z8X2422, Z8X3222, Z8X4822, and Z8X6422 devices.

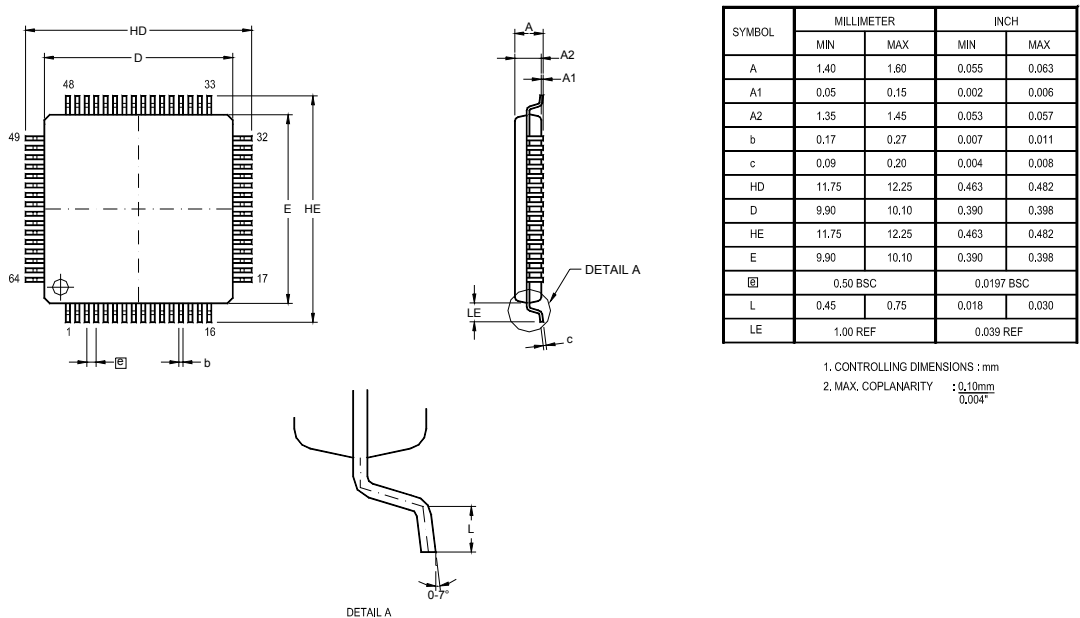


Figure 65. 64-Lead Low-Profile Quad Flat Package (LQFP)

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I ² C	SPI	UARTs with IrDA	Description
Z8F242x with 24 KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0 °C to 70 °C										
Z8F2421PM020SC	24 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F2421AN020SC	24 KB	2 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F2421VN020SC	24 KB	2 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F2422AR020SC	24 KB	2 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F2422VS020SC	24 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Extended Temperature: –40 °C to 105 °C										
Z8F2421PM020EC	24 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F2421AN020EC	24 KB	2 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F2421VN020EC	24 KB	2 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F2422AR020EC	24 KB	2 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F2422VS020EC	24 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Automotive/Industrial Temperature: –40 °C to 125 °C										
Z8F2421PM020AC	24 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F2421AN020AC	24 KB	2 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F2421VN020AC	24 KB	2 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F2422AR020AC	24 KB	2 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F2422VS020AC	24 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I ² C	SPI	UARTs with IrDA	Description
Z8F162x with 16 KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0 °C to 70 °C										
Z8F1621PM020SC	16 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F1621AN020SC	16 KB	2 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F1621VN020SC	16 KB	2 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F1622AR020SC	16 KB	2 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F1622VS020SC	16 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Extended Temperature: –40 °C to +105 °C										
Z8F1621PM020EC	16 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F1621AN020EC	16 KB	2 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F1621VN020EC	16 KB	2 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F1622AR020EC	16 KB	2 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F1622VS020EC	16 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Automotive/Industrial Temperature: –40 °C to +125 °C										
Z8F1621PM020AC	16 KB	2 KB	29	23	3	8	1	1	2	PDIP 40-pin package
Z8F1621AN020AC	16 KB	2 KB	31	23	3	8	1	1	2	LQFP 44-pin package
Z8F1621VN020AC	16 KB	2 KB	31	23	3	8	1	1	2	PLCC 44-pin package
Z8F1622AR020AC	16 KB	2 KB	46	24	4	12	1	1	2	LQFP 64-pin package
Z8F1622VS020AC	16 KB	2 KB	46	24	4	12	1	1	2	PLCC 68-pin package
Z8F64200100KITG										Development Kit
ZUSBSC00100ZACG										USB Smart Cable Accessory Kit
ZUSBOPTSC01ZACG										Opto-Isolated USB Smart Cable Accessory Kit

Note: Replace C with G for lead-free packaging.

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