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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	46
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f6422vs020sc00tr

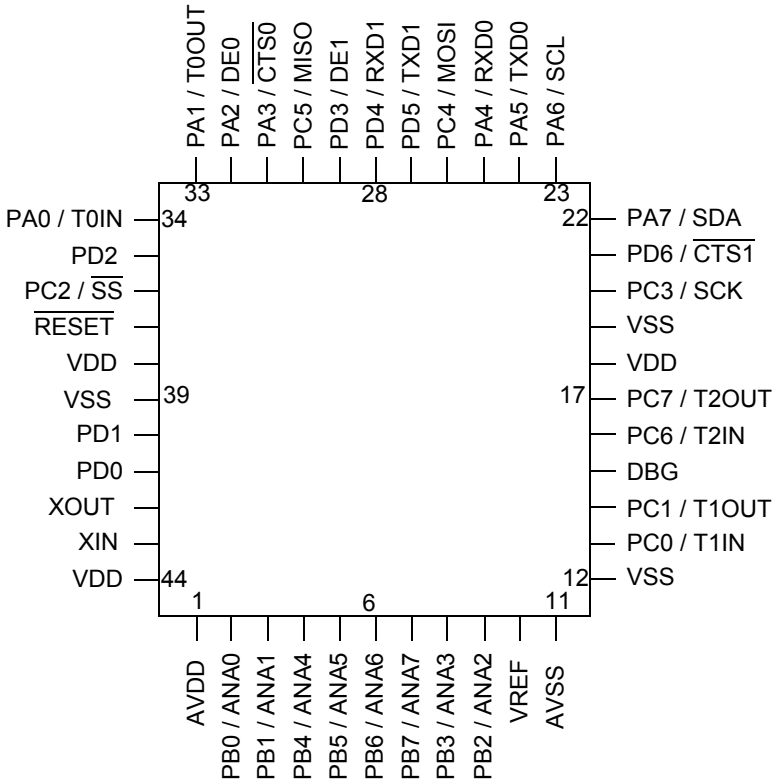


Figure 4. Z8 Encore! XP 64K Series Flash Microcontrollers in 44-Pin Low-Profile Quad Flat Package (LQFP)

Table 4. Pin Characteristics of the Z8 Encore! XP 64K Series Flash Microcontrollers

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tri-State Output	Internal Pull-up or Pull-down	Schmitt-Trigger Input	Open Drain Output
AVSS	N/A	N/A	N/A	N/A	No	No	N/A
AVDD	N/A	N/A	N/A	N/A	No	No	N/A
DBG	I/O	I	N/A	Yes	No	Yes	Yes
VSS	N/A	N/A	N/A	N/A	No	No	N/A
PA[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PB[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PC[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PD[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PE7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PF[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PG[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PH[3:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
RESET	I	I	Low	N/A	Pull-up	Yes	N/A
VDD	N/A	N/A	N/A	N/A	No	No	N/A
XIN	I	I	N/A	N/A	No	No	N/A
XOUT	O	O	N/A	Yes, in STOP mode	No	No	No

Note: *x* represents integer 0, 1,... to indicate multiple pins with symbol mnemonics that differ only by the integer.

DMA_ADC Control
DMAACTL (FBEH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: ADC Analog Input Number
  0000 = Analog input 0 updated
  0001 = Analog input 0-1 updated
  0010 = Analog input 0-2 updated
  0011 = Analog input 0-3 updated
  0100 = Analog input 0-4 updated
  0101 = Analog input 0-5 updated
  0100 = Analog input 0-6 updated
  0101 = Analog input 0-7 updated
  1000 = Analog input 0-8 updated
  1001 = Analog input 0-9 updated
  1010 = Analog input 0-10 updated
  1011 = Analog inputs 0-11 updated
  11xx = Reserved
- D4: Reserved
- D3: Interrupt request enable
  0 = DMA_ADC does not generate interrupt requests
  1 = DMA_ADC generates interrupt requests after last analog input
- D7: DMA_ADC Enable
  0 = DMA_ADC is disabled
  1 = DMA_ADC is enabled

DMA Status
DMAA_STAT (FBFH - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: DMA0 Interrupt Request Indicator
  0 = DMA0 is not the source of the IRQ
  1 = DMA0 is the source of the IRQ
- D1: DMA1 Interrupt Request Indicator
  0 = DMA1 is not the source of the IRQ
  1 = DMA1 is the source of the IRQ
- D2: DMA_ADC Interrupt Request
  0 = DMA_ADC is not the source of the IRQ
  1 = DMA_ADC is the source of the IRQ
- D3: Reserved
- D7: Current ADC analog input
  Identifies the analog input the ADC is currently converting

Interrupt Request 0
IRQ0 (FC0H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: ADC Interrupt Request
- D1: SPI Interrupt Request
- D2: I2C Interrupt Request
- D3: UART 0 Transmitter Interrupt
- D4: UART 0 Receiver Interrupt Request
- D5: Timer 0 Interrupt Request
- D6: Timer 1 Interrupt Request
- D7: Timer 2 Interrupt Request

For all of the above peripherals:
0 = Peripheral IRQ is not pending
1 = Peripheral IRQ is awaiting service

IRQ0 Enable High Bit
IRQ0ENH (FC1H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: ADC IRQ Enable Hit Bit
- D1: SPI IRQ Enable High Bit
- D2: I2C IRQ Enable High Bit
- D3: UART 0 Transmitter IRQ Enable
- D4: UART 0 Receiver IRQ Enable High
- D5: Timer 0 IRQ Enable High Bit
- D6: Timer 1 IRQ Enable High Bit
- D7: Timer 2 IRQ Enable High Bit

Watchdog Timer Control
WDTCTL (FF0H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: SM Configuration Indicator
- D1: Reserved
- D2: EXT
  0 = Reset not generated by $\overline{\text{RESET}}$ pin
  1 = Reset generated by $\overline{\text{RESET}}$ pin
- D3: WDT
  0 = WDT timeout has not occurred
  1 = WDT timeout occurred
- D4: STOP
  0 = SMR has not occurred
  1 = SMR has occurred
- D5: POR
  0 = POR has not occurred
  1 = POR has occurred

Watchdog Timer Reload Upper Byte
WDTU (FF1H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: WDT reload value [23:16]

Watchdog Timer Reload Middle Byte
WDTH (FF2 H- Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: WDT reload value [15:8]

Watchdog Timer Reload Low Byte
WDTL (FF3H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: WDT reload value [7:0]

Flash Control
FCTL (FF8H - Write Only)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: Flash Command
  73H = First unlock command
  8CH = Second unlock command
  95H = Page erase command
  63H = Mass erase command
  5EH = Flash Sector Protect reg select

Flash Status
FSTAT (FF8H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D3: Flash Controller Status
  00_0000 = Flash controller locked
  00_0001 = First unlock received
  00_0010 = Second unlock received
  00_0011 = Flash controller unlocked
  00_0100 = Flash Sector Protect register selected
  00_1xxx = Programming in progress
  01_0xxx = Page erase in progress
  10_0xxx = Mass erase in progress
- D4–D6: Reserved

Page Select
FPS (FF9H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D6: Page Select [6:0]
  Identifies the Flash memory page for Page Erase operation.
- D7: Information Area Enable
  0 = Information Area access is disabled
  1 = Information Area access is enabled

Flash Sector Protect
FPROT (FF9H - Read/Write to 1's)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: Flash Sector Protect [7:0]
  0 = Sector can be programmed or erased from user code
  1 = Sector is protected and cannot be programmed or erased from user code

Flash Frequency High Byte
FFREQH (FFAH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: Flash Frequency value [15:8]

Flash Frequency Low Byte
FFREQL (FFBH - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0–D7: Flash Frequency value [7:0]

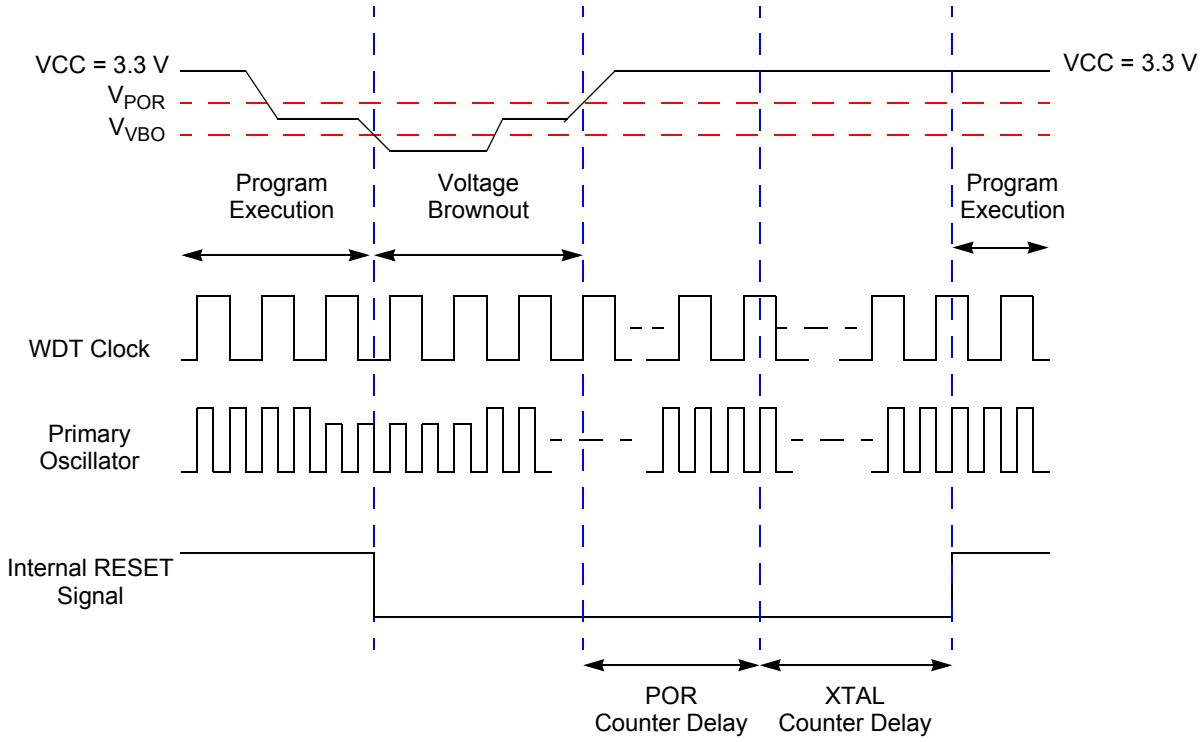


Figure 9. Voltage Brownout Reset Operation

Watchdog Timer Reset

If the device is in normal or HALT mode, the Watchdog Timer can initiate a system reset at time-out if the WDT_RES Option Bit is set to 1. This capability is the default (unprogrammed) setting of the WDT_RES Option Bit. The WDT status bit in the WDT Control register is set to signify that the reset was initiated by the Watchdog Timer.

External Pin Reset

The $\overline{\text{RESET}}$ pin has a Schmitt-triggered input, an internal pull-up, an analog filter and a digital filter to reject noise. Once the $\overline{\text{RESET}}$ pin is asserted for at least 4 system clock cycles, the devices progress through the system reset sequence. While the $\overline{\text{RESET}}$ input pin is asserted Low, the 64K Series devices continue to be held in the Reset state. If the $\overline{\text{RESET}}$ pin is held Low beyond the system reset time-out, the devices exit the Reset state immediately following $\overline{\text{RESET}}$ pin deassertion. Following a system reset initiated by the external $\overline{\text{RESET}}$ pin, the EXT status bit in the Watchdog Timer Control (WDTCTL) register is set to 1.

Table 11. Port Availability by Device and Package Type (Continued)

Device	Packages	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Port H
Z8X4823	80-pin	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[3:0]
Z8X6421	40-pin	[7:0]	[7:0]	[6:0]	[6:3, 1:0]	-	-	-	-
Z8X6421	44-pin	[7:0]	[7:0]	[7:0]	[6:0]	-	-	-	-
Z8X6422	64- and 68-pin	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[7]	[3]	[3:0]
Z8X6423	80-pin	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[3:0]

Architecture

Figure 10 displays a simplified block diagram of a GPIO port pin. In Figure 10, the ability to accommodate alternate functions and variable port current drive strength are not illustrated.

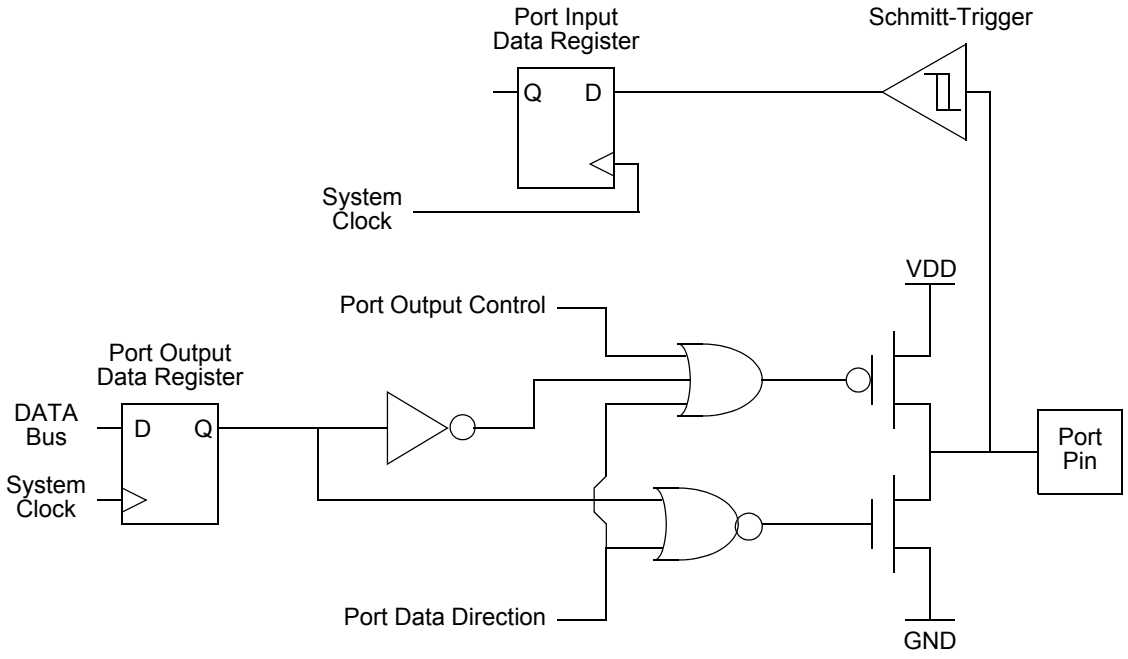


Figure 10. GPIO Port Pin Block Diagram

The timer continues counting up to the 16-bit Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt and continues counting.

Follow the steps below for configuring a timer for CAPTURE mode and initiating the count:

1. Write to the Timer Control 1 register to:
   – Disable the timer
   – Configure the timer for CAPTURE mode.
   – Set the prescale value.
   – Set the Capture edge (rising or falling) for the Timer Input.
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
4. Clear the Timer PWM High and Low Byte registers to 0000H. This allows the software to determine if interrupts were generated by either a capture event or a reload. If the PWM High and Low Byte registers still contain 0000H after the interrupt, then the interrupt was generated by a Reload.
5. If desired, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
6. Configure the associated GPIO port pin for the Timer Input alternate function.
7. Write to the Timer Control 1 register to enable the timer and initiate counting.

In CAPTURE mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

COMPARE Mode

In COMPARE mode, the timer counts up to the 16-bit maximum Compare value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the Compare value, the timer generates an interrupt and counting continues (the timer value is not reset to 0001H). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) upon Compare.

If the Timer reaches FFFFH, the timer rolls over to 0000H and continue counting.

– Set or clear the CTSE bit to enable or disable control from the remote receiver using the $\overline{\text{CTS}}$ pin.

5. Check the TDRE bit in the UART Status 0 register to determine if the Transmit Data register is empty (indicated by a 1). If empty, continue to step 6. If the Transmit Data register is full (indicated by a 0), continue to monitor the TDRE bit until the Transmit Data register becomes available to receive new data.
6. Write the UART Control 1 register to select the outgoing address bit.
7. Set the MULTIPROCESSOR Bit Transmitter (MPBT) if sending an address byte, clear it if sending a data byte.
8. Write the data byte to the UART Transmit Data register. The transmitter automatically transfers the data to the Transmit Shift register and transmits the data.
9. If desired and MULTIPROCESSOR mode is enabled, make any changes to the MULTIPROCESSOR Bit Transmitter (MPBT) value.
10. To transmit additional bytes, return to step 5.

Transmitting Data using the Interrupt-Driven Method

The UART transmitter interrupt indicates the availability of the Transmit Data register to accept new data for transmission. Follow the steps below to configure the UART for interrupt-driven data transmission:

1. Write to the UART Baud Rate High and Low Byte registers to set the desired baud rate.
2. Enable the UART pin functions by configuring the associated GPIO Port pins for alternate function operation.
3. Execute a DI instruction to disable interrupts.
4. Write to the Interrupt control registers to enable the UART Transmitter interrupt and set the desired priority.
5. If MULTIPROCESSOR mode is desired, write to the UART Control 1 register to enable MULTIPROCESSOR (9-bit) mode functions.
6. Set the MULTIPROCESSOR Mode Select (MPEN) to Enable MULTIPROCESSOR mode.
7. Write to the UART Control 0 register to:
   – Set the transmit enable bit (TEN) to enable the UART for data transmission.
   – Enable parity, if desired and if MULTIPROCESSOR mode is not enabled, and select either even or odd parity.
   – Set or clear the CTSE bit to enable or disable control from the remote receiver via the $\overline{\text{CTS}}$ pin.

register. The IRQE, PHASE, CLKPOL, WOR bits in the SPICTL register and the NUMBITS field in the SPIMODE register must be set to be consistent with the other SPI devices. The STR bit in the SPICTL register may be used if desired to force a "startup" interrupt. The BIRQ bit in the SPICTL register and the SSV bit in the SPIMODE register are not used in SLAVE mode. The SPI baud rate generator is not used in SLAVE mode so the SPIBRH and SPIBRL registers need not be initialized.

If the slave has data to send to the master, the data must be written to the SPIDAT register before the transaction starts (first edge of SCK when $\overline{SS}$ is asserted). If the SPIDAT register is not written prior to the slave transaction, the MISO pin outputs whatever value is currently in the SPIDAT register.

Due to the delay resulting from synchronization of the SPI input signals to the internal system clock, the maximum SPICLK baud rate that can be supported in SLAVE mode is the system clock frequency (XIN) divided by 8. This rate is controlled by the SPI master.

Error Detection

The SPI contains error detection logic to support SPI communication protocols and recognize when communication errors have occurred. The SPI Status register indicates when a data transmission error has been detected.

Overrun (Write Collision)

An overrun error (write collision) indicates a write to the SPI Data register was attempted while a data transfer is in progress (in either MASTER or SLAVE modes). An overrun sets the OVR bit in the SPI Status register to 1. Writing a 1 to OVR clears this error Flag. The data register is not altered when a write occurs while data transfer is in progress.

Mode Fault (Multi-Master Collision)

A mode fault indicates when more than one Master is trying to communicate at the same time (a multi-master collision). The mode fault is detected when the enabled Master's $\overline{SS}$ pin is asserted. A mode fault sets the COL bit in the SPI Status register to 1. Writing a 1 to COL clears this error Flag.

Slave Mode Abort

In SLAVE mode of operation if the $\overline{SS}$ pin deasserts before all bits in a character have been transferred, the transaction is aborted. When this condition occurs the ABT bit is set in the SPISTAT register as well as the IRQ bit (indicating the transaction is complete). The next time $\overline{SS}$ asserts, the MISO pin outputs SPIDAT[7], regardless of where the previous transaction left off. Writing a 1 to ABT clears this error Flag.

SPI Interrupts

When SPI interrupts are enabled, the SPI generates an interrupt after character transmission/reception completes in both MASTER and SLAVE modes. A character can be

Table 74. I²C Baud Rate Low Byte Register (I2CBRL)

BITS	7	6	5	4	3	2	1	0
FIELD	BRL							
RESET	FFH							
R/W	R/W							
ADDR	F54H							

BRL = I²C Baud Rate Low Byte
Least significant byte, BRG[7:0], of the I²C Baud Rate Generator's reload value.

Note: *If the DIAG bit in the I²C Diagnostic Control Register is set to 1, a read of the I2CBRL register returns the current value of the I²C Baud Rate Counter[7:0].*

I²C Diagnostic State Register

The I²C Diagnostic State register (Table 75) provides observability of internal state. This is a read only register used for I²C diagnostics and manufacturing test.

Table 75. I²C Diagnostic State Register (I2CDST)

BITS	7	6	5	4	3	2	1	0
FIELD	SCLIN	SDAIN	STPCNT	TXRXSTATE				
RESET	X		0					
R/W	R							
ADDR	F55H							

SCLIN—Value of Serial Clock input signal

SDAIN—Value of the Serial Data input signal

STPCNT—Value of the internal Stop Count control signal

TXRXSTATE—Value of the internal I²C state machine

Configuring DMA0 and DMA1 for Data Transfer

Follow the steps below to configure and enable DMA0 or DMA1:

1. Write to the DMA*x* I/O Address register to set the Register File address identifying the on-chip peripheral control register. The upper nibble of the 12-bit address for on-chip peripheral control registers is always FH. The full address is {FH, DMA*x*_IO[7:0]}.
2. Determine the 12-bit Start and End Register File addresses. The 12-bit Start Address is given by {DMA*x*_H[3:0], DMA_START[7:0]}. The 12-bit End Address is given by {DMA*x*_H[7:4], DMA_END[7:0]}.
3. Write the Start and End Register File address high nibbles to the DMA*x* End/Start Address High Nibble register.
4. Write the lower byte of the Start Address to the DMA*x* Start/Current Address register.
5. Write the lower byte of the End Address to the DMA*x* End Address register.
6. Write to the DMA*x* Control register to complete the following:
   – Select loop or single-pass mode operation
   – Select the data transfer direction (either from the Register File RAM to the on-chip peripheral control register; or from the on-chip peripheral control register to the Register File RAM)
   – Enable the DMA*x* interrupt request, if desired
   – Select Word or Byte mode
   – Select the DMA*x* request trigger
   – Enable the DMA*x* channel

DMA_ADC Operation

DMA_ADC transfers data from the ADC to the Register File. The sequence of operations in a DMA_ADC data transfer is:

1. ADC completes conversion on the current ADC input channel and signals the DMA controller that two-bytes of ADC data are ready for transfer.
2. DMA_ADC requests control of the system bus (address and data) from the eZ8 CPU.
3. After the eZ8 CPU acknowledges the bus request, DMA_ADC transfers the two-byte ADC output value to the Register File and then returns system bus control back to the eZ8 CPU.
4. If the current ADC Analog Input is the highest numbered input to be converted:
   – DMA_ADC resets the ADC Analog Input number to 0 and initiates data conversion on ADC Analog Input 0.
   – If configured to generate an interrupt, DMA_ADC sends an interrupt request to the Interrupt Controller

0101 = ADC Analog Inputs 0-5 updated.
0110 = ADC Analog Inputs 0-6 updated.
0111 = ADC Analog Inputs 0-7 updated.
1000 = ADC Analog Inputs 0-8 updated.
1001 = ADC Analog Inputs 0-9 updated.
1010 = ADC Analog Inputs 0-10 updated.
1011 = ADC Analog Inputs 0-11 updated.
1100-1111 = Reserved.

DMA Status Register

The DMA Status register (Table 85 on page 173) indicates the DMA channel that generated the interrupt and the ADC Analog Input that is currently undergoing conversion. Reads from this register reset the Interrupt Request Indicator bits (IRQA, IRQ1, and IRQ0) to 0. Therefore, software interrupt service routines that read this register must process all three interrupt sources from the DMA.

Table 85. DMA_ADC Status Register (DMAA_STAT)

BITS	7	6	5	4	3	2	1	0
FIELD	CADC[3:0]				Reserved	IRQA	IRQ1	IRQ0
RESET	0							
R/W	R							
ADDR	FBFH							

CADC[3:0]—Current ADC Analog Input
This field identifies the Analog Input that the ADC is currently converting.

Reserved
This bit is reserved and must be 0.

IRQA—DMA_ADC Interrupt Request Indicator
This bit is automatically reset to 0 each time a read from this register occurs.
0 = DMA_ADC is not the source of the interrupt from the DMA Controller.
1 = DMA_ADC completed transfer of data from the last ADC Analog Input and generated an interrupt.

IRQ1—DMA1 Interrupt Request Indicator
This bit is automatically reset to 0 each time a read from this register occurs.
0 = DMA1 is not the source of the interrupt from the DMA Controller.
1 = DMA1 completed transfer of data to/from the End Address and generated an interrupt.

IRQ0—DMA0 Interrupt Request Indicator
This bit is automatically reset to 0 each time a read from this register occurs.

While the Flash Controller programs the Flash memory, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. Interrupts that occur when a Programming operation is in progress are serviced once the Programming operation is complete. To exit Programming mode and lock the Flash Controller, write 00H to the Flash Control register.

User code cannot program Flash Memory on a page that lies in a protected sector. When user code writes memory locations, only addresses located in the unlocked page are programmed. Memory writes outside of the unlocked page are ignored.

Caution: *Each memory location must not be programmed more than twice before an erase occurs.*

Follow the steps below to program the Flash from user code:

1. Write 00H to the Flash Control register to reset the Flash Controller.
2. Write the page of memory to be programmed to the Page Select register.
3. Write the first unlock command 73H to the Flash Control register.
4. Write the second unlock command 8CH to the Flash Control register.
5. Re-write the page written in step 2 to the Page Select register.
6. Write Flash Memory using LDC or LDCI instructions to program the Flash.
7. Repeat step 6 to program additional memory locations on the same page.
8. Write 00H to the Flash Control register to lock the Flash Controller.

Page Erase

The Flash memory can be erased one page (512 bytes) at a time. Page Erasing the Flash memory sets all bytes in that page to the value FFH. The Page Select register identifies the page to be erased. While the Flash Controller executes the Page Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. The eZ8 CPU resumes operation after the Page Erase operation completes. Interrupts that occur when the Page Erase operation is in progress are serviced once the Page Erase operation is complete. When the Page Erase operation is complete, the Flash Controller returns to its locked state. Only pages located in unprotected sectors can be erased.

Follow the steps below to perform a Page Erase operation:

1. Write 00H to the Flash Control register to reset the Flash Controller.
2. Write the page to be erased to the Page Select register.
3. Write the first unlock command 73H to the Flash Control register.
4. Write the second unlock command 8CH to the Flash Control register.

finish the interrupt service routine it may be in and return the BRK instruction. When the CPU returns to the BRK instruction it was previously looping on, it automatically sets the DBGMODE bit and enter DEBUG mode.

Software detects that the majority of the OCD commands are still disabled when the eZ8™ CPU is looping on a BRK instruction. The eZ8 CPU must be stopped and the part must be in DEBUG mode before these commands can be issued.

Breakpoints in Flash Memory

The BRK instruction is opcode 00H, which corresponds to the fully programmed state of a byte in Flash memory. To implement a Breakpoint, write 00H to the desired address, overwriting the current instruction. To remove a Breakpoint, the corresponding page of Flash memory must be erased and reprogrammed with the original data.

On-Chip Debugger Commands

The host communicates to the On-Chip Debugger by sending OCD commands using the DBG interface. During normal operation, only a subset of the OCD commands are available. In DEBUG mode, all OCD commands become available unless the user code and control registers are protected by programming the Read Protect Option Bit (RP). The Read Protect Option Bit prevents the code in memory from being read out of the 64K Series products. When this option is enabled, several of the OCD commands are disabled. Table 101 contains a summary of the On-Chip Debugger commands. Each OCD command is described in detail in the bulleted list following Table 101.
Table 101 indicates those commands that operate when the device is not in DEBUG mode (normal operation) and those commands that are disabled by programming the Read Protect Option Bit.

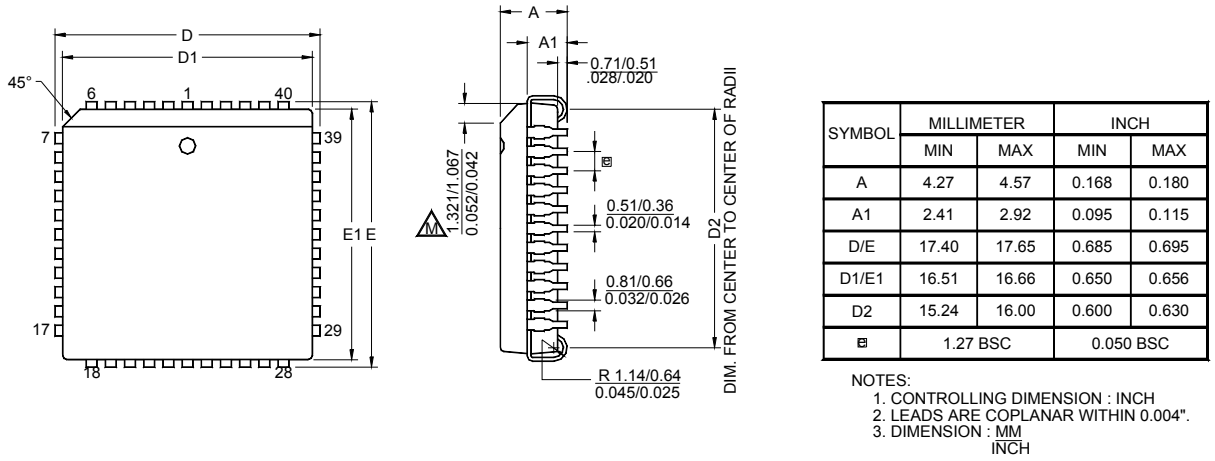
Table 101. On-Chip Debugger Commands

Debug Command	Command Byte	Enabled when NOT in DEBUG mode?	Disabled by Read Protect Option Bit
Read OCD Revision	00H	Yes	-
Read OCD Status Register	02H	Yes	-
Read Runtime Counter	03H	-	-
Write OCD Control Register	04H	Yes	Cannot clear DBGMODE bit
Read OCD Control Register	05H	Yes	-

Table 112. Analog-to-Digital Converter Electrical Characteristics and Timing

Symbol	Parameter	V_{DD} = 3.0–3.6 V T_A = –40 °C to 125 °C			Units	Conditions
		Minimum	Typical	Maximum		
	Resolution	10	–	–	bits	External V_{REF} = 3.0 V;
	Differential Nonlinearity (DNL)	-1.0		+1.0	lsb	Guaranteed by design
	Integral Nonlinearity (INL)	-3.0	±1.0	3.0	lsb	External V_{REF} = 3.0 V
	DC Offset Error	-35	–	25	mV	
	DC Offset Error	-50	–	25	mV	44-pin LQFP, 44-pin PLCC, and 68-pin PLCC packages.
V_{REF}	Internal Reference Voltage	1.9	2.0	2.4	V	V_{DD} = 3.0 - 3.6 V T_A = -40 °C to 105 °C
VC_{REF}	Voltage Coefficient of Internal Reference Voltage	–	78	–	mV/V	V_{REF} variation as a function of AVDD.
TC_{REF}	Temperature Coefficient of Internal Reference Voltage	–	1	–	mV/°C	
	Single-Shot Conversion Period	–	5129	–	cycles	System clock cycles
	Continuous Conversion Period	–	256	–	cycles	System clock cycles
R_S	Analog Source Impedance	–	–	150	Ω	Recommended
Zin	Input Impedance		150		kΩ	
V_{REF}	External Reference Voltage			AVDD	V	AVDD <= VDD. When using an external reference voltage, decoupling capacitance should be placed from VREF to AVSS.
I_{REF}	Current draw into VREF pin when driving with external source.		25.0	40.0	µA	

Figure 64 displays the 44-pin Plastic Lead Chip Carrier (PLCC) package available for the Z8X1621, Z8X2421, Z8X3221, Z8X4821, and Z8X6421 devices.

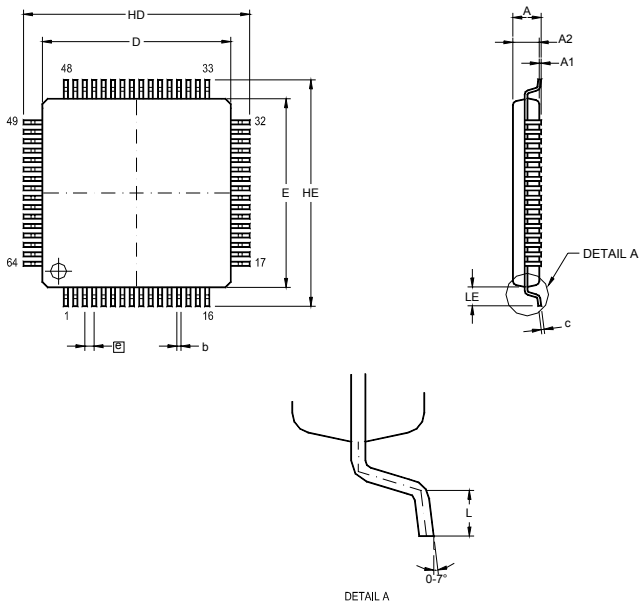


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 64. 44-Lead Plastic Lead Chip Carrier Package (PLCC)

Figure 64 displays the 64-pin Low-Profile Quad Flat Package (LQFP) available for the Z8X1622, Z8X2422, Z8X3222, Z8X4822, and Z8X6422 devices.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
HD	11.75	12.25	0.463	0.482
D	9.90	10.10	0.390	0.398
HE	11.75	12.25	0.463	0.482
E	9.90	10.10	0.390	0.398
e	0.50 BSC		0.0197 BSC	
L	0.45	0.75	0.018	0.030
LE	1.00 REF		0.039 REF	

1. CONTROLLING DIMENSIONS : mm
2. MAX. COPLANARITY : 0.10mm / 0.004"

Figure 65. 64-Lead Low-Profile Quad Flat Package (LQFP)

Example: Part number Z8F6421AN020SC is an 8-bit microcontroller product in an LQFP package, using 44 pins, operating with a maximum 20 MHz external clock frequency over a 0 ºC to +70 ºC temperature range and built using the Plastic-Standard environmental flow.

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