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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	EBI/EMI, Ethernet, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	104
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	58K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2377fbd144-551

- On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as the system clock. When used as the CPU clock, does not allow CAN and USB to run.
- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal. Can be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- Boundary scan for simplified board testing.
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions.

3. Applications

- Industrial control
- Medical systems
- Protocol converter
- Communications

4. Ordering information

Table 1. Ordering information

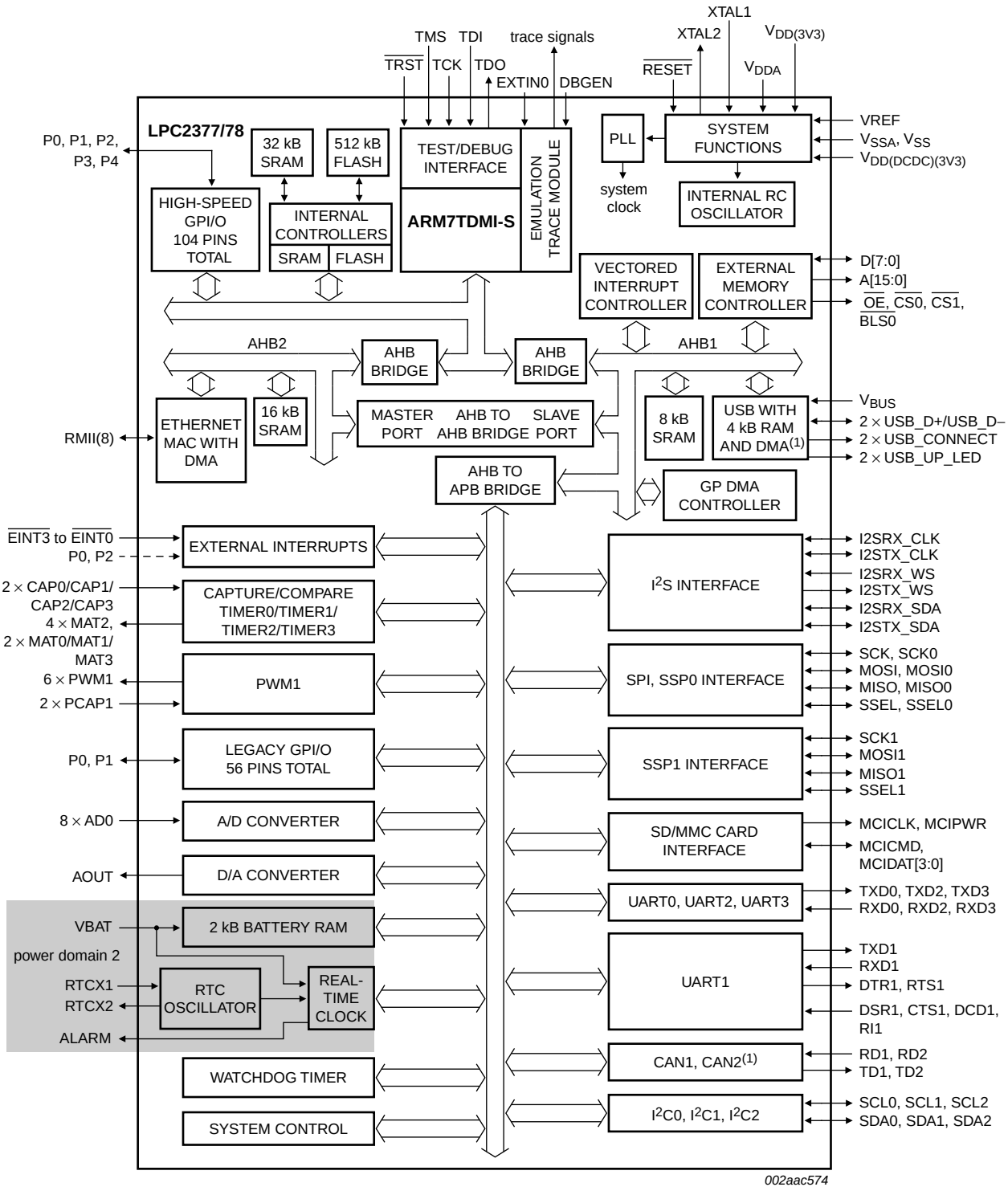
Type number	Package		
	Name	Description	Version
LPC2377FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2378FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					External bus	Ether net	USB device + 4 kB FIFO	CAN channels	SD/ MMC	GP DMA	ADC channels	DAC channels	Temp range
		Local bus	Ethernet buffer	GP/USB	RTC	Total									
LPC2377FBD144	512	32	16	8	2	58	MiniBus: 8 data, 16 address, and 2 chip select lines	RMII	no	-	yes	yes	8	1	–40 °C to +85 °C
LPC2378FBD144	512	32	16	8	2	58	MiniBus: 8 data, 16 address, and 2 chip select lines	RMII	yes	2	yes	yes	8	1	–40 °C to +85 °C

5. Block diagram



(1) LPC2378 only.

Fig 1. LPC2377/78 block diagram

6. Pinning information

6.1 Pinning

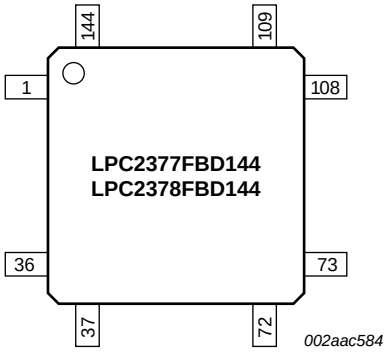


Fig 2. LPC2377/78 pinning

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0[9]/ I2STX_SDA/ MOSI1/MAT2[3]	109[1]	I/O	**P0[9] —** General purpose digital input/output pin.
		I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
		I/O	**MOSI1 —** Master Out Slave In for SSP1.
		O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	69[1]	I/O	**P0[10] —** General purpose digital input/output pin.
		O	**TXD2 —** Transmitter output for UART2.
		I/O	**SDA2 —** I^2C2 data input/output (this pin is not open-drain).
		O	**MAT3[0] —** Match output for Timer 3, channel 0.
P0[11]/RXD2/ SCL2/MAT3[1]	70[1]	I/O	**P0[11] —** General purpose digital input/output pin.
		I	**RXD2 —** Receiver input for UART2.
		I/O	**SCL2 —** I^2C2 clock input/output (this pin is not open-drain).
		O	**MAT3[1] —** Match output for Timer 3, channel 1.
P0[12]/MISO1/ AD0[6]	29[2]	I/O	**P0[12] —** General purpose digital input/output pin.
		I/O	**MISO1 —** Master In Slave Out for SSP1.
		I	**AD0[6] —** A/D converter 0, input 6.
P0[13]/ USB_UP_LED2/ MOSI1/AD0[7]	32[2]	I/O	**P0[13] —** General purpose digital input/output pin.
		O	**USB_UP_LED2 —** USB2 Good Link LED indicator. It is LOW when device is configured (non-control endpoints enabled), or when host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when host is enabled and detects activity on the bus. (LPC2378 only)
		I/O	**MOSI1 —** Master Out Slave In for SSP1.
		I	**AD0[7] —** A/D converter 0, input 7.
P0[14]/ USB_CONNECT2/ SSEL1	48[1]	I/O	**P0[14] —** General purpose digital input/output pin.
		O	**USB_CONNECT2 —** USB2 Soft Connect control. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature. (LPC2378 only)
		I/O	**SSEL1 —** Slave Select for SSP1.
P0[15]/TXD1/ SCK0/SCK	89[1]	I/O	**P0[15] —** General purpose digital input/output pin.
		O	**TXD1 —** Transmitter output for UART1.
		I/O	**SCK0 —** Serial clock for SSP0.
		I/O	**SCK —** Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	90[1]	I/O	**P0[16] —** General purpose digital input/output pin.
		I	**RXD1 —** Receiver input for UART1.
		I/O	**SSEL0 —** Slave Select for SSP0.
		I/O	**SSEL —** Slave Select for SPI.
P0[17]/CTS1/ MISO0/MISO	87[1]	I/O	**P0[17] —** General purpose digital input/output pin.
		I	**CTS1 —** Clear to Send input for UART1.
		I/O	**MISO0 —** Master In Slave Out for SSP0.
		I/O	**MISO —** Master In Slave Out for SPI.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0[28]/SCL0	34[4]	I/O	**P0[28] —** General purpose digital input/output pin. Output is open-drain.
		I/O	**SCL0 —** I^2C0 clock input/output. Open-drain output (for I^2C-bus compliance).
P0[29]/USB_D+1	42[5]	I/O	**P0[29] —** General purpose digital input/output pin.
		I/O	**USB_D+1 —** USB1 port bidirectional D+ line. (LPC2378 only)
P0[30]/USB_D−1	43[5]	I/O	**P0[30] —** General purpose digital input/output pin.
		I/O	**USB_D−1 —** USB1 port bidirectional D− line. (LPC2378 only)
P0[31]/USB_D+2	36[5]	I/O	**P0[31] —** General purpose digital input/output pin.
		I/O	**USB_D+2 —** USB2 port bidirectional D+ line. (LPC2378 only)
P1[0] to P1[31]		I/O	**Port 1:** Port 1 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 2, 3, 5, 6, 7, 11, 12, and 13 of this port are not available.
P1[0]/ ENET_TXD0	136[1]	I/O	**P1[0] —** General purpose digital input/output pin.
		O	**ENET_TXD0 —** Ethernet transmit data 0.
P1[1]/ ENET_TXD1	135[1]	I/O	**P1[1] —** General purpose digital input/output pin.
		O	**ENET_TXD1 —** Ethernet transmit data 1.
P1[4]/ ENET_TX_EN	133[1]	I/O	**P1[4] —** General purpose digital input/output pin.
		O	**ENET_TX_EN —** Ethernet transmit data enable.
P1[8]/ ENET_CRS	132[1]	I/O	**P1[8] —** General purpose digital input/output pin.
		I	**ENET_CRS —** Ethernet carrier sense.
P1[9]/ ENET_RXD0	131[1]	I/O	**P1[9] —** General purpose digital input/output pin.
		I	**ENET_RXD0 —** Ethernet receive data.
P1[10]/ ENET_RXD1	129[1]	I/O	**P1[10] —** General purpose digital input/output pin.
		I	**ENET_RXD1 —** Ethernet receive data.
P1[14]/ ENET_RX_ER	128[1]	I/O	**P1[14] —** General purpose digital input/output pin.
		I	**ENET_RX_ER —** Ethernet receive error.
P1[15]/ ENET_REF_CLK	126[1]	I/O	**P1[15] —** General purpose digital input/output pin.
		I	**ENET_REF_CLK/ENET_RX_CLK —** Ethernet receiver clock.
P1[16]/ ENET_MDC	125[1]	I/O	**P1[16] —** General purpose digital input/output pin.
		O	**ENET_MDC —** Ethernet MIIM clock.
P1[17]/ ENET_MDIO	123[1]	I/O	**P1[17] —** General purpose digital input/output pin.
		I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
P1[18]/ USB_UP_LED1/ PWM1[1]/ CAP1[0]	46[1]	I/O	**P1[18] —** General purpose digital input/output pin.
		O	**USB_UP_LED1 —** USB1 port Good Link LED indicator. It is LOW when device is configured (non-control endpoints enabled), or when host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when host is enabled and detects activity on the bus. (LPC2378 only)
		O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
		I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P1[19]/CAP1[1]	47[1]	I/O	**P1[19] —** General purpose digital input/output pin.
		I	**CAP1[1] —** Capture input for Timer 1, channel 1.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P2[1]/PWM1[2]/ RXD1/ PIPESTAT0	106[1]	I/O	**P2[1] —** General purpose digital input/output pin.
		O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
		I	**RXD1 —** Receiver input for UART1.
		O	**PIPESTAT0 —** Pipeline Status, bit 0.
P2[2]/PWM1[3]/ CTS1/ PIPESTAT1	105[1]	I/O	**P2[2] —** General purpose digital input/output pin.
		O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
		I	**CTS1 —** Clear to Send input for UART1.
		O	**PIPESTAT1 —** Pipeline Status, bit 1.
P2[3]/PWM1[4]/ DCD1/ PIPESTAT2	100[1]	I/O	**P2[3] —** General purpose digital input/output pin.
		O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
		I	**DCD1 —** Data Carrier Detect input for UART1.
		O	**PIPESTAT2 —** Pipeline Status, bit 2.
P2[4]/PWM1[5]/ DSR1/ TRACESYNC	99[1]	I/O	**P2[4] —** General purpose digital input/output pin.
		O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
		I	**DSR1 —** Data Set Ready input for UART1.
		O	**TRACESYNC —** Trace Synchronization.
P2[5]/PWM1[6]/ DTR1/ TRACEPKT0	97[1]	I/O	**P2[5] —** General purpose digital input/output pin.
		O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
		O	**DTR1 —** Data Terminal Ready output for UART1.
		O	**TRACEPKT0 —** Trace Packet, bit 0.
P2[6]/PCAP1[0]/ RI1/ TRACEPKT1	96[1]	I/O	**P2[6] —** General purpose digital input/output pin.
		I	**PCAP1[0] —** Capture input for PWM1, channel 0.
		I	**RI1 —** Ring Indicator input for UART1.
		O	**TRACEPKT1 —** Trace Packet, bit 1.
P2[7]/RD2/ RTS1/ TRACEPKT2	95[1]	I/O	**P2[7] —** General purpose digital input/output pin.
		I	**RD2 —** CAN2 receiver input. (LPC2378 only)
		O	**RTS1 —** Request to Send output for UART1.
		O	**TRACEPKT2 —** Trace Packet, bit 2.
P2[8]/TD2/ TXD2/ TRACEPKT3	93[1]	I/O	**P2[8] —** General purpose digital input/output pin.
		O	**TD2 —** CAN2 transmitter output. (LPC2378 only)
		O	**TXD2 —** Transmitter output for UART2.
		O	**TRACEPKT3 —** Trace Packet, bit 3.
P2[9]/ USB_CONNECT1/ RXD2/ EXTIN0	92[1]	I/O	**P2[9] —** General purpose digital input/output pin.
		O	**USB_CONNECT1 —** USB1 Soft Connect control. Signal used to switch an external 1.5 kΩ resistor under the software control. Used with the SoftConnect USB feature. (LPC2378 only)
		I	**RXD2 —** Receiver input for UART2.
		I	**EXTIN0 —** External Trigger Input.
P2[10]/$\overline{\text{EINT0}}$	76[6]	I/O	**P2[10] —** General purpose digital input/output pin. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after a reset.
		I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.

The 16-bit instruction length of the Thumb set allows it to approach twice the density of standard ARM code, while retaining most of the ARM performance advantage over a traditional 16-bit processor using 16-bit registers. This increase is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

7.2 On-chip flash programming memory

The LPC2377/78 incorporate a 512 kB flash memory system. This memory can be used for both code and data storage. Programming of the flash memory can be accomplished in several ways. It may be programmed In System via the serial port (UART0). The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field and firmware upgrades.

The flash memory is 128 bits wide and includes pre-fetching and buffering techniques to allow it to operate at SRAM speeds of 72 MHz.

7.3 On-chip SRAM

The LPC2377/78 include a SRAM memory of 32 kB reserved for the ARM processor exclusive use. This RAM may be used for code and/or data storage and may be accessed as 8 bits, 16 bits, and 32 bits.

A 16 kB SRAM block serving as a buffer for the Ethernet controller and an 8 kB SRAM used by the GPDMA controller or the USB device can be used for data and code storage. The 2 kB RTC SRAM can be used for data storage only. The RTC SRAM is battery powered and retains the content in the absence of the main power supply.

7.5 Interrupt controller

The ARM processor core has two interrupt inputs called Interrupt Request (IRQ) and Fast Interrupt Request (FIQ). The VIC takes 32 interrupt request inputs which can be programmed as FIQ or vectored IRQ types. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQs have the highest priority. If more than one request is assigned to FIQ, the VIC ORs the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs, which include all interrupt requests that are not classified as FIQs, have a programmable interrupt priority. When more than one interrupt is assigned the same priority and occur simultaneously, the one connected to the lowest numbered VIC channel will be serviced first.

The VIC ORs the requests from all of the vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping to the address supplied by that register.

7.5.1 Interrupt sources

Each peripheral device has one interrupt line connected to the VIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on Port 0 and Port 2 (total of 46 pins) regardless of the selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both. Such interrupt requests coming from Port 0 and/or Port 2 will be combined with the $\overline{\text{EINT3}}$ interrupt requests.

7.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 External memory controller

The LPC2377/78 EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

7.10 Ethernet

The Ethernet block contain a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share a dedicated AHB subsystem that is used to access the Ethernet SRAM for Ethernet data, control, and status information. All other AHB traffic in the LPC2377/78 takes place on a different AHB subsystem, effectively separating Ethernet activity from the rest of the system. The Ethernet DMA can also access off-chip memory via the EMC, as well as the SRAM located on another AHB, if it is not being used by the USB block. However, using memory other than the Ethernet SRAM, especially off-chip memory, will slow Ethernet access to memory and increase the loading of its AHB.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.10.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x full duplex flow control and half duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching.
  - Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.

- Physical interface:
  - Attachment of external PHY chip through standard RMII interface.
  - PHY register access is available via the MIIM interface.

7.11 USB interface (LPC2378 only)

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and a number (127 maximum) of peripherals. The host controller allocates the USB bandwidth to attached devices through a token based protocol. The bus supports hot plugging, unplugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The two sets of pins needed by a USB device are named V_{BUS}, USB_D+1, USB_D−1, USB_UP_LED1, USB_CONNECT1, and USB_D+2, USB_D−2, USB_UP_LED2, and USB_CONNECT2 respectively. At any given time only one of these two sets can be active and used by the application.

7.11.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of register interface, serial interface engine, endpoint buffer memory, and the DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. The DMA controller when enabled transfers data between the endpoint buffer and the USB RAM.

7.11.1.1 Features

- Fully compliant with *USB 2.0 specification* (full speed).
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the LPC2377/78 can enter one of the reduced power modes and wake up on a USB activity.
- Supports DMA transfers with the DMA RAM of 8 kB on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

7.14 10-bit DAC

The DAC allows the LPC2377/78 to generate a variable analog output. The maximum output value of the DAC is $V_{i(VREF)}$.

7.14.1 Features

- 10-bit DAC
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable output drive

7.15 UARTs

The LPC2377/78 contain four UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 can be achieved with any crystal frequency above 2 MHz.

7.15.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- UART3 includes an IrDA mode to support infrared communication.

7.16 SPI serial I/O controller

The LPC2377/78 contain one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

7.16.1 Features

- Compliant with SPI specification
- Synchronous, Serial, Full Duplex Communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

7.24 RTC and battery RAM

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power in Power-down and Deep power-down modes. On the LPC2377/78, the RTC can be clocked by a separate 32.768 kHz oscillator or by a programmable prescale divider based on the APB clock. Also, the RTC is powered by its own power supply pin, VBAT, which can be connected to a battery or to the same 3.3 V supply used by the rest of the device.

The VBAT pin supplies power only to the RTC and the battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery. When the CPU and the rest of chip functions are stopped and power removed, the RTC can supply an alarm output that can be used by external hardware to restore chip power and resume operation.

7.24.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated 32 kHz oscillator or programmable prescaler from APB clock.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- An alarm output pin is included to assist in waking up from Power-down mode, or when the chip has had power removed to all functions except the RTC and battery RAM.
- Periodic interrupts can be generated from increments of any field of the time registers, and selected fractional second values.
- 2 kB data SRAM powered by VBAT.
- RTC and battery RAM power supply is isolated from the rest of the chip.

7.25 Clocking and power control

7.25.1 Crystal oscillators

The LPC2377/78 include three independent oscillators. These are the Main Oscillator, the Internal RC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the PLL and ultimately the CPU.

Following reset, the LPC2377/78 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

7.25.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to $\pm$ 1 % accuracy.

Upon power-up or any chip reset, the LPC2377/78 use the IRC as the clock source. Software may later switch to one of the other available clock sources.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P2[10] pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.26.4 AHB

The LPC2377/78 implement two AHBs in order to allow the Ethernet block to operate without interference caused by other system activity. The primary AHB, referred to as AHB1, includes the Vectored Interrupt Controller, GPDMA controller, USB interface, and 8 kB SRAM primarily intended for use by the USB.

The second AHB, referred to as AHB2, includes only the Ethernet block and an associated 16 kB SRAM. In addition, a bus bridge is provided that allows the secondary AHB to be a bus master on AHB1, allowing expansion of Ethernet buffer space into off-chip memory or unused space in memory residing on AHB1.

In summary, bus masters with access to AHB1 are the ARM7 itself, the USB block, the GPDMA function, and the Ethernet block (via the bus bridge from AHB2). Bus masters with access to AHB2 are the ARM7 and the Ethernet block.

7.26.5 External interrupt inputs

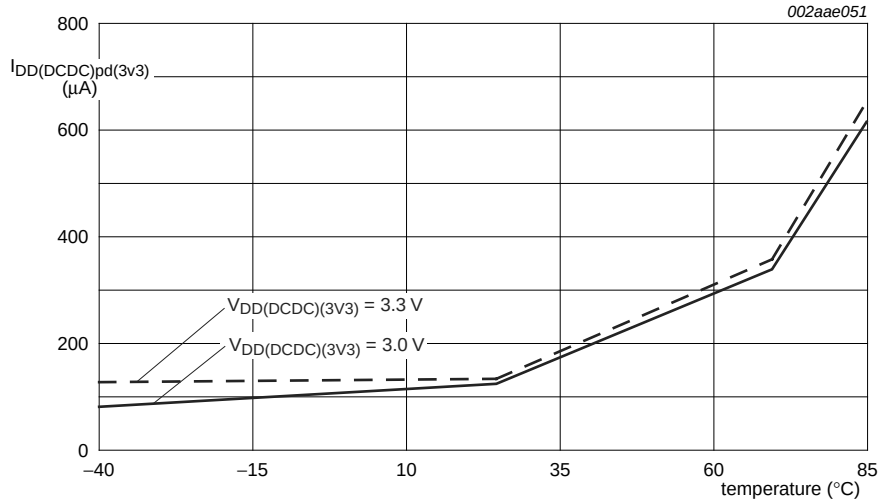
The LPC2377/78 include up to 50 edge sensitive interrupt inputs combined with up to four level sensitive external interrupt inputs as selectable pin functions. The external interrupt inputs can optionally be used to wake up the processor from Power-down mode.

7.26.6 Memory mapping control

The memory mapping control alters the mapping of the interrupt vectors that appear at the beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the Boot ROM, the SRAM, or external memory. This allows code running in different memory spaces to have control of the interrupts.

7.27 Emulation and debugging

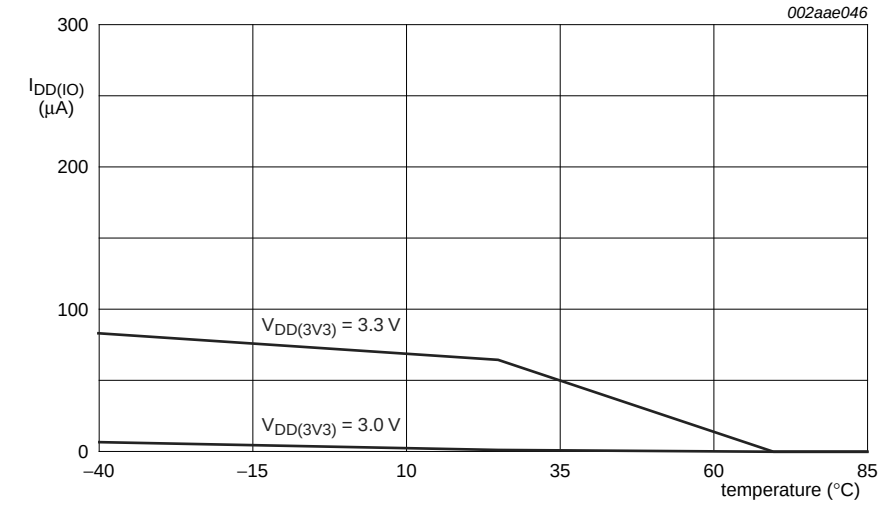
The LPC2377/78 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on P2[0] to P2[9]. This means that all communication, timer, and interface peripherals residing on other pins are available during the development and debugging phase as they are when the application is run in the embedded system itself.



$V_{DD(3V3)} = V_{i(VBAT)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 6. Total DC-to-DC converter supply current $I_{DD(DCDC)pd(3V3)}$ at different temperatures in Power-down mode

10.2 Deep power-down mode



$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 7. I/O maximum supply current $I_{DD(IO)}$ versus temperature in Deep power-down mode

11. Dynamic characteristics

Table 8. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock (see Figure 12)						
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
I^2C-bus pins (P0[27] and P0[28])						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns
SSP interface						
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 16	-	11	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

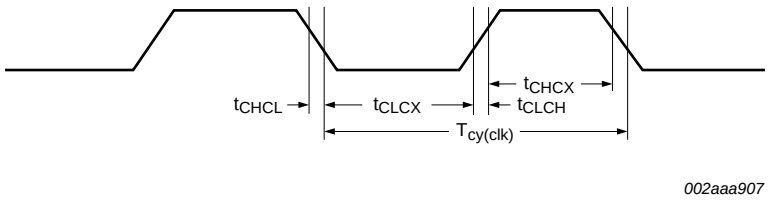


Fig 12. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.5 Static external memory interface

Table 13. Dynamic characteristics: Static external memory interface
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(DCDC)(3V3)}$ = $V_{DD(3V3)}$ = 3.0 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to read and write cycles[1]						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time		−0.29	0.20	2.54	ns
Read cycle parameters[1][2]						
t_{OELAV}	$\overline{OE}$ LOW to address valid time		−0.29	0.20	2.54	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		−0.78 + $T_{cy(CCLK)}$ × WAITOEN	0 + $T_{cy(CCLK)}$ × WAITOEN	0.49 + $T_{cy(CCLK)}$ × WAITOEN	ns
t_{am}	memory access time	[3][4]	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 12.70	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 9.57	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 8.11	ns
$t_{h(D)}$	data input hold time	[5]	0	-	-	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		−0.49	0	0.20	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		−0.20	0.20	2.44	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		−0.59 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	0 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	0.10 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	
Write cycle parameters[1]						
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time		−0.88 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	0.10 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	0.20 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	ns
t_{BLSLDV}	$\overline{BLS}$ LOW to data valid time		0.68	2.54	5.86	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		0	2.64	4.79	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[3]	−0.78 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	0 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	0.10 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time	[3]	0 + $T_{cy(CCLK)}$	0.20 + $T_{cy(CCLK)}$	2.74 + $T_{cy(CCLK)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	[3]	0.78	2.54	5.96	ns

[1] V_{OH} = 2.5 V, V_{OL} = 0.2 V.

[2] V_{IH} = 2.5 V, V_{IL} = 0.5 V.

[3] $T_{cy(CCLK)} = {}^{1}/_{CCLK}$.

[4] Latest of address valid, $\overline{CS}$ LOW, $\overline{OE}$ LOW to data valid.

[5] Earliest of $\overline{CS}$ HIGH, $\overline{OE}$ HIGH, address change to data invalid.

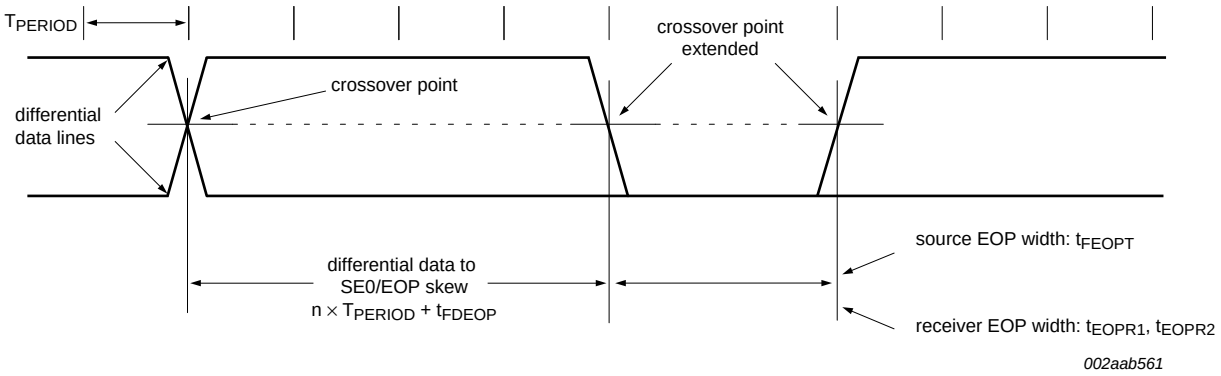


Fig 15. Differential data-to-EOP transition skew and EOP width

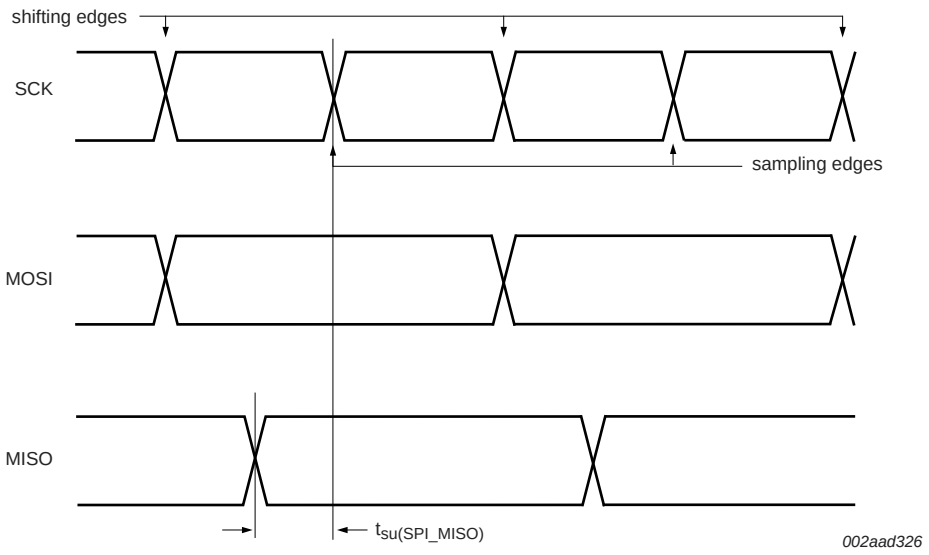


Fig 16. MISO line set-up time in SSP Master mode

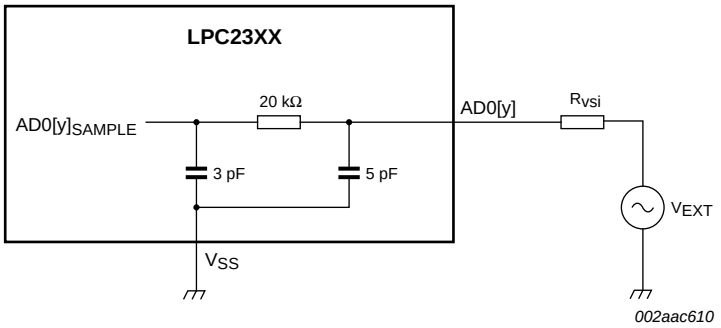


Fig 18. Suggested ADC interface - LPC2377/78 AD0[y] pin

14.6 Reset pin configuration

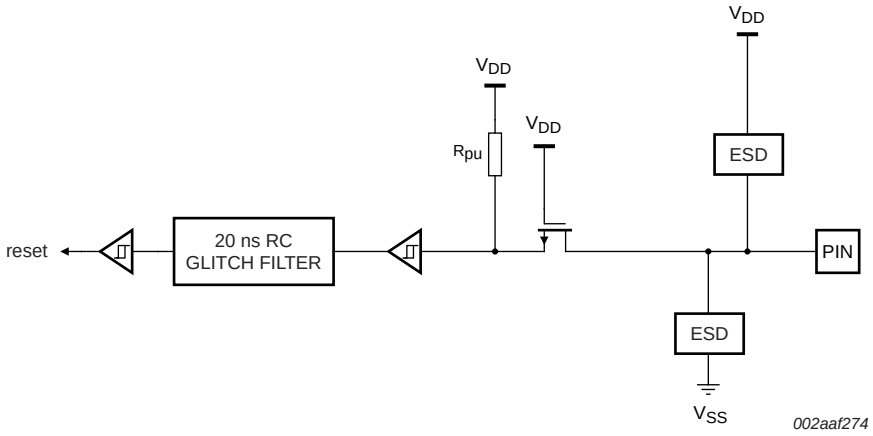


Fig 25. Reset pin configuration

Table 20. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2377_78 v.5	20100617	Product data sheet	-	LPC2377_78 v.4
Modifications:	• Table 3 “Pin description”: Added Table note 9 for XTAL1 and XTAL2 pins. • Table 3 “Pin description”: Added Table note 10 for RTCX1 and RTCX2 pins. • Table 4 “Limiting values”: Changed V_{ESD} min/max to −2500/+2500. • Table 7 “Static characteristics”: Removed R_{pu}. • Table 7 “Static characteristics”, Table note 13: Changed value from 18 to 33. • Table 7 “Static characteristics”: Updated min, typical and max values for oscillator pins. • Table 7 “Static characteristics”: Updated conditions and typical values for $I_{DD(DCDC)pd(3V3)}$, I_{BATact}; added $I_{DD(DCDC)dpd(3V3)}$ and I_{BAT}. • Added Table 12 “Dynamic characteristics of flash”. • Table 13 “Dynamic characteristics: Static external memory interface”: Updated table. • Added Table 15 “DAC electrical characteristics”. • Section 7.2 “On-chip flash programming memory”: Removed text regarding flash endurance minimum specs. • Added Section 7.25.4.4 “Deep power-down mode”. • Section 7.26.2 “Brownout detection”: Changed $V_{DD(3V3)}$ to $V_{DD(DCDC)(3V3)}$. • Added Section 9 “Thermal characteristics”. • Added Section 10.1 “Power-down mode”. • Added Section 10.2 “Deep power-down mode” • Added Section 10.3 “Electrical pin characteristics” • Added Section 14.2 “Crystal oscillator XTAL input and component selection”. • Added Section 14.3 “RTC 32 kHz oscillator component selection”. • Added Section 14.4 “XTAL and RTCX Printed Circuit Board (PCB) layout guidelines”. • Added Section 14.5 “Standard I/O pin configuration” • Added Section 14.6 “Reset pin configuration” • Moved Figure 12 “External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)” to below Table 8 “Dynamic characteristics”. • Updated Figure 13 “External memory read access”. • Updated Figure 14 “External memory write access”. • Updated Figure 17 “ADC characteristics”.			
LPC2377_78 v.4	20081119	Product data sheet	-	LPC2378 v.3
LPC2378 v.3	20070927	Preliminary data sheet	-	LPC2378 v.2
Modifications:	• Font in graphics updated.			
LPC2378 v.2	20070501	Preliminary data sheet	-	LPC2378 v.1
Modifications:	• Removed references to $V_{DD(1V8)}$. • Removed Deep power-down mode chapter and related references.			
LPC2378 v.1	20061206	Preliminary data sheet	-	-