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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	104
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	58K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2378fbd144-551

- General Purpose DMA controller (GPDMA) on AHB that can be used with the SSP serial interfaces, the I^2S port, and the Secure Digital/MultiMediaCard (SD/MMC) card port, as well as for memory-to-memory transfers.
- Serial Interfaces:
  - Ethernet MAC with associated DMA controller. These functions reside on an independent AHB.
  - USB 2.0 full-speed device with on-chip PHY and associated DMA controller (LPC2378 only).
  - Four UARTs with fractional baud rate generation, one with modem control I/O, one with IrDA support, all with FIFO.
  - CAN controller with two channels (LPC2378 only).
  - SPI controller.
  - Two SSP controllers with FIFO and multi-protocol capabilities. One is an alternate for the SPI port, sharing its interrupt and pins. These controllers can be used with the GPDMA controller.
  - Three I^2C-bus interfaces (one with open-drain and two with standard port pins).
  - I^2S (Inter-IC Sound) interface for digital audio input or output. It can be used with the GPDMA.
- Other peripherals:
  - SD/MMC memory card interface.
  - 104 General purpose I/O pins with configurable pull-up/down resistors.
  - 10-bit ADC with input multiplexing among 8 pins.
  - 10-bit DAC.
  - Four general purpose timers/counters with 8 capture inputs and 10 compare outputs. Each timer block has an external count input.
  - One PWM/timer block with support for three-phase motor control. The PWM has two external count inputs.
  - Real-Time Clock (RTC) with separate power pin, clock source can be the RTC oscillator or the APB clock.
  - 2 kB SRAM powered from the RTC power pin, allowing data to be stored when the rest of the chip is powered off.
  - WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation trace module supports real-time trace.
- Single 3.3 V power supply (3.0 V to 3.6 V).
- Four reduced power modes: idle, sleep, power-down, and deep power-down.
- Four external interrupt inputs configurable as edge/level sensitive. All pins on Port 0 and Port 2 can be used as edge sensitive interrupt sources.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt).
- Two independent power domains allow fine-tuning of power consumption based on needed features.
- Each peripheral has its own clock divider for further power saving.
- Brownout detect with separate thresholds for interrupt and forced reset.
- On-chip power-on reset.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0[9]/ I2STX_SDA/ MOSI1/MAT2[3]	109[1]	I/O	**P0[9] —** General purpose digital input/output pin.
		I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
		I/O	**MOSI1 —** Master Out Slave In for SSP1.
		O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	69[1]	I/O	**P0[10] —** General purpose digital input/output pin.
		O	**TXD2 —** Transmitter output for UART2.
		I/O	**SDA2 —** I^2C2 data input/output (this pin is not open-drain).
		O	**MAT3[0] —** Match output for Timer 3, channel 0.
P0[11]/RXD2/ SCL2/MAT3[1]	70[1]	I/O	**P0[11] —** General purpose digital input/output pin.
		I	**RXD2 —** Receiver input for UART2.
		I/O	**SCL2 —** I^2C2 clock input/output (this pin is not open-drain).
		O	**MAT3[1] —** Match output for Timer 3, channel 1.
P0[12]/MISO1/ AD0[6]	29[2]	I/O	**P0[12] —** General purpose digital input/output pin.
		I/O	**MISO1 —** Master In Slave Out for SSP1.
		I	**AD0[6] —** A/D converter 0, input 6.
P0[13]/ USB_UP_LED2/ MOSI1/AD0[7]	32[2]	I/O	**P0[13] —** General purpose digital input/output pin.
		O	**USB_UP_LED2 —** USB2 Good Link LED indicator. It is LOW when device is configured (non-control endpoints enabled), or when host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when host is enabled and detects activity on the bus. (LPC2378 only)
		I/O	**MOSI1 —** Master Out Slave In for SSP1.
		I	**AD0[7] —** A/D converter 0, input 7.
P0[14]/ USB_CONNECT2/ SSEL1	48[1]	I/O	**P0[14] —** General purpose digital input/output pin.
		O	**USB_CONNECT2 —** USB2 Soft Connect control. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature. (LPC2378 only)
		I/O	**SSEL1 —** Slave Select for SSP1.
P0[15]/TXD1/ SCK0/SCK	89[1]	I/O	**P0[15] —** General purpose digital input/output pin.
		O	**TXD1 —** Transmitter output for UART1.
		I/O	**SCK0 —** Serial clock for SSP0.
		I/O	**SCK —** Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	90[1]	I/O	**P0[16] —** General purpose digital input/output pin.
		I	**RXD1 —** Receiver input for UART1.
		I/O	**SSEL0 —** Slave Select for SSP0.
		I/O	**SSEL —** Slave Select for SPI.
P0[17]/CTS1/ MISO0/MISO	87[1]	I/O	**P0[17] —** General purpose digital input/output pin.
		I	**CTS1 —** Clear to Send input for UART1.
		I/O	**MISO0 —** Master In Slave Out for SSP0.
		I/O	**MISO —** Master In Slave Out for SPI.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P3[25]/MAT0[0]/ PWM1[2]	39[1]	I/O	**P3[25] —** General purpose digital input/output pin.
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
		O	**PWM1[2] —** Pulse Width Modulator 1, output 2.
P3[26]/MAT0[1]/ PWM1[3]	38[1]	I/O	**P3[26] —** General purpose digital input/output pin.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
		O	**PWM1[3] —** Pulse Width Modulator 1, output 3.
P4[0] to P4[31]		I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the pin connect block. Pins 16 through 23, 26, and 27 of this port are not available.
P4[0]/A0	52[1]	I/O	**P4[0] —**]General purpose digital input/output pin.
		I/O	**A0 —** External memory address line 0.
P4[1]/A1	55[1]	I/O	**P4[1] —** General purpose digital input/output pin.
		I/O	**A1 —** External memory address line 1.
P4[2]/A2	58[1]	I/O	**P4[2] —** General purpose digital input/output pin.
		I/O	**A2 —** External memory address line 2.
P4[3]/A3	68[1]	I/O	**P4[3] —** General purpose digital input/output pin.
		I/O	**A3 —** External memory address line 3.
P4[4]/A4	72[1]	I/O	**P4[4] —** General purpose digital input/output pin.
		I/O	**A4 —** External memory address line 4.
P4[5]/A5	74[1]	I/O	**P4[5] —** General purpose digital input/output pin.
		I/O	**A5 —** External memory address line 5.
P4[6]/A6	78[1]	I/O	**P4[6] —** General purpose digital input/output pin.
		I/O	**A6 —** External memory address line 6.
P4[7]/A7	84[1]	I/O	**P4[7] —** General purpose digital input/output pin.
		I/O	**A7 —** External memory address line 7.
P4[8]/A8	88[1]	I/O	**P4[8] —** General purpose digital input/output pin.
		I/O	**A8 —** External memory address line 8.
P4[9]/A9	91[1]	I/O	**P4[9] —** General purpose digital input/output pin.
		I/O	**A9 —** External memory address line 9.
P4[10]/A10	94[1]	I/O	**P4[10] —** General purpose digital input/output pin.
		I/O	**A10 —** External memory address line 10.
P4[11]/A11	101[1]	I/O	**P4[11] —** General purpose digital input/output pin.
		I/O	**A11 —** External memory address line 11.
P4[12]/A12	104[1]	I/O	**P4[12] —** General purpose digital input/output pin.
		I/O	**A12 —** External memory address line 12.
P4[13]/A13	108[1]	I/O	**P4[13] —** General purpose digital input/output pin.
		I/O	**A13 —** External memory address line 13.
P4[14]/A14	110[1]	I/O	**P4[14] —** General purpose digital input/output pin.
		I/O	**A14 —** External memory address line 14.
P4[15]/A15	120[1]	I/O	**P4[15] —** General purpose digital input/output pin.
		I/O	**A15 —** External memory address line 15.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
$V_{DD(3V3)}$	41, 62, 77, 102, 114, 138[15]	I	**3.3 V supply voltage:** These pins provide power supply voltage for the I/O ports.
n.c.	21, 81, 98[16]	I	Leave these pins unconnected.
$V_{DD(DCDC)(3V3)}$	18, 60, 121[17]	I	**3.3 V DC-to-DC converter supply voltage:** These pins provide the power supply voltage for the on-chip DC-to-DC converter only.
V_{DDA}	14[18]	I	**analog 3.3 V pad supply voltage:** This pin should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC.
VREF	17[18]	I	**ADC reference:** This pin should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. The level on this pin is used as a reference for ADC and DAC.
VBAT	27[18]	I	**RTC pin power supply:** 3.3 V on this pin supplies the power to the RTC peripheral.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis.

[2] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input. When configured as a DAC input, digital section of the pad is disabled.

[3] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[4] Open-drain, 5 V tolerant digital I/O pad compatible with I^2C-bus 400 kHz specification. It requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[5] Pad provides digital I/O and USB functions (LPC2378 only). It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only).

[6] 5 V tolerant pad with 10 ns glitch filter providing digital I/O functions with TTL levels and hysteresis.

[7] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[8] Pad provides special analog functionality.

[9] This pin has a built-in pull-up resistor.

[10] This pin has no built-in pull-up and no built-in pull-down resistor.

[11] When the main oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

[12] If the RTC is not used, these pins can be left floating.

[13] Pad provides special analog functionality.

[14] Pad provides special analog functionality.

[15] Pad provides special analog functionality.

[16] Pad provides special analog functionality.

[17] Pad provides special analog functionality.

[18] Pad provides special analog functionality.

The 16-bit instruction length of the Thumb set allows it to approach twice the density of standard ARM code, while retaining most of the ARM performance advantage over a traditional 16-bit processor using 16-bit registers. This increase is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

7.2 On-chip flash programming memory

The LPC2377/78 incorporate a 512 kB flash memory system. This memory can be used for both code and data storage. Programming of the flash memory can be accomplished in several ways. It may be programmed In System via the serial port (UART0). The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field and firmware upgrades.

The flash memory is 128 bits wide and includes pre-fetching and buffering techniques to allow it to operate at SRAM speeds of 72 MHz.

7.3 On-chip SRAM

The LPC2377/78 include a SRAM memory of 32 kB reserved for the ARM processor exclusive use. This RAM may be used for code and/or data storage and may be accessed as 8 bits, 16 bits, and 32 bits.

A 16 kB SRAM block serving as a buffer for the Ethernet controller and an 8 kB SRAM used by the GPDMA controller or the USB device can be used for data and code storage. The 2 kB RTC SRAM can be used for data storage only. The RTC SRAM is battery powered and retains the content in the absence of the main power supply.

7.5 Interrupt controller

The ARM processor core has two interrupt inputs called Interrupt Request (IRQ) and Fast Interrupt Request (FIQ). The VIC takes 32 interrupt request inputs which can be programmed as FIQ or vectored IRQ types. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQs have the highest priority. If more than one request is assigned to FIQ, the VIC ORs the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs, which include all interrupt requests that are not classified as FIQs, have a programmable interrupt priority. When more than one interrupt is assigned the same priority and occur simultaneously, the one connected to the lowest numbered VIC channel will be serviced first.

The VIC ORs the requests from all of the vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping to the address supplied by that register.

7.5.1 Interrupt sources

Each peripheral device has one interrupt line connected to the VIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on Port 0 and Port 2 (total of 46 pins) regardless of the selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both. Such interrupt requests coming from Port 0 and/or Port 2 will be combined with the $\overline{\text{EINT3}}$ interrupt requests.

7.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 External memory controller

The LPC2377/78 EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

7.12 CAN controller and acceptance filters (LPC2378 only)

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router among a number of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.12.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

7.13 10-bit ADC

The LPC2377/78 contain one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.13.1 Features

- 10-bit successive approximation ADC
- Input multiplexing among 8 pins
- Power-down mode
- Measurement range 0 V to $V_{i(VREF)}$
- 10-bit conversion time $\geq$ 2.44 μs
- Burst conversion mode for single or multiple inputs
- Optional conversion on transition of input pin or Timer Match signal
- Individual result registers for each ADC channel to reduce interrupt overhead

Three match registers can be used to provide a PWM output with both edges controlled. Again, the PWMMR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

7.22.1 Features

- The LPC2377/78 have one PWM block with Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

7.23 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

7.23.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the RTC clock, the Internal RC oscillator (IRC), or the APB peripheral clock. This gives a wide range of potential timing choices of watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring, for increased reliability.

7.25.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL. The clock selected as the PLL input is PLLCLKIN. The ARM processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The clock frequency for each peripheral can be selected individually and is referred to as PCLK. Refer to Section 7.25.2 for additional information.

7.25.1.3 RTC oscillator

The RTC oscillator can be used as the clock source for the RTC and/or the WDT. Also, the RTC oscillator can be used to drive the PLL and the CPU.

7.25.2 PLL

The PLL accepts an input clock frequency in the range of 32 kHz to 25 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and the USB block.

The PLL input, in the range of 32 kHz to 25 MHz, may initially be divided down by a value ‘N’, which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

Following the PLL input divider is the PLL multiplier. This can multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value ‘M’, in the range of 1 through 32768. The resulting frequency must be in the range of 275 MHz to 550 MHz. The multiplier works by dividing the CCO output by the value of M, then using a phase-frequency detector to compare the divided CCO output to the multiplier input. The error value is used to adjust the CCO frequency.

The PLL is turned off and bypassed following a chip Reset and by entering Power-down mode. PLL is enabled by software only. The program must configure and activate the PLL, wait for the PLL to lock, then connect to the PLL as a clock source.

7.25.3 Wake-up timer

The LPC2377/78 begin operation at power-up and when awakened from Power-down and Deep power-down modes by using the 4 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power-on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down and Deep power-down modes, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient

7.27.1 EmbeddedICE

The EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. The EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM7TDMI-S core present on the target system.

The ARM core has a Debug Communication Channel (DCC) function built-in. The DCC allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The DCC is accessed as a coprocessor 14 by the program running on the ARM7TDMI-S core. The DCC allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The DCC data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $1/6$ of the CPU clock (CCLK) for the JTAG interface to operate.

7.27.2 Embedded trace

Since the LPC2377/78 has significant amounts of on-chip memories, it is not possible to determine how the processor core is operating simply by observing the external pins. The ETM provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to a trace port. A software debugger allows configuration of the ETM using a JTAG interface and displays the trace information that has been captured.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external Trace Port Analyzer captures the trace information under software debugger control. The trace port can broadcast the Instruction trace information. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

7.27.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2377/78 contain a specific configuration of RealMonitor software programmed into the on-chip ROM memory.

10. Static characteristics

Table 7. Static characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	core and external rail		3.0	3.3	3.6	V
$V_{DD(DCDC)(3V3)}$	DC-to-DC converter supply voltage (3.3 V)			3.0	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			3.0	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[2]	2.0	3.3	3.6	V
$V_{i(VREF)}$	input voltage on pin VREF			2.5	3.3	V_{DDA}	V
$I_{DD(DCDC)act(3V3)}$	active mode DC-to-DC converter supply current (3.3 V)	$V_{DD(DCDC)(3V3)}$ = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from flash; no peripherals enabled; PCLK = CCLK					
		CCLK = 10 MHz		-	15	-	mA
		CCLK = 72 MHz		-	63	-	mA
		all peripherals enabled; PCLK = CCLK / 8					
		CCLK = 10 MHz		-	21	-	mA
		CCLK = 72 MHz		-	92	-	mA
		all peripherals enabled; PCLK = CCLK					
		CCLK = 10 MHz		-	27	-	mA
		CCLK = 72 MHz		-	125	-	mA
$I_{DD(DCDC)pd(3V3)}$	Power-down mode DC-to-DC converter supply current (3.3 V)	$V_{DD(DCDC)(3V3)}$ = 3.3 V; T_{amb} = 25 °C	[3]	-	113	-	μA
$I_{DD(DCDC)dpd(3V3)}$	Deep power-down mode DC-to-DC converter supply current (3.3 V)		[3]	-	20	-	μA
I_{BATact}	active mode battery supply current		[4]	-	20	-	μA
I_{BAT}	battery supply current	Deep power-down mode	[3]	-	20	-	μA
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	μA

Table 7. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_j < 125$ °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function	[5][6][7] [8]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[9]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[9]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[9]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[9]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[10]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[11]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	μA
		$V_{DD(3V3)} < V_I < 5$ V	[11]	0	0	0	μA
I^2C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[9]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[12]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	1.8	1.95	V

Table 7. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{o(RTCX2)}$	output voltage on pin RTCX2		−0.5	1.8	1.95	V
USB pins (LPC2378 only)						
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	-	-	±10	μA
V_{BUS}	bus supply voltage		-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V	-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive [13]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[3] $V_{DD(DCDC)(3V3)}$ = 3.3 V; $V_{DD(3V3)}$ = 3.3 V; $V_{i(VBAT)}$ = 3.3 V; T_{amb} = 25 °C.

[4] On pin VBAT.

[5] Including voltage on outputs in 3-state mode.

[6] $V_{DD(3V3)}$ supply voltages must be present.

[7] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[8] Please also see the errata note in errata sheet.

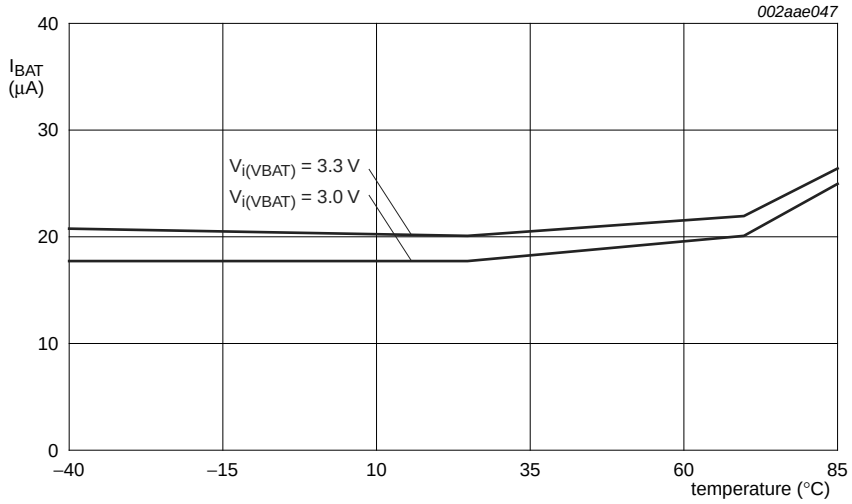
[9] Accounts for 100 mV voltage drop in all supply lines.

[10] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[11] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

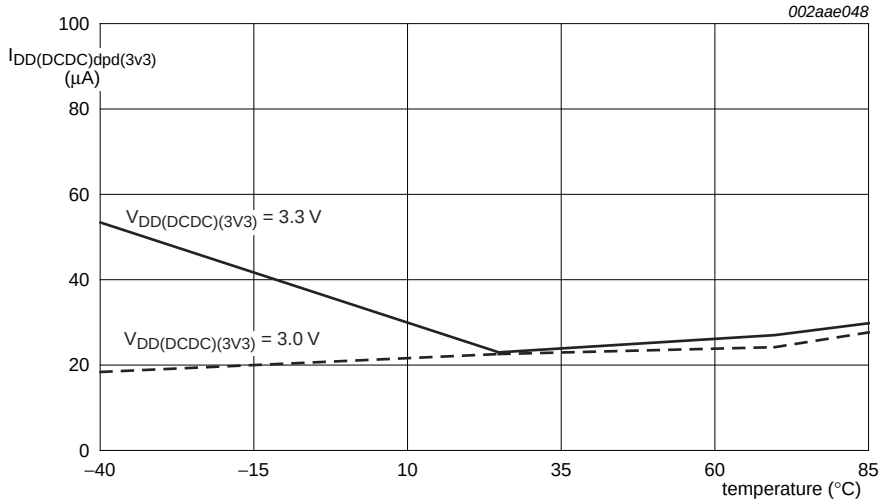
[12] To V_{SS}.

[13] Includes external resistors of 33 Ω ± 1 % on D+ and D−.



$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C

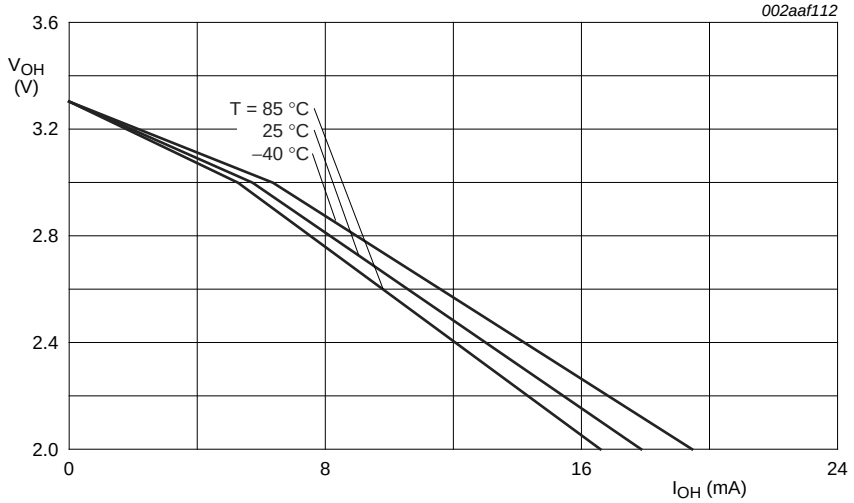
Fig 8. RTC battery maximum supply current I_{BAT} versus temperature in Deep power-down mode



$V_{DD(3V3)} = V_{i(VBAT)} = 3.3$ V; $T_{amb} = 25$ °C.

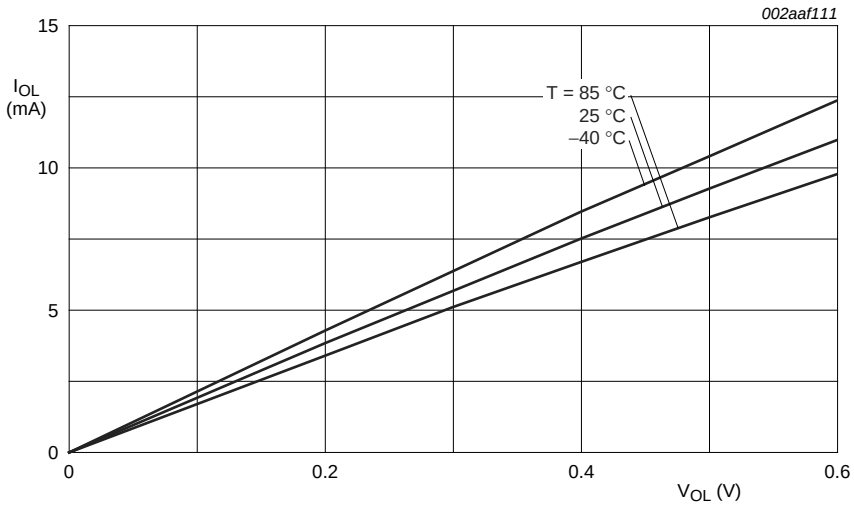
Fig 9. Total DC-to-DC converter maximum supply current $I_{DD(DCDC)dpd(3V3)}$ versus temperature in Deep power-down mode

10.3 Electrical pin characteristics



Conditions: $V_{DD(3V3)}$ = 3.3 V; standard port pins.

Fig 10. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: $V_{DD(3V3)}$ = 3.3 V; standard port pins.

Fig 11. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

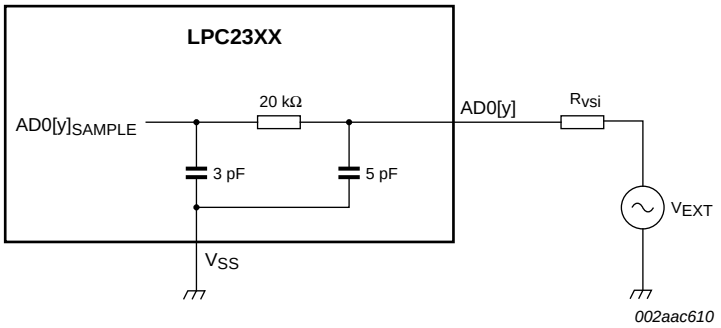


Fig 18. Suggested ADC interface - LPC2377/78 AD0[y] pin

13. DAC electrical characteristics

Table 15. DAC electrical characteristics

V_{DDA} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E_D	differential linearity error		-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		-	±1.5	-	LSB
E_O	offset error		-	0.6	-	%
E_G	gain error		-	0.6	-	%
C_L	load capacitance		-	200	-	pF
R_L	load resistance		1	-	-	kΩ

14. Application information

14.1 Suggested USB interface solutions (LPC2378 only)

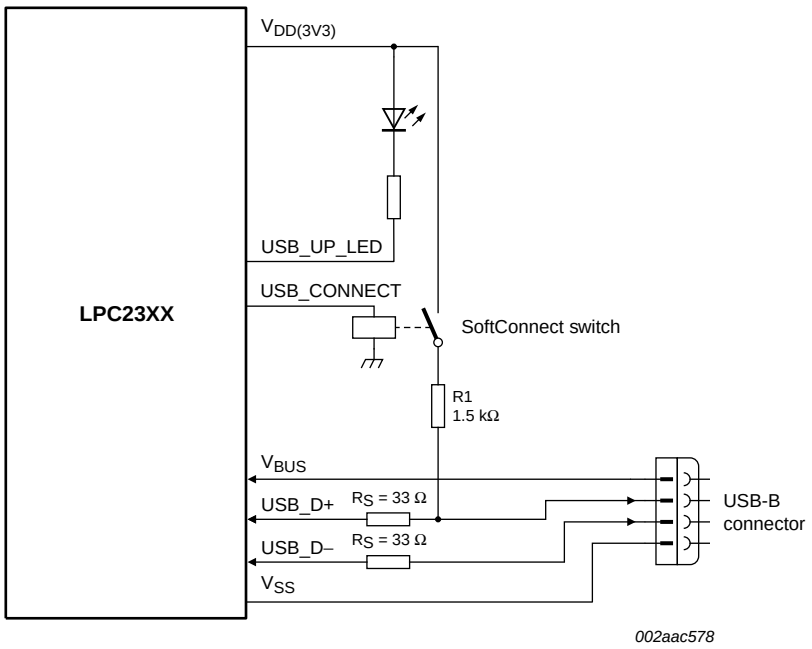


Fig 19. LPC2378 USB interface on a self-powered device

16. Abbreviations

Table 19. Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BLS	Byte Lane Select
BOD	BrownOut Detection
CAN	Controller Area Network
CTS	Clear To Send
DAC	Digital-to-Analog Converter
DCC	Debug Communication Channel
DMA	Direct Memory Access
DSP	Digital Signal Processing
EOP	End Of Packet
ETM	Embedded Trace Macrocell
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
MII	Media Independent Interface
MIIM	Media Independent Interface Management
PHY	Physical Layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
RTS	Request To Send
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

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Date of release: 16 October 2013
Document identifier: LPC2377_78