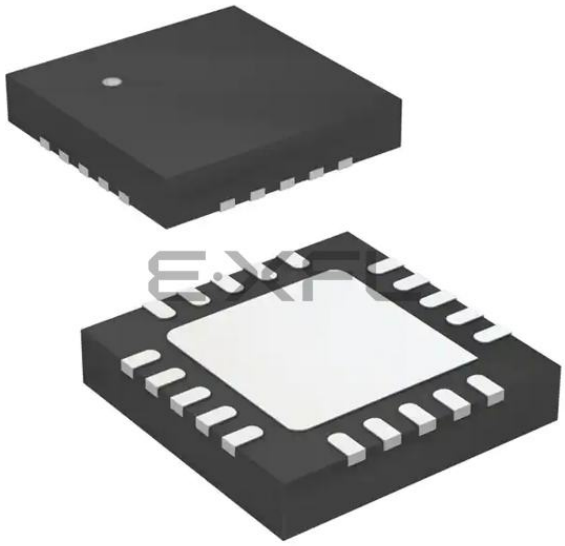


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

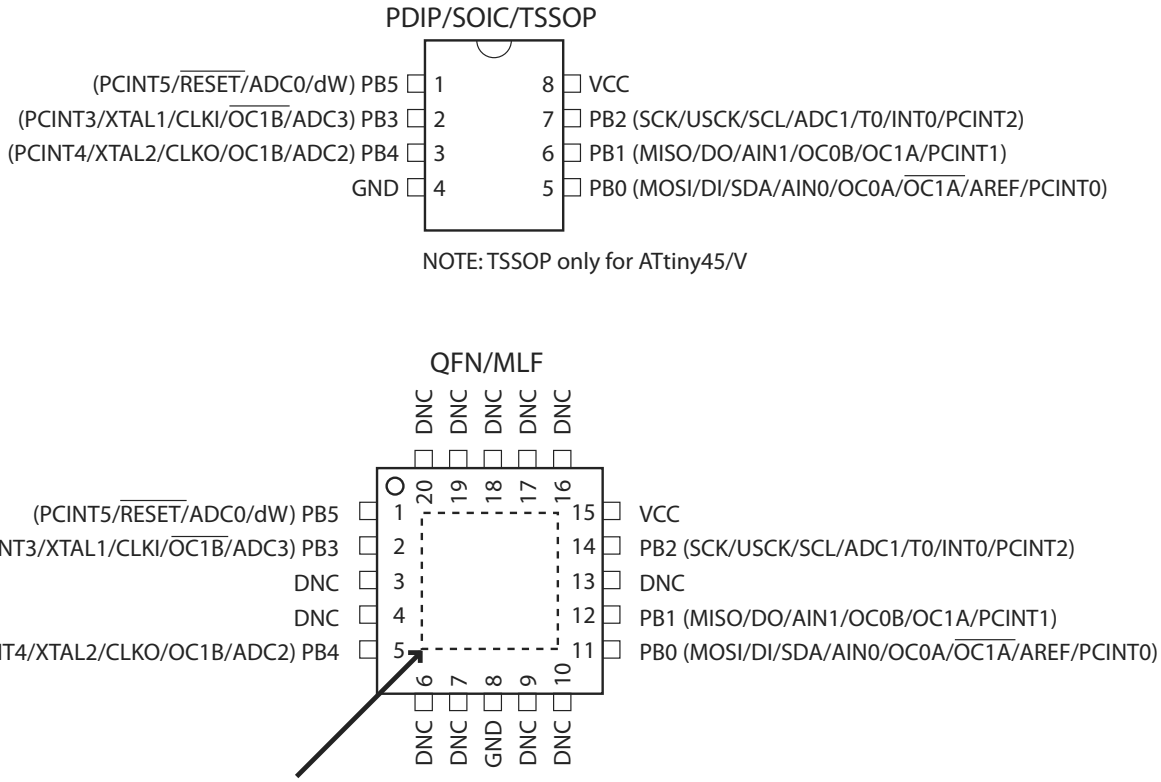
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | AVR |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | USI |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 6 |
| Program Memory Size | 4KB (2K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-WFQFN Exposed Pad |
| Supplier Device Package | 20-QFN-EP (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/attiny45-20mur |

# 1. Pin Configurations

**Figure 1-1.** Pinout ATtiny25/45/85




## 1.1 Pin Descriptions

### 1.1.1 VCC

Supply voltage.

### 1.1.2 GND

Ground.

### 1.1.3 Port B (PB5:PB0)

Port B is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny25/45/85 as listed in “Alternate Functions of Port B” on page 60.

On ATtiny25, the programmable I/O ports PB3 and PB4 (pins 2 and 3) are exchanged in ATtiny15 Compatibility Mode for supporting the backward compatibility with ATtiny15.

### 1.1.4 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in Table 21-4 on page 165. Shorter pulses are not guaranteed to generate a reset.

The reset pin can also be used as a (weak) I/O pin.

The ATtiny25/45/85 provides the following features: 2/4/8K bytes of In-System Programmable Flash, 128/256/512 bytes EEPROM, 128/256/256 bytes SRAM, 6 general purpose I/O lines, 32 general purpose working registers, one 8-bit Timer/Counter with compare modes, one 8-bit high speed Timer/Counter, Universal Serial Interface, Internal and External Interrupts, a 4-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. Power-down mode saves the register contents, disabling all chip functions until the next Interrupt or Hardware Reset. ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the Program memory to be re-programmed In-System through an SPI serial interface, by a conventional non-volatile memory programmer or by an On-chip boot code running on the AVR core.

The ATtiny25/45/85 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators and Evaluation kits.

should never be written.

2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

# 5. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| **ARITHMETIC AND LOGIC INSTRUCTIONS** | | | | | |
| ADD | Rd, Rr | Add two Registers | Rd ← Rd + Rr | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | Rd ← Rd + Rr + C | Z,C,N,V,H | 1 |
| ADIW | Rdl,K | Add Immediate to Word | Rdh:Rdl ← Rdh:Rdl + K | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | Rd ← Rd - Rr | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | Rd ← Rd - K | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | Rd ← Rd - Rr - C | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | Rd ← Rd - K - C | Z,C,N,V,H | 1 |
| SBIW | Rdl,K | Subtract Immediate from Word | Rdh:Rdl ← Rdh:Rdl - K | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | Rd ← Rd • Rr | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | Rd ← Rd • K | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | Rd ← Rd v Rr | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | Rd ← Rd v K | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | Rd ← Rd ⊕ Rr | Z,N,V | 1 |
| COM | Rd | One's Complement | Rd ← 0xFF – Rd | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | Rd ← 0x00 – Rd | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | Rd ← Rd v K | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | Rd ← Rd • (0xFF - K) | Z,N,V | 1 |
| INC | Rd | Increment | Rd ← Rd + 1 | Z,N,V | 1 |
| DEC | Rd | Decrement | Rd ← Rd – 1 | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | Rd ← Rd • Rd | Z,N,V | 1 |
| CLR | Rd | Clear Register | Rd ← Rd ⊕ Rd | Z,N,V | 1 |
| SER | Rd | Set Register | Rd ← 0xFF | None | 1 |
| **BRANCH INSTRUCTIONS** | | | | | |
| RJMP | k | Relative Jump | PC ← PC + k + 1 | None | 2 |
| IJMP | | Indirect Jump to (Z) | PC ← Z | None | 2 |
| RCALL | k | Relative Subroutine Call | PC ← PC + k + 1 | None | 3 |
| ICALL | | Indirect Call to (Z) | PC ← Z | None | 3 |
| RET | | Subroutine Return | PC ← STACK | None | 4 |
| RETI | | Interrupt Return | PC ← STACK | I | 4 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) PC ← PC + 2 or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | Rd – Rr | Z, N,V,C,H | 1 |
| CPC | Rd,Rr | Compare with Carry | Rd – Rr – C | Z, N,V,C,H | 1 |
| CPI | Rd,K | Compare Register with Immediate | Rd – K | Z, N,V,C,H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if (Rr(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if (P(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if (P(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then PC←PC+k + 1 | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then PC←PC+k + 1 | None | 1/2 |
| BREQ | k | Branch if Equal | if (Z = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLO | k | Branch if Lower | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRMI | k | Branch if Minus | if (N = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRPL | k | Branch if Plus | if (N = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N ⊕ V= 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if (N ⊕ V= 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if ( I = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if ( I = 0) then PC ← PC + k + 1 | None | 1/2 |
| **BIT AND BIT-TEST INSTRUCTIONS** | | | | | |
| SBI | P,b | Set Bit in I/O Register | I/O(P,b) ← 1 | None | 2 |
| CBI | P,b | Clear Bit in I/O Register | I/O(P,b) ← 0 | None | 2 |
| LSL | Rd | Logical Shift Left | Rd(n+1) ← Rd(n), Rd(0) ← 0 | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | Rd(n) ← Rd(n+1), Rd(7) ← 0 | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7) | Z,C,N,V | 1 |
| ROR | Rd | Rotate Right Through Carry | Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0) | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | Rd(n) ← Rd(n+1), n=0..6 | Z,C,N,V | 1 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| SWAP | Rd | Swap Nibbles | Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0) | None | 1 |
| BSET | s | Flag Set | SREG(s) ← 1 | SREG(s) | 1 |
| BCLR | s | Flag Clear | SREG(s) ← 0 | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | T ← Rr(b) | T | 1 |
| BLD | Rd, b | Bit load from T to Register | Rd(b) ← T | None | 1 |
| SEC | | Set Carry | C ← 1 | C | 1 |
| CLC | | Clear Carry | C ← 0 | C | 1 |
| SEN | | Set Negative Flag | N ← 1 | N | 1 |
| CLN | | Clear Negative Flag | N ← 0 | N | 1 |
| SEZ | | Set Zero Flag | Z ← 1 | Z | 1 |
| CLZ | | Clear Zero Flag | Z ← 0 | Z | 1 |
| SEI | | Global Interrupt Enable | I ← 1 | I | 1 |
| CLI | | Global Interrupt Disable | I ← 0 | I | 1 |
| SES | | Set Signed Test Flag | S ← 1 | S | 1 |
| CLS | | Clear Signed Test Flag | S ← 0 | S | 1 |
| SEV | | Set Twos Complement Overflow. | V ← 1 | V | 1 |
| CLV | | Clear Twos Complement Overflow | V ← 0 | V | 1 |
| SET | | Set T in SREG | T ← 1 | T | 1 |
| CLT | | Clear T in SREG | T ← 0 | T | 1 |
| SEH | | Set Half Carry Flag in SREG | H ← 1 | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | H ← 0 | H | 1 |
| **DATA TRANSFER INSTRUCTIONS** | | | | | |
| MOV | Rd, Rr | Move Between Registers | Rd ← Rr | None | 1 |
| MOVW | Rd, Rr | Copy Register Word | Rd+1:Rd ← Rr+1:Rr | None | 1 |
| LDI | Rd, K | Load Immediate | Rd ← K | None | 1 |
| LD | Rd, X | Load Indirect | Rd ← (X) | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Inc. | Rd ← (X), X ← X + 1 | None | 2 |
| LD | Rd, - X | Load Indirect and Pre-Dec. | X ← X - 1, Rd ← (X) | None | 2 |
| LD | Rd, Y | Load Indirect | Rd ← (Y) | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Inc. | Rd ← (Y), Y ← Y + 1 | None | 2 |
| LD | Rd, - Y | Load Indirect and Pre-Dec. | Y ← Y - 1, Rd ← (Y) | None | 2 |
| LDD | Rd,Y+q | Load Indirect with Displacement | Rd ← (Y + q) | None | 2 |
| LD | Rd, Z | Load Indirect | Rd ← (Z) | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Inc. | Rd ← (Z), Z ← Z+1 | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Dec. | Z ← Z - 1, Rd ← (Z) | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | Rd ← (Z + q) | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | Rd ← (k) | None | 2 |
| ST | X, Rr | Store Indirect | (X) ← Rr | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Inc. | (X) ← Rr, X ← X + 1 | None | 2 |
| ST | - X, Rr | Store Indirect and Pre-Dec. | X ← X - 1, (X) ← Rr | None | 2 |
| ST | Y, Rr | Store Indirect | (Y) ← Rr | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Inc. | (Y) ← Rr, Y ← Y + 1 | None | 2 |
| ST | - Y, Rr | Store Indirect and Pre-Dec. | Y ← Y - 1, (Y) ← Rr | None | 2 |
| STD | Y+q,Rr | Store Indirect with Displacement | (Y + q) ← Rr | None | 2 |
| ST | Z, Rr | Store Indirect | (Z) ← Rr | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Inc. | (Z) ← Rr, Z ← Z + 1 | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-Dec. | Z ← Z - 1, (Z) ← Rr | None | 2 |
| STD | Z+q,Rr | Store Indirect with Displacement | (Z + q) ← Rr | None | 2 |
| STS | k, Rr | Store Direct to SRAM | (k) ← Rr | None | 2 |
| LPM | | Load Program Memory | R0 ← (Z) | None | 3 |
| LPM | Rd, Z | Load Program Memory | Rd ← (Z) | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Inc | Rd ← (Z), Z ← Z+1 | None | 3 |
| SPM | | Store Program Memory | (z) ← R1:R0 | None | |
| IN | Rd, P | In Port | Rd ← P | None | 1 |
| OUT | P, Rr | Out Port | P ← Rr | None | 1 |
| PUSH | Rr | Push Register on Stack | STACK ← Rr | None | 2 |
| POP | Rd | Pop Register from Stack | Rd ← STACK | None | 2 |
| **MCU CONTROL INSTRUCTIONS** | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/Timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

## 6.2 ATtiny45

| Speed (MHz) [1] | Supply Voltage (V) | Temperature Range | Package [2] | Ordering Code [3] |
|---|---|---|---|---|
| 10 | 1.8 – 5.5 | Industrial (-40°C to +85°C) [4] | 8P3 | ATtiny45V-10PU |
| | | | 8S2 | ATtiny45V-10SU<br>ATtiny45V-10SUR<br>ATtiny45V-10SH<br>ATtiny45V-10SHR |
| | | | 8X | ATtiny45V-10XU<br>ATtiny45V-10XUR |
| | | | 20M1 | ATtiny45V-10MU<br>ATtiny45V-10MUR |
| 20 | 2.7 – 5.5 | Industrial (-40°C to +85°C) [4] | 8P3 | ATtiny45-20PU |
| | | | 8S2 | ATtiny45-20SU<br>ATtiny45-20SUR<br>ATtiny45-20SH<br>ATtiny45-20SHR |
| | | | 8X | ATtiny45-20XU<br>ATtiny45-20XUR |
| | | | 20M1 | ATtiny45-20MU<br>ATtiny45-20MUR |

Notes:
1. For speed vs. supply voltage, see section 21.3 “Speed” on page 163.
2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. Code indicators:
   - H: NiPdAu lead finish
   - U: matte tin
   - R: tape & reel
4. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

| Package Types | |
|---|---|
| 8P3 | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 8S2 | 8-lead, 0.208" Wide, Plastic Gull-Wing Small Outline (EIAJ SOIC) |
| 8X | 8-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline Package (TSSOP) |
| 20M1 | 20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF) |

## 6.3 ATtiny85

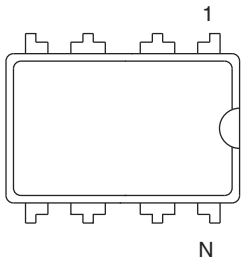
| Speed (MHz) [1] | Supply Voltage (V) | Temperature Range | Package [2] | Ordering Code [3] |
|---|---|---|---|---|
| 10 | 1.8 – 5.5 | Industrial (-40°C to +85°C) [4] | 8P3 | ATtiny85V-10PU |
| | | | 8S2 | ATtiny85V-10SU<br>ATtiny85V-10SUR<br>ATtiny85V-10SH<br>ATtiny85V-10SHR |
| | | | 20M1 | ATtiny85V-10MU<br>ATtiny85V-10MUR |
| 20 | 2.7 – 5.5 | Industrial (-40°C to +85°C) [4] | 8P3 | ATtiny85-20PU |
| | | | 8S2 | ATtiny85-20SU<br>ATtiny85-20SUR<br>ATtiny85-20SH<br>ATtiny85-20SHR |
| | | | 20M1 | ATtiny85-20MU<br>ATtiny85-20MUR |

Notes:
1. For speed vs. supply voltage, see section 21.3 “Speed” on page 163.
2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. Code indicators:
   – H: NiPdAu lead finish
   – U: matte tin
   – R: tape & reel
4. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

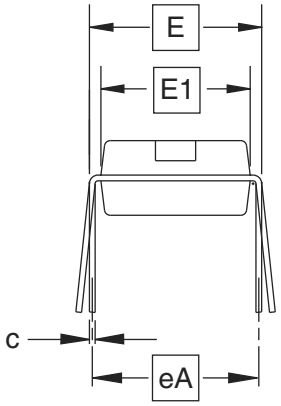
| Package Types | |
|---|---|
| 8P3 | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 8S2 | 8-lead, 0.208" Wide, Plastic Gull-Wing Small Outline (EIAJ SOIC) |
| 20M1 | 20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF) |

# 7. Packaging Information

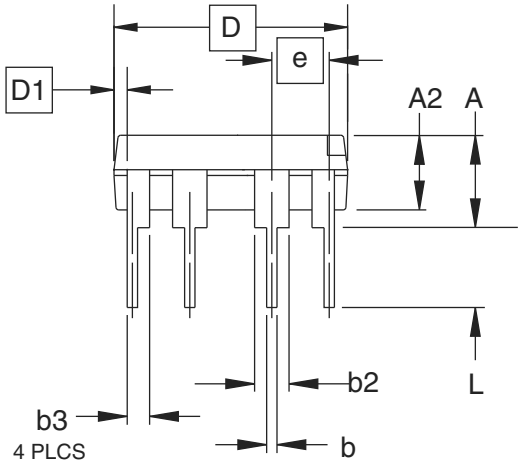
## 7.1 8P3




Top View




End View




Side View

**COMMON DIMENSIONS**
(Unit of Measure = inches)

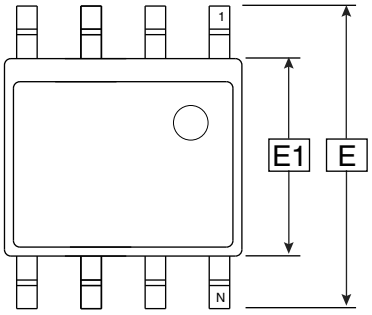
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | | | 0.210 | 2 |
| A2 | 0.115 | 0.130 | 0.195 | |
| b | 0.014 | 0.018 | 0.022 | 5 |
| b2 | 0.045 | 0.060 | 0.070 | 6 |
| b3 | 0.030 | 0.039 | 0.045 | 6 |
| c | 0.008 | 0.010 | 0.014 | |
| D | 0.355 | 0.365 | 0.400 | 3 |
| D1 | 0.005 | | | 3 |
| E | 0.300 | 0.310 | 0.325 | 4 |
| E1 | 0.240 | 0.250 | 0.280 | 3 |
| e | 0.100 BSC | | | |
| eA | 0.300 BSC | | | 4 |
| L | 0.115 | 0.130 | 0.150 | 2 |

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

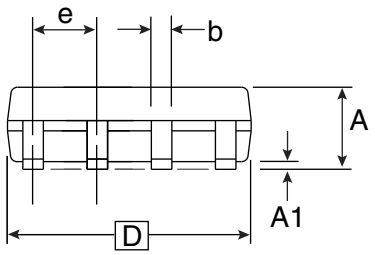
01/09/02

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP) | 8P3 | B |

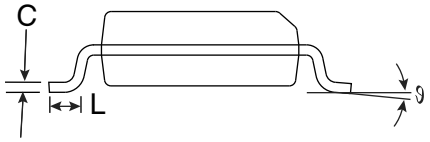
## 7.3 S8S1




Top View




Side View




End View

**COMMON DIMENSIONS**
(Unit of Measure = mm)

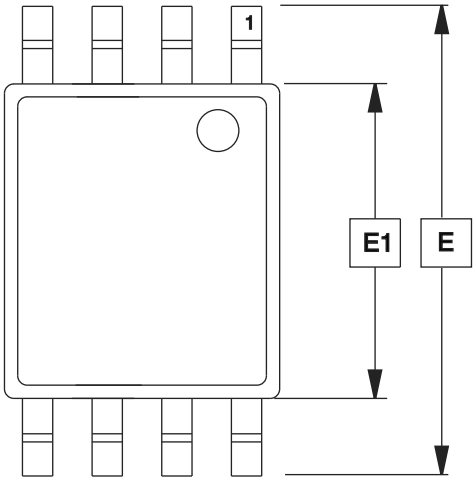
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| E | 5.79 | | 6.20 | |
| E1 | 3.81 | | 3.99 | |
| A | 1.35 | | 1.75 | |
| A1 | 0.1 | | 0.25 | |
| D | 4.80 | | 4.98 | |
| C | 0.17 | | 0.25 | |
| b | 0.31 | | 0.51 | |
| L | 0.4 | | 1.27 | |
| e | 1.27 BSC | | | |
| θ | 0° | | 8° | |

Notes: 1. This drawing is for general information only; refer to JEDEC Drawing MS-012 for proper dimensions, tolerances, datums,etc.

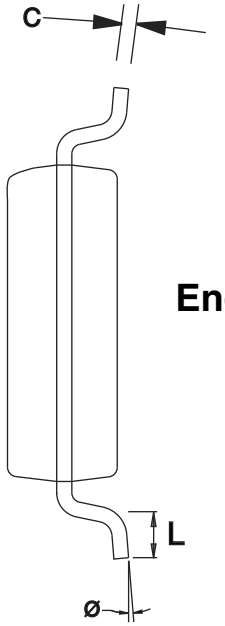
7/28/03

| | | | |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **TITLE**<br>**S8S1**, 8-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline (JEDEC SOIC) | **DRAWING NO.**<br>S8S1 | **REV.**<br>A |

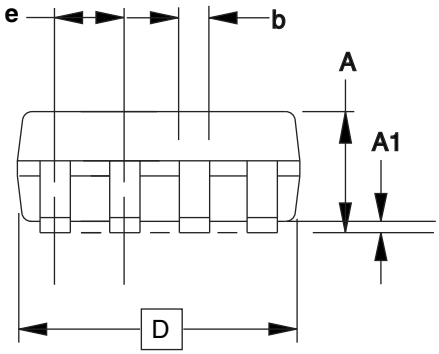
## 7.4 8X




Top View




End View




Side View

**COMMON DIMENSIONS**
(Unit of Measure = mm)

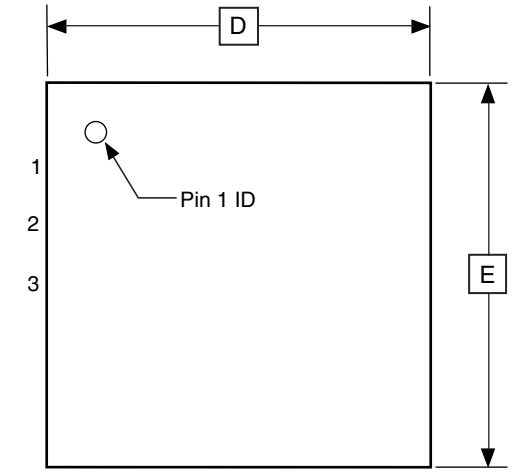
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 1.05 | 1.10 | 1.20 | |
| A1 | 0.05 | 0.10 | 0.15 | |
| b | 0.25 | – | 0.30 | |
| C | – | 0.127 | – | |
| D | 2.90 | 3.05 | 3.10 | |
| E1 | 4.30 | 4.40 | 4.50 | |
| E | 6.20 | 6.40 | 6.60 | |
| e | 0.65 TYP | | | |
| L | 0.50 | 0.60 | 0.70 | |
| ø | 0° | – | 8° | |

Note: These drawings are for general information only. Refer to JEDEC Drawing MO-153AC.

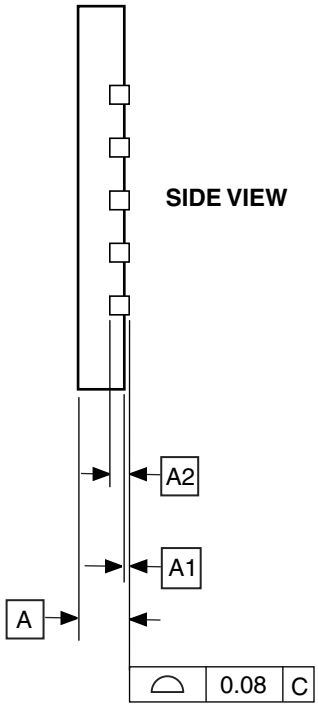
4/14/05

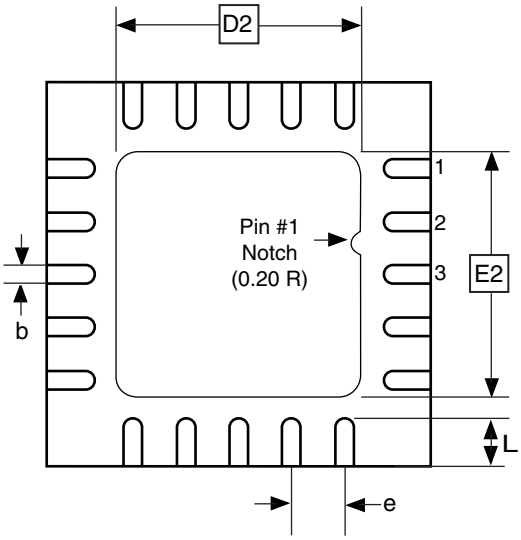
| | | | |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **TITLE**<br>**8X**, 8-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP) | **DRAWING NO.**<br>8X | **REV.**<br>A |

## 7.5 20M1




TOP VIEW




BOTTOM VIEW

**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 | |
| A1 | – | 0.01 | 0.05 | |
| A2 | | 0.20 REF | | |
| b | 0.18 | 0.23 | 0.30 | |
| D | | 4.00 BSC | | |
| D2 | 2.45 | 2.60 | 2.75 | |
| E | | 4.00 BSC | | |
| E2 | 2.45 | 2.60 | 2.75 | |
| e | | 0.50 BSC | | |
| L | 0.35 | 0.40 | 0.55 | |

Note: Reference JEDEC Standard MO-220, Fig. 1 (SAW Singulation) WGGD-5.

10/27/04

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **20M1**, 20-pad, 4 x 4 x 0.8 mm Body, Lead Pitch 0.50 mm,<br>2.6 mm Exposed Pad, Micro Lead Frame Package (MLF) | 20M1 | B |

# 8. Errata

## 8.1 Errata ATtiny25

The revision letter in this section refers to the revision of the ATtiny25 device.

### 8.1.1 Rev D – F

No known errata.

### 8.1.2 Rev B – C

- **EEPROM read may fail at low supply voltage / low clock frequency**

1. **EEPROM read may fail at low supply voltage / low clock frequency**

   Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

   **Problem Fix/Workaround**

   Do not use the EEPROM when clock frequency is below 1MHz and supply voltage is below 2V. If operating frequency can not be raised above 1MHz then supply voltage should be more than 2V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 1MHz.

   This feature is known to be temperature dependent but it has not been characterised. Guidelines are given for room temperature, only.

### 8.1.3 Rev A

Not sampled.

## 8.2 Errata ATtiny45

The revision letter in this section refers to the revision of the ATtiny45 device.

### 8.2.1 Rev F – G

No known errata

### 8.2.2 Rev D – E

- **EEPROM read may fail at low supply voltage / low clock frequency**

1. **EEPROM read may fail at low supply voltage / low clock frequency**

   Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

   **Problem Fix/Workaround**

   Do not use the EEPROM when clock frequency is below 1MHz and supply voltage is below 2V. If operating frequency can not be raised above 1MHz then supply voltage should be more than 2V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 1MHz.

   This feature is known to be temperature dependent but it has not been characterised. Guidelines are given for room temperature, only.

– When using external clock, avoid setting the clock pin as Output.
– Do not read the EEPROM if power down power consumption is important.
– Use VCC lower than 4.5 Volts.

2. **DebugWIRE looses communication when single stepping into interrupts**
   When receiving an interrupt during single stepping, debugwire will loose

   communication.

   **Problem fix / Workaround**
   – When singlestepping, disable interrupts.
   – When debugging interrupts, use breakpoints within the interrupt routine, and run into the interrupt.

3. **PLL not locking**
   When at frequencies below 6.0 MHz, the PLL will not lock

   **Problem fix / Workaround**
   When using the PLL, run at 6.0 MHz or higher.

4. **EEPROM read from application code does not work in Lock Bit Mode 3**
   When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

   **Problem Fix/Work around**
   Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

5. **EEPROM read may fail at low supply voltage / low clock frequency**
   Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

   **Problem Fix/Workaround**
   Do not use the EEPROM when clock frequency is below 1MHz and supply voltage is below 2V. If operating frequency can not be raised above 1MHz then supply voltage should be more than 2V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 1MHz.

   This feature is known to be temperature dependent but it has not been characterized. Guidelines are given for room temperature, only.

## 8.3 Errata ATtiny85

The revision letter in this section refers to the revision of the ATtiny85 device.

### 8.3.1 Rev B – C

No known errata.

### 8.3.2 Rev A

- **EEPROM read may fail at low supply voltage / low clock frequency**

1. **EEPROM read may fail at low supply voltage / low clock frequency**

   Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

   **Problem Fix/Workaround**

   Do not use the EEPROM when clock frequency is below 1MHz and supply voltage is below 2V. If operating frequency can not be raised above 1MHz then supply voltage should be more than 2V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 1MHz.

   This feature is known to be temperature dependent but it has not been characterised. Guidelines are given for room temperature, only.

# 9. Datasheet Revision History

## 9.1 Rev. 2586Q-08/13

1. “Bit 3 – FOC1B: Force Output Compare Match 1B” description in “GTCCR – General Timer/Counter1 Control Register” on page 90 updated: PB3 in “compare match output pin PB3 (OC1B)” corrected to PB4.

## 9.2 Rev. 2586P-06/13

1. Updated description of “EEARH – EEPROM Address Register” and “EEARL – EEPROM Address Register” on page 20.

## 9.3 Rev. 2586O-02/13

Updated ordering codes on page 11, page 12, and page 13.

## 9.4 Rev. 2586N-04/11

1. Added:
   – Section “Capacitive Touch Sensing” on page 6.
2. Updated:
   – Document template.
   – Removed “Preliminary” on front page. All devices now final and in production.
   – Section “Limitations” on page 36.
   – Program example on page 49.
   – Section “Overview” on page 122.
   – Table 17-4 on page 135.
   – Section “Limitations of debugWIRE” on page 140.
   – Section “Serial Programming Algorithm” on page 151.
   – Table 21-7 on page 166.
   – EEPROM errata on pages 19, 19, 20, 21, and 22
   – Ordering information on pages 11, 12, and 13.

## 9.5 Rev. 2586M-07/10

1. Clarified Section 6.4 “Clock Output Buffer” on page 31.
2. Added Ordering Codes -SN and -SNR for ATtiny25 extended temperature.

## 9.6 Rev. 2586L-06/10

1. Added:
   – TSSOP for ATtiny45 in “Features” on page 1, Pinout Figure 1-1 on page 2, Ordering Information in Section 6.2 “ATtiny45” on page 12, and Packaging Information in Section 7.4 “8X” on page 17
   – Table 6-11, “Capacitance of Low-Frequency Crystal Oscillator,” on page 29
   – Figure 22-36 on page 191 and Figure 22-37 on page 191, Typical Characteristics plots for Bandgap Voltage vs. $V_{CC}$ and Temperature
   – Extended temperature in Section 6.1 “ATtiny25” on page 11, Ordering Information

– Tape & reel part numbers in Ordering Information, in Section 6.1 “ATtiny25” on page 11 and Section 6.2 “ATtiny45” on page 12

2. Updated:
   – “Features” on page 1, removed Preliminary from ATtiny25
   – Section 8.4.2 “Code Example” on page 44
   – “PCMSK – Pin Change Mask Register” on page 52, Bit Descriptions
   – “TCCR1 – Timer/Counter1 Control Register” on page 89 and “GTCCR – General Timer/Counter1 Control Register” on page 90, COM bit descriptions clarified
   – Section 20.3.2 “Calibration Bytes” on page 150, frequencies (8 MHz, 6.4 MHz)
   – Table 20-11, “Minimum Wait Delay Before Writing the Next Flash or EEPROM Location,” on page 153, value for $t_{WD\_ERASE}$
   – Table 20-16, “High-voltage Serial Programming Instruction Set for ATtiny25/45/85,” on page 158
   – Table 21-1, “DC Characteristics. $T_A$ = -40°C to +85°C,” on page 161, notes adjusted
   – Table 21-11, “Serial Programming Characteristics, $T_A$ = -40°C to +85°C, $V_{CC}$ = 1.8 - 5.5V (Unless Otherwise Noted),” on page 170, added $t_{SLIV}$
   – Bit syntax throughout the datasheet, e.g. from CS02:0 to CS0[2:0].

## 9.7 Rev. 2586K-01/08

1. Updated Document Template.
2. Added Sections:
   – “Data Retention” on page 6
   – “Low Level Interrupt” on page 49
   – “Device Signature Imprint Table” on page 149
3. Updated Sections:
   – “Internal PLL for Fast Peripheral Clock Generation - clkPCK” on page 24
   – “System Clock and Clock Options” on page 23
   – “Internal PLL in ATtiny15 Compatibility Mode” on page 24
   – “Sleep Modes” on page 34
   – “Software BOD Disable” on page 35
   – “External Interrupts” on page 49
   – “Timer/Counter1 in PWM Mode” on page 97
   – “USI – Universal Serial Interface” on page 108
   – “Temperature Measurement” on page 133
   – “Reading Lock, Fuse and Signature Data from Software” on page 143
   – “Program And Data Memory Lock Bits” on page 147
   – “Fuse Bytes” on page 148
   – “Signature Bytes” on page 150
   – “Calibration Bytes” on page 150
   – “System and Reset Characteristics” on page 165
4. Added Figures:
   – “Reset Pin Output Voltage vs. Sink Current ($V_{CC}$ = 3V)” on page 184
   – “Reset Pin Output Voltage vs. Sink Current ($V_{CC}$ = 5V)” on page 185
   – “Reset Pin Output Voltage vs. Source Current ($V_{CC}$ = 3V)” on page 185

## 9.9 Rev. 2586I-09/06

1. All Characterization data moved to “Electrical Characteristics” on page 161.
2. All Register Descriptions are gathered up in seperate sections in the end of each chapter.
3. Updated Table 11-3 on page 78, Table 11-5 on page 79, Table 11-6 on page 80 and Table 20-4 on page 148.
4. Updated “Calibrated Internal Oscillator” on page 27.
5. Updated Note in Table 7-1 on page 34.
6. Updated “System Control and Reset” on page 39.
7. Updated Register Description in “I/O Ports” on page 53.
8. Updated Features in “USI – Universal Serial Interface” on page 108.
9. Updated Code Example in “SPI Master Operation Example” on page 110 and “SPI Slave Operation Example” on page 111.
10. Updated “Analog Comparator Multiplexed Input” on page 119.
11. Updated Figure 17-1 on page 123.
12. Updated “Signature Bytes” on page 150.
13. Updated “Electrical Characteristics” on page 161.

## 9.10 Rev. 2586H-06/06

1. Updated “Calibrated Internal Oscillator” on page 27.
2. Updated Table 6.5.1 on page 31.
3. Added Table 21-2 on page 164.

## 9.11 Rev. 2586G-05/06

1. Updated “Internal PLL for Fast Peripheral Clock Generation - clkPCK” on page 24.
2. Updated “Default Clock Source” on page 30.
3. Updated “Low-Frequency Crystal Oscillator” on page 29.
4. Updated “Calibrated Internal Oscillator” on page 27.
5. Updated “Clock Output Buffer” on page 31.
6. Updated “Power Management and Sleep Modes” on page 34.
7. Added “Software BOD Disable” on page 35.
8. Updated Figure 16-1 on page 119.
9. Updated “Bit 6 – ACBG: Analog Comparator Bandgap Select” on page 120.
10. Added note for Table 17-2 on page 125.
11. Updated “Register Summary” on page 7.

## 9.12 Rev. 2586F-04/06

1. Updated “Digital Input Enable and Sleep Modes” on page 57.
2. Updated Table 20-16 on page 158.
3. Updated “Ordering Information” on page 11.

## 9.13 Rev. 2586E-03/06

1. Updated Features in “Analog to Digital Converter” on page 122.
2. Updated Operation in “Analog to Digital Converter” on page 122.
3. Updated Table 17-2 on page 133.
4. Updated Table 17-3 on page 134.
5. Updated “Errata” on page 19.

## 9.14 Rev. 2586D-02/06

1. Updated Table 6-13 on page 30, Table 6-10 on page 29, Table 6-3 on page 26, Table 6-9 on page 28, Table 6-5 on page 26, Table 9-1 on page 48,Table 17-4 on page 135, Table 20-16 on page 158, Table 21-8 on page 167.
2. Updated “Timer/Counter1 in PWM Mode” on page 86.
3. Updated text “Bit 2 – TOV1: Timer/Counter1 Overflow Flag” on page 93.
4. Updated values in “DC Characteristics” on page 161.
5. Updated “Register Summary” on page 7.
6. Updated “Ordering Information” on page 11.
7. Updated Rev B and C in “Errata ATtiny45” on page 19.
8. All references to power-save mode are removed.
9. Updated Register Adresses.

## 9.15 Rev. 2586C-06/05

1. Updated “Features” on page 1.
2. Updated Figure 1-1 on page 2.
3. Updated Code Examples on page 18 and page 19.
4. Moved “Temperature Measurement” to Section 17.12 page 133.
5. Updated “Register Summary” on page 7.
6. Updated “Ordering Information” on page 11.

## 9.16 Rev. 2586B-05/05

1. CLKI added, instances of EEMWE/EEWE renamed EEMPE/EEPE, removed some TBD.
   Removed “Preliminary Description” from “Temperature Measurement” on page 133.
2. Updated “Features” on page 1.
3. Updated Figure 1-1 on page 2 and Figure 8-1 on page 39.
4. Updated Table 7-2 on page 38, Table 10-4 on page 63, Table 10-5 on page 63
5. Updated “Serial Programming Instruction set” on page 153.
6. Updated SPH register in “Instruction Set Summary” on page 9.
7. Updated “DC Characteristics” on page 161.
8. Updated “Ordering Information” on page 11.
9. Updated “Errata” on page 19.

## 9.17 Rev. 2586A-02/05

Initial revision.

Atmel® | Enabling Unlimited Possibilities®

**Atmel Corporation**
1600 Technology Drive
San Jose, CA 95110
USA
**Tel:** (+1) (408) 441-0311
**Fax:** (+1) (408) 487-2600
www.atmel.com

**Atmel Asia Limited**
Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Roa
Kwun Tong, Kowloon
HONG KONG
**Tel:** (+852) 2245-6100
**Fax:** (+852) 2722-1369

**Atmel Munich GmbH**
Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY
**Tel:** (+49) 89-31970-0
**Fax:** (+49) 89-3194621

**Atmel Japan G.K.**
16F Shin-Osaki Kangyo Bldg
1-6-4 Osaki, Shinagawa-ku
Tokyo 141-0032
JAPAN
**Tel:** (+81) (3) 6417-0300
**Fax:** (+81) (3) 6417-0370