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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | AVR |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | USI |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 6 |
| Program Memory Size | 8KB (4K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 8-SOIC (0.209", 5.30mm Width) |
| Supplier Device Package | 8-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/atmel/attiny85-20sh |

Port B also serves the functions of various special features of the ATtiny25/45/85 as listed in “Alternate Functions of Port B” on page 60.

On ATtiny25, the programmable I/O ports PB3 and PB4 (pins 2 and 3) are exchanged in ATtiny15 Compatibility Mode for supporting the backward compatibility with ATtiny15.

1.1.4 **RESET**

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in Table 21-4 on page 165. Shorter pulses are not guaranteed to generate a reset.

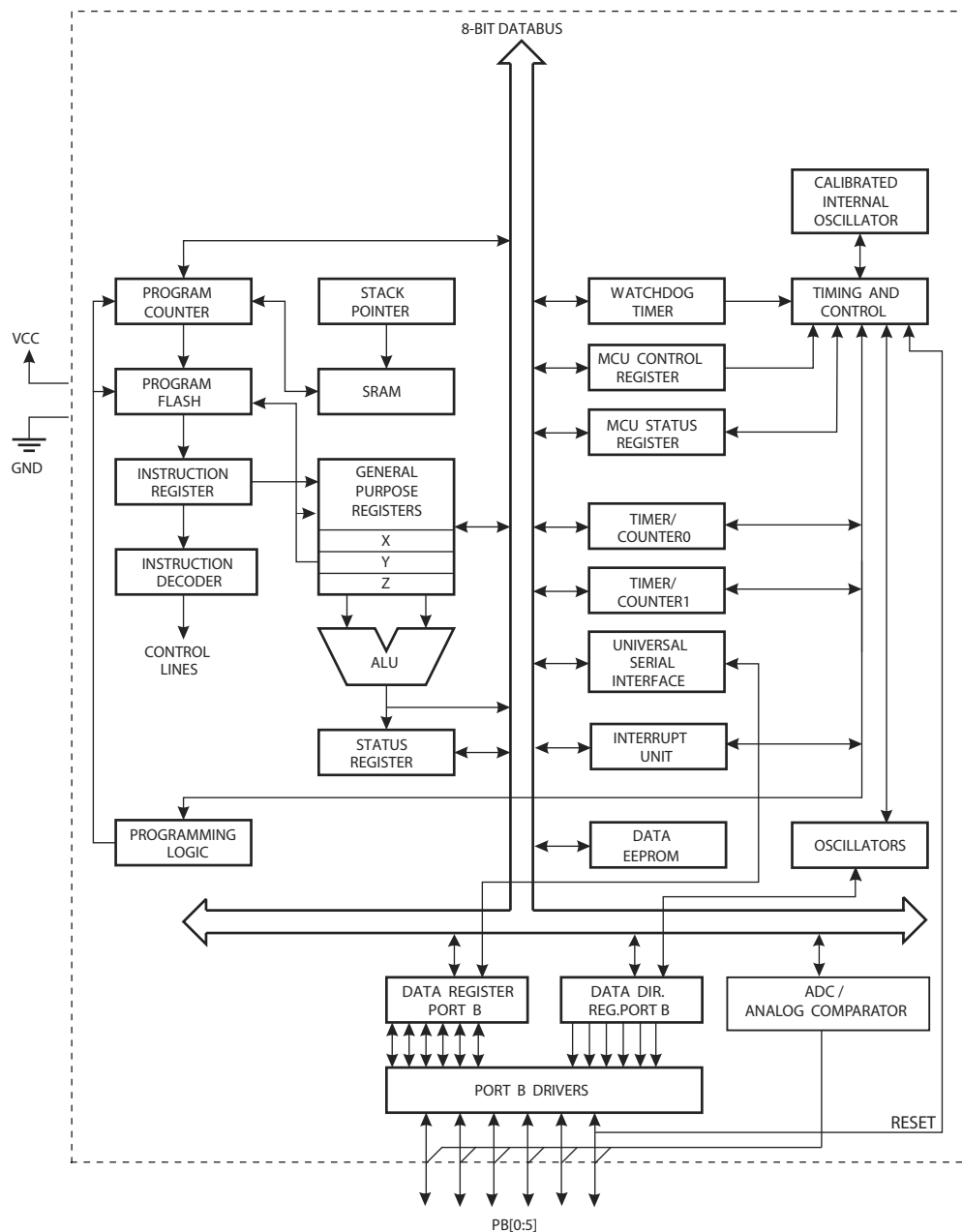
The reset pin can also be used as a (weak) I/O pin.

2. Overview

The ATtiny25/45/85 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny25/45/85 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny25/45/85 provides the following features: 2/4/8K bytes of In-System Programmable Flash, 128/256/512 bytes EEPROM, 128/256/256 bytes SRAM, 6 general purpose I/O lines, 32 general purpose working registers, one 8-bit Timer/Counter with compare modes, one 8-bit high speed Timer/Counter, Universal Serial Interface, Internal and External Interrupts, a 4-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. Power-down mode saves the register contents, disabling all chip functions until the next Interrupt or Hardware Reset. ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the Program memory to be re-programmed In-System through an SPI serial interface, by a conventional non-volatile memory programmer or by an On-chip boot code running on the AVR core.

The ATtiny25/45/85 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators and Evaluation kits.

3. About

3.1 Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in the extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically, this means “LDS” and “STS” combined with “SBR”, “SBRC”, “SBR”, and “CBR”. Note that not all AVR devices include an extended I/O map.

3.3 Capacitive Touch Sensing

Atmel QTouch Library provides a simple to use solution for touch sensitive interfaces on Atmel AVR microcontrollers. The QTouch Library includes support for QTouch[®] and QMatrix[®] acquisition methods.

Touch sensing is easily added to any application by linking the QTouch Library and using the Application Programming Interface (API) of the library to define the touch channels and sensors. The application then calls the API to retrieve channel information and determine the state of the touch sensor.

The QTouch Library is free and can be downloaded from the Atmel website. For more information and details of implementation, refer to the QTouch Library User Guide – also available from the Atmel website.

3.4 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

should never be written.

2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVR's, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

5. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|--|----------|--|--|---------------|---------|
| ARITHMETIC AND LOGIC INSTRUCTIONS | | | | | |
| ADD | Rd, Rr | Add two Registers | $Rd \leftarrow Rd + Rr$ | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | $Rd \leftarrow Rd + Rr + C$ | Z,C,N,V,H | 1 |
| ADIW | Rdl, K | Add Immediate to Word | $Rdh:Rdl \leftarrow Rdh:Rdl + K$ | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | $Rd \leftarrow Rd - Rr$ | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | $Rd \leftarrow Rd - K$ | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | $Rd \leftarrow Rd - Rr - C$ | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$ | Z,C,N,V,H | 1 |
| SBIW | Rdl, K | Subtract Immediate from Word | $Rdh:Rdl \leftarrow Rdh:Rdl - K$ | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | $Rd \leftarrow Rd \bullet Rr$ | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | $Rd \leftarrow Rd \bullet K$ | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | $Rd \leftarrow Rd \vee Rr$ | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | $Rd \leftarrow Rd \oplus Rr$ | Z,N,V | 1 |
| COM | Rd | One's Complement | $Rd \leftarrow 0xFF - Rd$ | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | $Rd \leftarrow 0x00 - Rd$ | Z,C,N,V,H | 1 |
| SBR | Rd, K | Set Bit(s) in Register | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| CBR | Rd, K | Clear Bit(s) in Register | $Rd \leftarrow Rd \bullet (0xFF - K)$ | Z,N,V | 1 |
| INC | Rd | Increment | $Rd \leftarrow Rd + 1$ | Z,N,V | 1 |
| DEC | Rd | Decrement | $Rd \leftarrow Rd - 1$ | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | $Rd \leftarrow Rd \bullet Rd$ | Z,N,V | 1 |
| CLR | Rd | Clear Register | $Rd \leftarrow Rd \oplus Rd$ | Z,N,V | 1 |
| SER | Rd | Set Register | $Rd \leftarrow 0xFF$ | None | 1 |
| BRANCH INSTRUCTIONS | | | | | |
| RJMP | k | Relative Jump | $PC \leftarrow PC + k + 1$ | None | 2 |
| JMP | | Indirect Jump to (Z) | $PC \leftarrow Z$ | None | 2 |
| RCALL | k | Relative Subroutine Call | $PC \leftarrow PC + k + 1$ | None | 3 |
| ICALL | | Indirect Call to (Z) | $PC \leftarrow Z$ | None | 3 |
| RET | | Subroutine Return | $PC \leftarrow STACK$ | None | 4 |
| RETI | | Interrupt Return | $PC \leftarrow STACK$ | I | 4 |
| CPSE | Rd, Rr | Compare, Skip if Equal | if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| CP | Rd, Rr | Compare | $Rd - Rr$ | Z, N, V, C, H | 1 |
| CPC | Rd, Rr | Compare with Carry | $Rd - Rr - C$ | Z, N, V, C, H | 1 |
| CPI | Rd, K | Compare Register with Immediate | $Rd - K$ | Z, N, V, C, H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if $(Rr(b)=0)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBRSC | Rr, b | Skip if Bit in Register is Set | if $(Rr(b)=1)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if $(P(b)=0)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBSIS | P, b | Skip if Bit in I/O Register is Set | if $(P(b)=1)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BREQ | k | Branch if Equal | if $(Z = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRNE | k | Branch if Not Equal | if $(Z = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCS | k | Branch if Carry Set | if $(C = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if $(C = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if $(C = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLO | k | Branch if Lower | if $(C = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRMI | k | Branch if Minus | if $(N = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRPL | k | Branch if Plus | if $(N = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if $(H = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if $(H = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if $(T = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if $(T = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if $(V = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if $(V = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if $(I = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if $(I = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BIT AND BIT-TEST INSTRUCTIONS | | | | | |
| SBI | P, b | Set Bit in I/O Register | $I/O(P, b) \leftarrow 1$ | None | 2 |
| CBI | P, b | Clear Bit in I/O Register | $I/O(P, b) \leftarrow 0$ | None | 2 |
| LSL | Rd | Logical Shift Left | $Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$ | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | $Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$ | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | $Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$ | Z,C,N,V | 1 |
| ROR | Rd | Rotate Right Through Carry | $Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$ | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | $Rd(n) \leftarrow Rd(n+1), n=0..6$ | Z,C,N,V | 1 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|-----------------------------------|----------|----------------------------------|--|---------|---------|
| SWAP | Rd | Swap Nibbles | $Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$ | None | 1 |
| BSET | s | Flag Set | $SREG(s) \leftarrow 1$ | SREG(s) | 1 |
| BCLR | s | Flag Clear | $SREG(s) \leftarrow 0$ | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | $T \leftarrow Rr(b)$ | T | 1 |
| BLD | Rd, b | Bit load from T to Register | $Rd(b) \leftarrow T$ | None | 1 |
| SEC | | Set Carry | $C \leftarrow 1$ | C | 1 |
| CLC | | Clear Carry | $C \leftarrow 0$ | C | 1 |
| SEN | | Set Negative Flag | $N \leftarrow 1$ | N | 1 |
| CLN | | Clear Negative Flag | $N \leftarrow 0$ | N | 1 |
| SEZ | | Set Zero Flag | $Z \leftarrow 1$ | Z | 1 |
| CLZ | | Clear Zero Flag | $Z \leftarrow 0$ | Z | 1 |
| SEI | | Global Interrupt Enable | $I \leftarrow 1$ | I | 1 |
| CLI | | Global Interrupt Disable | $I \leftarrow 0$ | I | 1 |
| SES | | Set Signed Test Flag | $S \leftarrow 1$ | S | 1 |
| CLS | | Clear Signed Test Flag | $S \leftarrow 0$ | S | 1 |
| SEV | | Set Twos Complement Overflow | $V \leftarrow 1$ | V | 1 |
| CLV | | Clear Twos Complement Overflow | $V \leftarrow 0$ | V | 1 |
| SET | | Set T in SREG | $T \leftarrow 1$ | T | 1 |
| CLT | | Clear T in SREG | $T \leftarrow 0$ | T | 1 |
| SEH | | Set Half Carry Flag in SREG | $H \leftarrow 1$ | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | $H \leftarrow 0$ | H | 1 |
| DATA TRANSFER INSTRUCTIONS | | | | | |
| MOV | Rd, Rr | Move Between Registers | $Rd \leftarrow Rr$ | None | 1 |
| MOVW | Rd, Rr | Copy Register Word | $Rd+1:Rd \leftarrow Rr+1:Rr$ | None | 1 |
| LDI | Rd, K | Load Immediate | $Rd \leftarrow K$ | None | 1 |
| LD | Rd, X | Load Indirect | $Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Inc. | $Rd \leftarrow (X), X \leftarrow X + 1$ | None | 2 |
| LD | Rd, -X | Load Indirect and Pre-Dec. | $X \leftarrow X - 1, Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, Y | Load Indirect | $Rd \leftarrow (Y)$ | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Inc. | $Rd \leftarrow (Y), Y \leftarrow Y + 1$ | None | 2 |
| LD | Rd, -Y | Load Indirect and Pre-Dec. | $Y \leftarrow Y - 1, Rd \leftarrow (Y)$ | None | 2 |
| LDD | Rd, Y+q | Load Indirect with Displacement | $Rd \leftarrow (Y + q)$ | None | 2 |
| LD | Rd, Z | Load Indirect | $Rd \leftarrow (Z)$ | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Inc. | $Rd \leftarrow (Z), Z \leftarrow Z + 1$ | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Dec. | $Z \leftarrow Z - 1, Rd \leftarrow (Z)$ | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | $Rd \leftarrow (Z + q)$ | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | $Rd \leftarrow (k)$ | None | 2 |
| ST | X, Rr | Store Indirect | $(X) \leftarrow Rr$ | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Inc. | $(X) \leftarrow Rr, X \leftarrow X + 1$ | None | 2 |
| ST | -X, Rr | Store Indirect and Pre-Dec. | $X \leftarrow X - 1, (X) \leftarrow Rr$ | None | 2 |
| ST | Y, Rr | Store Indirect | $(Y) \leftarrow Rr$ | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Inc. | $(Y) \leftarrow Rr, Y \leftarrow Y + 1$ | None | 2 |
| ST | -Y, Rr | Store Indirect and Pre-Dec. | $Y \leftarrow Y - 1, (Y) \leftarrow Rr$ | None | 2 |
| STD | Y+q, Rr | Store Indirect with Displacement | $(Y + q) \leftarrow Rr$ | None | 2 |
| ST | Z, Rr | Store Indirect | $(Z) \leftarrow Rr$ | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Inc. | $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-Dec. | $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ | None | 2 |
| STD | Z+q, Rr | Store Indirect with Displacement | $(Z + q) \leftarrow Rr$ | None | 2 |
| STS | k, Rr | Store Direct to SRAM | $(k) \leftarrow Rr$ | None | 2 |
| LPM | | Load Program Memory | $R0 \leftarrow (Z)$ | None | 3 |
| LPM | Rd, Z | Load Program Memory | $Rd \leftarrow (Z)$ | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Inc | $Rd \leftarrow (Z), Z \leftarrow Z + 1$ | None | 3 |
| SPM | | Store Program Memory | $(z) \leftarrow R1:R0$ | None | |
| IN | Rd, P | In Port | $Rd \leftarrow P$ | None | 1 |
| OUT | P, Rr | Out Port | $P \leftarrow Rr$ | None | 1 |
| PUSH | Rr | Push Register on Stack | $STACK \leftarrow Rr$ | None | 2 |
| POP | Rd | Pop Register from Stack | $Rd \leftarrow STACK$ | None | 2 |
| MCU CONTROL INSTRUCTIONS | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/Timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

6. Ordering Information

6.1 ATtiny25

| Speed (MHz) ⁽¹⁾ | Supply Voltage (V) | Temperature Range | Package ⁽²⁾ | Ordering Code ⁽³⁾ |
|----------------------------|--------------------|--|------------------------|--|
| 10 | 1.8 – 5.5 | Industrial (-40°C to +85°C) ⁽⁴⁾ | 8P3 | ATtiny25V-10PU |
| | | | 8S2 | ATtiny25V-10SU ATtiny25V-10SUR ATtiny25V-10SH ATtiny25V-10SHR |
| | | | S8S1 | ATtiny25V-10SSU ATtiny25V-10SSUR ATtiny25V-10SSH ATtiny25V-10SSHR |
| | | | 20M1 | ATtiny25V-10MU ATtiny25V-10MUR |
| | | Industrial (-40°C to +105°C) ⁽⁵⁾ | 8S2 | ATtiny25V-10SN ATtiny25V-10SNR |
| | | | S8S1 | ATtiny25V-10SSN ATtiny25V-10SSNR |
| | | Industrial (-40°C to +125°C) ⁽⁶⁾ | 20M1 | ATtiny25V-10MF ATtiny25V-10MFR |
| | | | | |
| 20 | 2.7 – 5.5 | Industrial (-40°C to +85°C) ⁽⁴⁾ | 8P3 | ATtiny25-20PU |
| | | | 8S2 | ATtiny25-20SU ATtiny25-20SUR ATtiny25-20SH ATtiny25-20SHR |
| | | | S8S1 | ATtiny25-20SSU ATtiny25-20SSUR ATtiny25-20SSH ATtiny25-20SSHR |
| | | | 20M1 | ATtiny25-20MU ATtiny25-20MUR |
| | | Industrial (-40°C to +105°C) ⁽⁵⁾ | 8S2 | ATtiny25-20SN ATtiny25-20SNR |
| | | | S8S1 | ATtiny25-20SSN ATtiny25-20SSNR |
| | | Industrial (-40°C to +125°C) ⁽⁶⁾ | 20M1 | ATtiny25-20MF ATtiny25-20MFR |
| | | | | |

- Notes:
1. For speed vs. supply voltage, see section 21.3 “Speed” on page 163.
 2. All Pb-free, halide-free, fully green, and comply with European directive for Restriction of Hazardous Substances (RoHS).
 3. Code indicators: H = NiPdAu lead finish, U/N = matte tin, R = tape & reel.
 4. Can also be supplied in wafer form. Contact your local Atmel sales office for ordering information and minimum quantities.
 5. For characteristics, see “Appendix A – Specification at 105°C”.
 6. For characteristics, see “Appendix B – Specification at 125°C”.

| Package Types | |
|---------------|---|
| 8P3 | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 8S2 | 8-lead, 0.208" Wide, Plastic Gull-Wing Small Outline (EIAJ SOIC) |
| S8S1 | 8-lead, 0.150" Wide, Plastic Gull-Wing Small Outline (JEDEC SOIC) |
| 20M1 | 20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF) |

6.3 ATtiny85

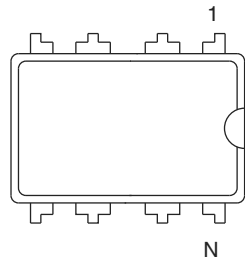
| Speed (MHz) ⁽¹⁾ | Supply Voltage (V) | Temperature Range | Package ⁽²⁾ | Ordering Code ⁽³⁾ |
|----------------------------|--------------------|---|------------------------|--|
| 10 | 1.8 – 5.5 | Industrial (-40°C to +85°C) ⁽⁴⁾ | 8P3 | ATtiny85V-10PU |
| | | | 8S2 | ATtiny85V-10SU ATtiny85V-10SUR ATtiny85V-10SH ATtiny85V-10SHR |
| | | | 20M1 | ATtiny85V-10MU ATtiny85V-10MUR |
| 20 | 2.7 – 5.5 | Industrial (-40°C to +85°C) ⁽⁴⁾ | 8P3 | ATtiny85-20PU |
| | | | 8S2 | ATtiny85-20SU ATtiny85-20SUR ATtiny85-20SH ATtiny85-20SHR |
| | | | 20M1 | ATtiny85-20MU ATtiny85-20MUR |

- Notes:
1. For speed vs. supply voltage, see section 21.3 “Speed” on page 163.
 2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
 3. Code indicators:
 - H: NiPdAu lead finish
 - U: matte tin
 - R: tape & reel
 4. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

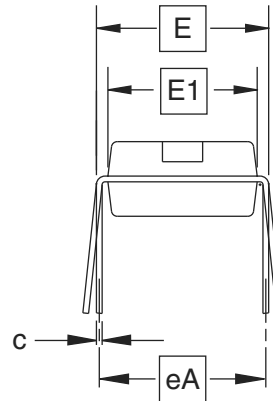
| Package Types | |
|---------------|---|
| 8P3 | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 8S2 | 8-lead, 0.208" Wide, Plastic Gull-Wing Small Outline (EIAJ SOIC) |
| 20M1 | 20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF) |

7. Packaging Information

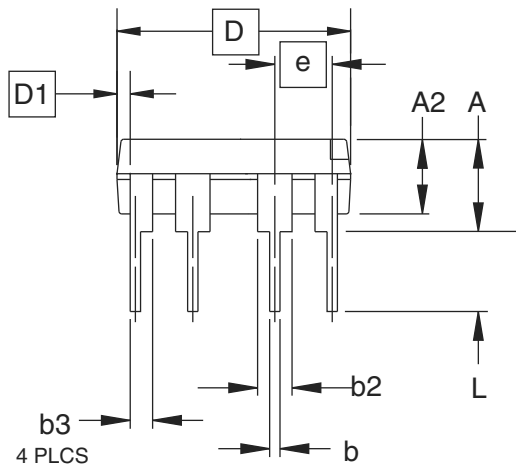
7.1 8P3



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-------|-------|------|
| A | | | 0.210 | 2 |
| A2 | 0.115 | 0.130 | 0.195 | |
| b | 0.014 | 0.018 | 0.022 | 5 |
| b2 | 0.045 | 0.060 | 0.070 | 6 |
| b3 | 0.030 | 0.039 | 0.045 | 6 |
| c | 0.008 | 0.010 | 0.014 | |
| D | 0.355 | 0.365 | 0.400 | 3 |
| D1 | 0.005 | | | 3 |
| E | 0.300 | 0.310 | 0.325 | 4 |
| E1 | 0.240 | 0.250 | 0.280 | 3 |
| e | 0.100 BSC | | | |
| eA | 0.300 BSC | | | 4 |
| L | 0.115 | 0.130 | 0.150 | 2 |

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
 2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
 3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
 4. E and eA measured with the leads constrained to be perpendicular to datum.
 5. Pointed or rounded lead tips are preferred to ease insertion.
 6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

01/09/02

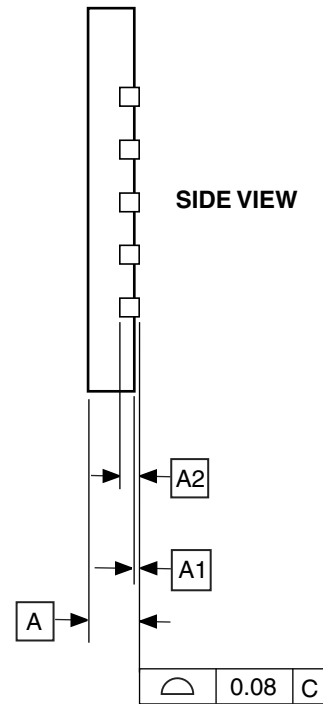
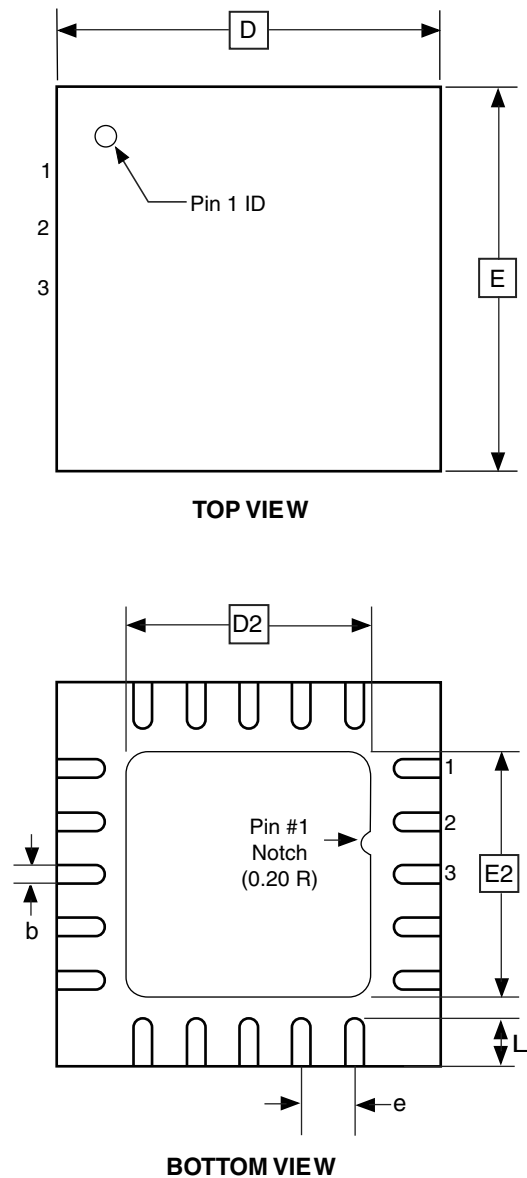
2325 Orchard Parkway
San Jose, CA 95131

TITLE
8P3, 8-lead, 0.300" Wide Body, Plastic Dual
In-line Package (PDIP)

DRAWING NO.
8P3

REV.
B

7.5 20M1



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|------|------|------|
| A | 0.70 | 0.75 | 0.80 | |
| A1 | — | 0.01 | 0.05 | |
| A2 | 0.20 REF | | | |
| b | 0.18 | 0.23 | 0.30 | |
| D | 4.00 BSC | | | |
| D2 | 2.45 | 2.60 | 2.75 | |
| E | 4.00 BSC | | | |
| E2 | 2.45 | 2.60 | 2.75 | |
| e | 0.50 BSC | | | |
| L | 0.35 | 0.40 | 0.55 | |

Note: Reference JEDEC Standard MO-220, Fig. 1 (SAW Singulation) WGGD-5.

10/27/04



2325 Orchard Parkway
San Jose, CA 95131

TITLE

20M1, 20-pad, 4 x 4 x 0.8 mm Body, Lead Pitch 0.50 mm,
2.6 mm Exposed Pad, Micro Lead Frame Package (MLF)

DRAWING NO.

20M1

REV.

B

8.2.3 Rev B – C

- PLL not locking
- EEPROM read from application code does not work in Lock Bit Mode 3
- EEPROM read may fail at low supply voltage / low clock frequency
- Timer Counter 1 PWM output generation on OC1B- XOC1B does not work correctly

1. PLL not locking

When at frequencies below 6.0 MHz, the PLL will not lock

Problem fix / Workaround

When using the PLL, run at 6.0 MHz or higher.

2. EEPROM read from application code does not work in Lock Bit Mode 3

When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

Problem Fix/Work around

Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

3. EEPROM read may fail at low supply voltage / low clock frequency

Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

Problem Fix/Workaround

Do not use the EEPROM when clock frequency is below 1MHz and supply voltage is below 2V. If operating frequency can not be raised above 1MHz then supply voltage should be more than 2V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 1MHz.

This feature is known to be temperature dependent but it has not been characterised. Guidelines are given for room temperature, only.

4. Timer Counter 1 PWM output generation on OC1B – XOC1B does not work correctly

Timer Counter1 PWM output OC1B-XOC1B does not work correctly. Only in the case when the control bits, COM1B1 and COM1B0 are in the same mode as COM1A1 and COM1A0, respectively, the OC1B-XOC1B output works correctly.

Problem Fix/Work around

The only workaround is to use same control setting on COM1A[1:0] and COM1B[1:0] control bits, see table 14-4 in the data sheet. The problem has been fixed for Tiny45 rev D.

8.2.4 Rev A

- Too high power down power consumption
- DebugWIRE loses communication when single stepping into interrupts
- PLL not locking
- EEPROM read from application code does not work in Lock Bit Mode 3
- EEPROM read may fail at low supply voltage / low clock frequency

1. Too high power down power consumption

Three situations will lead to a too high power down power consumption. These are:

- An external clock is selected by fuses, but the I/O PORT is still enabled as an output.
- The EEPROM is read before entering power down.
- VCC is 4.5 volts or higher.

Problem fix / Workaround

- When using external clock, avoid setting the clock pin as Output.
- Do not read the EEPROM if power down power consumption is important.
- Use VCC lower than 4.5 Volts.

2. DebugWIRE loses communication when single stepping into interrupts

When receiving an interrupt during single stepping, debugwire will lose communication.

Problem fix / Workaround

- When singlestepping, disable interrupts.
- When debugging interrupts, use breakpoints within the interrupt routine, and run into the interrupt.

3. PLL not locking

When at frequencies below 6.0 MHz, the PLL will not lock

Problem fix / Workaround

When using the PLL, run at 6.0 MHz or higher.

4. EEPROM read from application code does not work in Lock Bit Mode 3

When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

Problem Fix/Work around

Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

5. EEPROM read may fail at low supply voltage / low clock frequency

Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

Problem Fix/Workaround

Do not use the EEPROM when clock frequency is below 1MHz and supply voltage is below 2V. If operating frequency can not be raised above 1MHz then supply voltage should be more than 2V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 1MHz.

This feature is known to be temperature dependent but it has not been characterized. Guidelines are given for room temperature, only.

8.3 Errata ATtiny85

The revision letter in this section refers to the revision of the ATtiny85 device.

8.3.1 Rev B – C

No known errata.

8.3.2 Rev A

- **EEPROM read may fail at low supply voltage / low clock frequency**

1. **EEPROM read may fail at low supply voltage / low clock frequency**

Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

Problem Fix/Workaround

Do not use the EEPROM when clock frequency is below 1MHz and supply voltage is below 2V. If operating frequency can not be raised above 1MHz then supply voltage should be more than 2V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 1MHz.

This feature is known to be temperature dependent but it has not been characterised. Guidelines are given for room temperature, only.

9. Datasheet Revision History

9.1 Rev. 2586Q-08/13

1. “Bit 3 – FOC1B: Force Output Compare Match 1B” description in “GTCCR – General Timer/Counter1 Control Register” on page 90 updated: PB3 in “compare match output pin PB3 (OC1B)” corrected to PB4.

9.2 Rev. 2586P-06/13

1. Updated description of “EEARH – EEPROM Address Register” and “EEARL – EEPROM Address Register” on page 20.

9.3 Rev. 2586O-02/13

Updated ordering codes on page 11, page 12, and page 13.

9.4 Rev. 2586N-04/11

1. Added:
 - Section “Capacitive Touch Sensing” on page 6.
2. Updated:
 - Document template.
 - Removed “Preliminary” on front page. All devices now final and in production.
 - Section “Limitations” on page 36.
 - Program example on page 49.
 - Section “Overview” on page 122.
 - Table 17-4 on page 135.
 - Section “Limitations of debugWIRE” on page 140.
 - Section “Serial Programming Algorithm” on page 151.
 - Table 21-7 on page 166.
 - EEPROM errata on pages 19, 19, 20, 21, and 22
 - Ordering information on pages 11, 12, and 13.

9.5 Rev. 2586M-07/10

1. Clarified Section 6.4 “Clock Output Buffer” on page 31.
2. Added Ordering Codes -SN and -SNR for ATtiny25 extended temperature.

9.6 Rev. 2586L-06/10

1. Added:
 - TSSOP for ATtiny45 in “Features” on page 1, Pinout Figure 1-1 on page 2, Ordering Information in Section 6.2 “ATtiny45” on page 12, and Packaging Information in Section 7.4 “8X” on page 17
 - Table 6-11, “Capacitance of Low-Frequency Crystal Oscillator,” on page 29
 - Figure 22-36 on page 191 and Figure 22-37 on page 191, Typical Characteristics plots for Bandgap Voltage vs. V_{CC} and Temperature
 - Extended temperature in Section 6.1 “ATtiny25” on page 11, Ordering Information

- Tape & reel part numbers in Ordering Information, in Section 6.1 “ATtiny25” on page 11 and Section 6.2 “ATtiny45” on page 12
- 2. Updated:
 - “Features” on page 1, removed Preliminary from ATtiny25
 - Section 8.4.2 “Code Example” on page 44
 - “PCMSK – Pin Change Mask Register” on page 52, Bit Descriptions
 - “TCCR1 – Timer/Counter1 Control Register” on page 89 and “GTCCR – General Timer/Counter1 Control Register” on page 90, COM bit descriptions clarified
 - Section 20.3.2 “Calibration Bytes” on page 150, frequencies (8 MHz, 6.4 MHz)
 - Table 20-11, “Minimum Wait Delay Before Writing the Next Flash or EEPROM Location,” on page 153, value for t_{WD_ERASE}
 - Table 20-16, “High-voltage Serial Programming Instruction Set for ATtiny25/45/85,” on page 158
 - Table 21-1, “DC Characteristics. $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$,” on page 161, notes adjusted
 - Table 21-11, “Serial Programming Characteristics, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 1.8 - 5.5\text{V}$ (Unless Otherwise Noted),” on page 170, added t_{SLIV}
 - Bit syntax throughout the datasheet, e.g. from CS02:0 to CS0[2:0].

9.7 Rev. 2586K-01/08

1. Updated Document Template.
2. Added Sections:
 - “Data Retention” on page 6
 - “Low Level Interrupt” on page 49
 - “Device Signature Imprint Table” on page 149
3. Updated Sections:
 - “Internal PLL for Fast Peripheral Clock Generation - clkPCK” on page 24
 - “System Clock and Clock Options” on page 23
 - “Internal PLL in ATtiny15 Compatibility Mode” on page 24
 - “Sleep Modes” on page 34
 - “Software BOD Disable” on page 35
 - “External Interrupts” on page 49
 - “Timer/Counter1 in PWM Mode” on page 97
 - “USI – Universal Serial Interface” on page 108
 - “Temperature Measurement” on page 133
 - “Reading Lock, Fuse and Signature Data from Software” on page 143
 - “Program And Data Memory Lock Bits” on page 147
 - “Fuse Bytes” on page 148
 - “Signature Bytes” on page 150
 - “Calibration Bytes” on page 150
 - “System and Reset Characteristics” on page 165
4. Added Figures:
 - “Reset Pin Output Voltage vs. Sink Current ($V_{CC} = 3\text{V}$)” on page 184
 - “Reset Pin Output Voltage vs. Sink Current ($V_{CC} = 5\text{V}$)” on page 185
 - “Reset Pin Output Voltage vs. Source Current ($V_{CC} = 3\text{V}$)” on page 185

6. Updated “Internal PLL for Fast Peripheral Clock Generation - clkPCK” on page 24.
7. Replaced single clocking system figure with two: Figure 6-2 and Figure 6-3.
8. Updated Table 6-1 on page 25, Table 6-13 on page 30 and Table 6-6 on page 27.
9. Updated “Calibrated Internal Oscillator” on page 27.
10. Updated Table 6-5 on page 26.
11. Updated “OSCCAL – Oscillator Calibration Register” on page 31.
12. Updated “CLKPR – Clock Prescale Register” on page 32.
13. Updated “Power-down Mode” on page 35.
14. Updated “Bit 0” in “PRR – Power Reduction Register” on page 38.
15. Added footnote to Table 8-3 on page 46.
16. Updated Table 10-5 on page 63.
17. Deleted “Bits 7, 2” in “MCUCR – MCU Control Register” on page 64.
18. Updated and moved section “Timer/Counter0 Prescaler and Clock Sources”, now located on page 66.
19. Updated “Timer/Counter1 Initialization for Asynchronous Mode” on page 86.
20. Updated bit description in “PLLCSR – PLL Control and Status Register” on page 94 and “PLLCSR – PLL Control and Status Register” on page 103.
21. Added recommended maximum frequency in “Prescaling and Conversion Timing” on page 125.
22. Updated Figure 17-8 on page 129 .
23. Updated “Temperature Measurement” on page 133.
24. Updated Table 17-3 on page 134.
25. Updated bit R/W descriptions in:
 - “TIMSK – Timer/Counter Interrupt Mask Register” on page 81,
 - “TIFR – Timer/Counter Interrupt Flag Register” on page 81,
 - “TIMSK – Timer/Counter Interrupt Mask Register” on page 92,
 - “TIFR – Timer/Counter Interrupt Flag Register” on page 93,
 - “PLLCSR – PLL Control and Status Register” on page 94,
 - “TIMSK – Timer/Counter Interrupt Mask Register” on page 102,
 - “TIFR – Timer/Counter Interrupt Flag Register” on page 103,
 - “PLLCSR – PLL Control and Status Register” on page 103 and
 - “DIDR0 – Digital Input Disable Register 0” on page 138.
26. Added limitation to “Limitations of debugWIRE” on page 140.
27. Updated “DC Characteristics” on page 161.
28. Updated Table 21-7 on page 166.
29. Updated Figure 21-6 on page 171.
30. Updated Table 21-12 on page 171.
31. Updated Table 22-1 on page 177.
32. Updated Table 22-2 on page 177.
33. Updated Table 22-30, Table 22-31 and Table 22-32, starting on page 188.
34. Updated Table 22-33, Table 22-34 and Table 22-35, starting on page 189.
35. Updated Table 22-39 on page 192.
36. Updated Table 22-46, Table 22-47, Table 22-48 and Table 22-49.

9.9 Rev. 2586I-09/06

1. All Characterization data moved to “Electrical Characteristics” on page 161.
2. All Register Descriptions are gathered up in separate sections in the end of each chapter.
3. Updated Table 11-3 on page 78, Table 11-5 on page 79, Table 11-6 on page 80 and Table 20-4 on page 148.
4. Updated “Calibrated Internal Oscillator” on page 27.
5. Updated Note in Table 7-1 on page 34.
6. Updated “System Control and Reset” on page 39.
7. Updated Register Description in “I/O Ports” on page 53.
8. Updated Features in “USI – Universal Serial Interface” on page 108.
9. Updated Code Example in “SPI Master Operation Example” on page 110 and “SPI Slave Operation Example” on page 111.
10. Updated “Analog Comparator Multiplexed Input” on page 119.
11. Updated Figure 17-1 on page 123.
12. Updated “Signature Bytes” on page 150.
13. Updated “Electrical Characteristics” on page 161.

9.10 Rev. 2586H-06/06

1. Updated “Calibrated Internal Oscillator” on page 27.
2. Updated Table 6.5.1 on page 31.
3. Added Table 21-2 on page 164.

9.11 Rev. 2586G-05/06

1. Updated “Internal PLL for Fast Peripheral Clock Generation - clkPCK” on page 24.
2. Updated “Default Clock Source” on page 30.
3. Updated “Low-Frequency Crystal Oscillator” on page 29.
4. Updated “Calibrated Internal Oscillator” on page 27.
5. Updated “Clock Output Buffer” on page 31.
6. Updated “Power Management and Sleep Modes” on page 34.
7. Added “Software BOD Disable” on page 35.
8. Updated Figure 16-1 on page 119.
9. Updated “Bit 6 – ACBG: Analog Comparator Bandgap Select” on page 120.
10. Added note for Table 17-2 on page 125.
11. Updated “Register Summary” on page 7.

9.12 Rev. 2586F-04/06

1. Updated “Digital Input Enable and Sleep Modes” on page 57.
2. Updated Table 20-16 on page 158.
3. Updated “Ordering Information” on page 11.

9.13 Rev. 2586E-03/06

1. Updated Features in “Analog to Digital Converter” on page 122.
2. Updated Operation in “Analog to Digital Converter” on page 122.
3. Updated Table 17-2 on page 133.
4. Updated Table 17-3 on page 134.
5. Updated “Errata” on page 19.

9.14 Rev. 2586D-02/06

1. Updated Table 6-13 on page 30, Table 6-10 on page 29, Table 6-3 on page 26, Table 6-9 on page 28, Table 6-5 on page 26, Table 9-1 on page 48, Table 17-4 on page 135, Table 20-16 on page 158, Table 21-8 on page 167.
2. Updated “Timer/Counter1 in PWM Mode” on page 86.
3. Updated text “Bit 2 – TOV1: Timer/Counter1 Overflow Flag” on page 93.
4. Updated values in “DC Characteristics” on page 161.
5. Updated “Register Summary” on page 7.
6. Updated “Ordering Information” on page 11.
7. Updated Rev B and C in “Errata ATtiny45” on page 19.
8. All references to power-save mode are removed.
9. Updated Register Addresses.

9.15 Rev. 2586C-06/05

1. Updated “Features” on page 1.
2. Updated Figure 1-1 on page 2.
3. Updated Code Examples on page 18 and page 19.
4. Moved “Temperature Measurement” to Section 17.12 page 133.
5. Updated “Register Summary” on page 7.
6. Updated “Ordering Information” on page 11.

9.16 Rev. 2586B-05/05

1. CLKI added, instances of EEMWE/EEWE renamed EEMPE/EEPE, removed some TBD.
Removed “Preliminary Description” from “Temperature Measurement” on page 133.
2. Updated “Features” on page 1.
3. Updated Figure 1-1 on page 2 and Figure 8-1 on page 39.
4. Updated Table 7-2 on page 38, Table 10-4 on page 63, Table 10-5 on page 63
5. Updated “Serial Programming Instruction set” on page 153.
6. Updated SPH register in “Instruction Set Summary” on page 9.
7. Updated “DC Characteristics” on page 161.
8. Updated “Ordering Information” on page 11.
9. Updated “Errata” on page 19.

9.17 Rev. 2586A-02/05

Initial revision.

