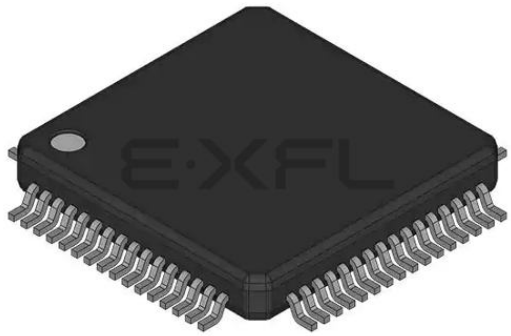

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f82348mlh

- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-port RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses by the core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory
  - Up to 32 KB program/data flash memory
  - Up to 4 KB dual port data/program RAM

1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user-programmable priority levels for each interrupt source: level 0, level 1, level 2
  - Unmaskable level 3 interrupts include illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Interrupt level 3 is highest priority and non-maskable. Its sources include:
    - Illegal instructions
    - Hardware stack overflow
    - SWI instruction
    - EOnce interrupts
    - Misaligned data accesses
  - Lowest-priority software interrupt: level LP
- Support for nested interrupts, so that a higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level is managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6 Peripheral highlights

1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- Up to 100 MHz operation clock with PWM Resolution as fine as 10 ns
- PWM module contains four identical submodules, with two outputs per submodule

1.6.6 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters
- Up to 100 MHz operation clock

1.6.7 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection
- Up to 6.25 Mbit/s baud rate at 100 MHz operation clock

1.6.8 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 12.5 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers
- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.9 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard

1.6.16 General Purpose I/O (GPIO)

- 5 V tolerance
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins (except JTAG and RESETB) default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block diagrams

The 56800EX core is based on a modified dual Harvard-style architecture, consisting of three execution units operating in parallel, and allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set enable straightforward generation of efficient and compact code for the DSP and control functions. The instruction set is also efficient for C compilers, to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 shows how the 56800EX system buses communicate with internal memories, and the IPBus interface and the internal connections among the units of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device’s Reference Manual for details.

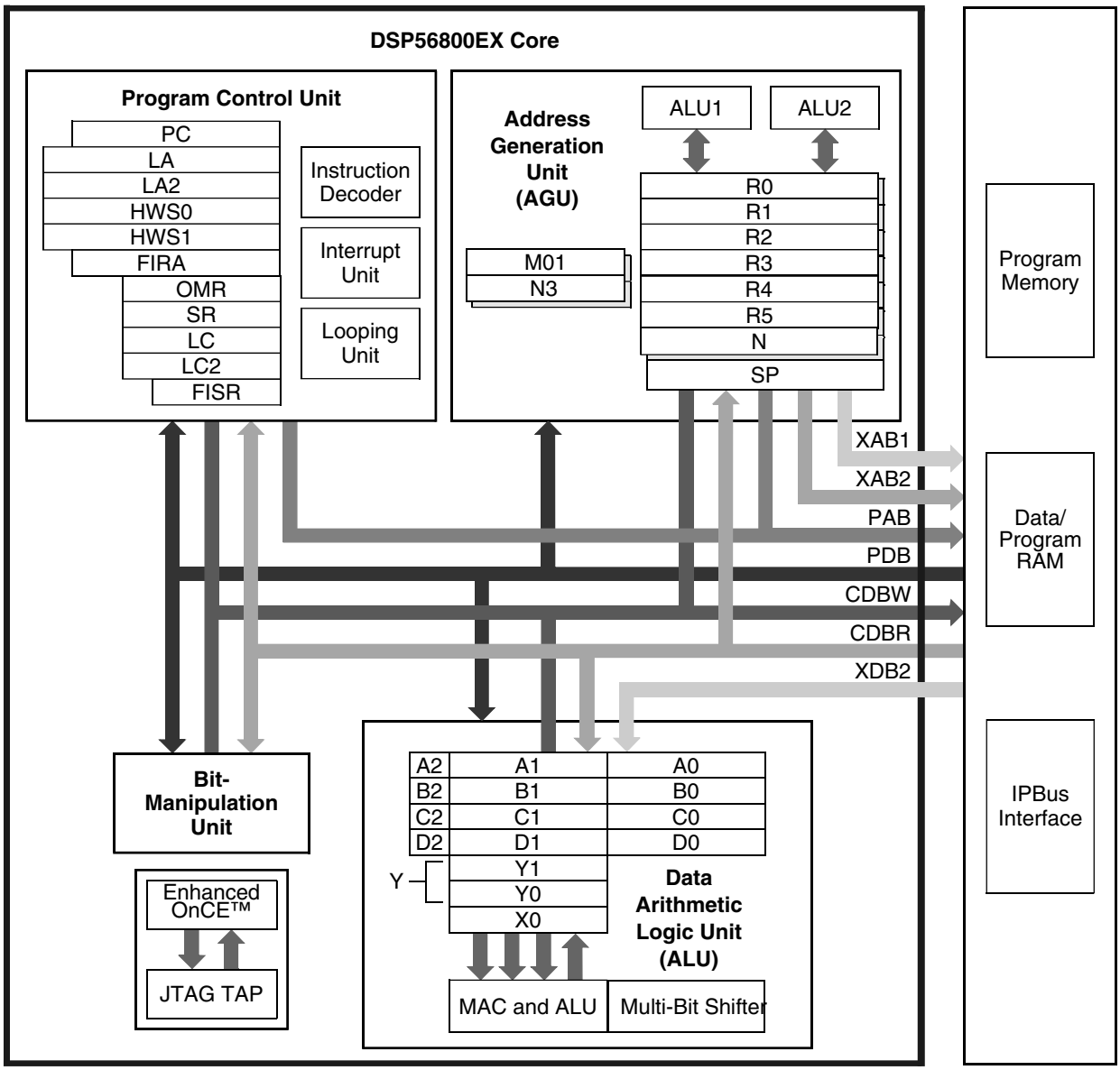


Figure 1. 56800EX basic block diagram

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
TMS	63	Input	Input, internal pullup enabled	Test Mode Select Input — It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TMS. **NOTE:** Always tie the TMS pin to V_{DD} through a 2.2 kΩ resistor if need to keep on-board debug capability. Otherwise, directly tie to V_{DD}.
(GPIOD3)		Input/ Output		GPIO Port D3
$\overline{\text{RESET}}$ or RESETB	2	Input	Input, internal pullup enabled	Reset — A direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. After reset, the default state is $\overline{\text{RESET}}$. Recommended a capacitor of up to 0.1 µF for filtering noise.
(GPIOD4)		Input/ Opendrain Output		GPIO Port D4 $\overline{\text{RESET}}$ functionality is disabled in this mode and the device can be reset only through POR, COP reset, or software reset.
GPIOA0	13	Input/ Output	Input, internal pullup enabled	GPIO Port A0
(ANA0&CMPA_IN3)		Input		ANA0 is analog input to channel 0 of ADCA; CMPA_IN3 is positive input 3 of analog comparator A. After reset, the default state is GPIOA0.
(CMPC_O)		Output		Analog comparator C output
GPIOA1	14	Input/ Output	Input, internal pullup enabled	GPIO Port A1: After reset, the default state is GPIOA1.
(ANA1&CMPA_IN0)		Input		ANA1 is analog input to channel 1 of ADCA; CMPA_IN0 is negative input 0 of analog comparator A. When used as an analog input, the signal goes to ANA1 and CMPA_IN0. The ADC control register configures this input as ANA1 or CMPA_IN0.
GPIOA2	15	Input/ Output	Input, internal pullup enabled	GPIO Port A2: After reset, the default state is GPIOA2.
(ANA2&VREFHA&CMPA_IN1)		Input		ANA2 is analog input to channel 2 of ADCA; VREFHA is analog reference high of ADCA; CMPA_IN1 is negative input 1 of analog comparator A. When used as an analog input, the signal goes to both ANA2, VREFHA, and CMPA_IN1.
GPIOA3	16	Input/ Output	Input, internal pullup enabled	GPIO Port A3: After reset, the default state is GPIOA3.
(ANA3&VREFLA&CMPA_IN2)		Input		ANA3 is analog input to channel 3 of ADCA; VREFLA is analog reference low of ADCA; CMPA_IN2 is negative input 2 of analog comparator A.
GPIOA4	12	Input/ Output	Input, internal pullup enabled	GPIO Port A4: After reset, the default state is GPIOA4.
(ANA4&CMPD_IN0)		Input		ANA4 is Analog input to channel 4 of ADCA; CMPD_IN0 is input 0 to comparator D.

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
GPIOA5	11	Input/ Output	Input, internal pullup enabled	GPIO Port A5: After reset, the default state is GPIOA5.
(ANA5&CMPD_IN1)		Input		ANA5 is analog input to channel 5 of ADCA; ANC9 is analog input to channel 9 of ADCC; CMPD_IN1 is negative input 1 of analog comparator D.
GPIOA6	10	Input/ Output	Input, internal pullup enabled	GPIO Port A6: After reset, the default state is GPIOA6.
(ANA6&CMPD_IN2)		Input		ANA6 is analog input to channel 5 of ADCA; CMPD_IN2 is negative input 2 of analog comparator D.
GPIOA7	9	Input/ Output	Input, internal pullup enabled	GPIO Port A7: After reset, the default state is GPIOA7.
(ANA7&CMPD_IN3)		Input		ANA7 is analog input to channel 7 of ADCA; CMPD_IN3 is negative input 3 of analog comparator D.
GPIOB0	24	Input/ Output	Input, internal pullup enabled	GPIO Port B0: After reset, the default state is GPIOB0.
(ANB0&CMPB_IN3)		Input		ANB0 is analog input to channel 0 of ADCB; CMPB_IN3 is positive input 3 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_IN3. The ADC control register configures this input as ANB0.
GPIOB1	25	Input/ Output	Input, internal pullup enabled	GPIO Port B1: After reset, the default state is GPIOB1.
(ANB1&CMPB_IN0)		Input		ANB1 is analog input to channel 1 of ADCB; CMPB_IN0 is negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_IN0. The ADC control register configures this input as ANB1.
GPIOB2	27	Input/ Output	Input, internal pullup enabled	GPIO Port B2: After reset, the default state is GPIOB2.
(ANB2&VERFHB&CMPC_IN3)		Input		ANB2 is analog input to channel 2 of ADCB; VREFHB is analog reference high of ADCB; CMPC_IN3 is positive input 3 of analog comparator C. When used as an analog input, the signal goes to both ANB2 and CMPC_IN3.
GPIOB3	28	Input/ Output	Input, internal pullup enabled	GPIO Port B3: After reset, the default state is GPIOB3.
(ANB3&VREFLB&CMPC_IN0)		Input		ANB3 is analog input to channel 3 of ADCB; VREFLB is analog reference low of ADCB; CMPC_IN0 is negative input 0 of analog comparator C.
GPIOB4	21	Input/ Output	Input, internal pullup enabled	GPIO Port B4: After reset, the default state is GPIOB4.
(ANB4&CMPC_IN1)		Input		ANB4 is analog input to channel 4 of ADCB; CMPC_IN1 is negative input 1 of analog comparator C.
GPIOB5	20	Input/ Output	Input, internal pullup enabled	GPIO Port B5: After reset, the default state is GPIOB5.
(ANB5&CMPC_IN2)		Input		ANB5 is analog input to channel 5 of ADCB; CMPC_IN2 is negative input 2 of analog comparator C.

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
GPIOB6	19	Input/ Output	Input, internal pullup enabled	GPIO Port B6: After reset, the default state is GPIOB6.
(ANB6&CMPB_IN1)		Input		ANB6 is analog input to channel 6 of ADCB; CMPB_IN1 is negative input 1 of analog comparator B.
GPIOB7	17	Input/ Output	Input, internal pullup enabled	GPIO Port B7: After reset, the default state is GPIOB7.
(ANB7&CMPB_IN2)		Input		ANB7 is analog input to channel 7 of ADCB; CMPB_IN2 is negative input 2 of analog comparator B.
GPIOC0	3	Input/ Output	Input, internal pullup enabled	GPIO Port C0: After reset, the default state is GPIOC0.
(EXTAL)		Analog Input		The external crystal oscillator input (EXTAL) connects the internal crystal oscillator input to an external crystal or ceramic resonator.
(CLKIN0)		Input		External clock input 0[1]
GPIOC1	4	Input/ Output	Input, internal pullup enabled	GPIO Port C1: After reset, the default state is GPIOC1.
(XTAL)		Input		The external crystal oscillator output (XTAL) connects the internal crystal oscillator output to an external crystal or ceramic resonator.
GPIOC2	5	Input/ Output	Input, internal pullup enabled	GPIO Port C2: After reset, the default state is GPIOC2.
(TXD0)		Output		SCI0 transmit data output or transmit/receive in single wire operation
(XB_OUT11)		Output		Crossbar module output 11
(XB_IN2)		Input		Crossbar module input 2
(CLKO0)		Output		Buffered clock output 0: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
GPIOC3	7	Input/ Output	Input, internal pullup enabled	GPIO Port C3: After reset, the default state is GPIOC3.
(TA0)		Input/ Output		Quad timer module A channel 0 input/output
(CMPA_O)		Output		Analog comparator A output
(RXD0)		Input		SCI0 receive data input
(CLKIN1)		Input		External clock input 1
GPIOC4	8	Input/ Output	Input, internal pullup enabled	GPIO Port C4: After reset, the default state is GPIOC4.
(TA1)		Input/ Output		Quad timer module A channel 1 input/output
(CMPB_O)		Output		Analog comparator B output
(XB_IN6)		Input		Crossbar module input 6
(EWM_OUT_B)		Output		External Watchdog Module output
GPIOC5	18	Input/ Output	Input, internal pullup enabled	GPIO Port C5: After reset, the default state is GPIOC5.
(DACA_O)		Analog Output		12-bit digital-to-analog output
(XB_IN7)		Input		Crossbar module input 7

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
GPIOF2	39	Input/ Output	Input, internal pullup enabled	GPIO Port F2: After reset, the default state is GPIOF2.
(SCL0)		Input/ Open-drain Output		I^2C0 serial clock
(XB_OUT6)		Output		Crossbar module output 6
(MISO1)		Input/ Output		Master in/slave out for SPI1 —In master mode, MISO1 pin is the data input. In slave mode, MISO1 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
GPIOF3	40	Input/ Output	Input, internal pullup enabled	GPIO Port F3: After reset, the default state is GPIOF3.
(SDA0)		Input/ Open-drain Output		I^2C0 serial data line
(XB_OUT7)		Output		Crossbar module output 7
(MOSI1)		Input/ Output		Master out/slave in for SPI1— In master mode, MOSI1 pin is the data output. In slave mode, MOSI1 pin is the data input.
GPIOF4	41	Input/ Output	Input, internal pullup enabled	GPIO Port F4: After reset, the default state is GPIOF4.
(TXD1)		Output		SCI1 transmit data output or transmit/receive in single wire operation
(XB_OUT8)		Output		Crossbar module output 8
(PWMA_0X)		Input/ Output		PWM module A (NanoEdge), submodule 0, output X or input capture X
(PWMA_FAULT 6)		Input		Disable PWMA output 6
GPIOF5	42	Input/ Output	Input, internal pullup enabled	GPIO Port F5: After reset, the default state is GPIOF5.
(RXD1)		Input		SCI1 receive data input
(XB_OUT9)		Output		Crossbar module output 9
(PWMA_1X)		Input/ Output		PWM module A (NanoEdge), submodule 1, output X or input capture X
(PWMA_FAULT 7)		Input		Disable PWMA output 7
GPIOF6	58	Input/ Output	Input, internal pullup enabled	GPIO Port F6: After reset, the default state is GPIOF6.
(PWMA_3X)		Input/ Output		PWM module A (NanoEdge), submodule 3, output X or input capture X
(XB_IN2)		Input		Crossbar module input 2

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	64 LQFP	Type	State During Reset	Signal Description
GPIOF7	59	Input/ Output	Input, internal pullup enabled	GPIO Port F7: After reset, the default state is GPIOF7.
(CMPC_O)		Output		Analog comparator C output
(SS1_B)		Input/ Output		In slave mode, SS1_B indicates to the SPI1 module that the current transfer is to be received.
(XB_IN3)		Input		Crossbar module input 3
GPIOF8	6	Input/ Output	Input, internal pullup enabled	GPIO Port F8: After reset, the default state is GPIOF8.
(RXD0)		Input		SCI0 receive data input
(XB_OUT10)		Output		Crossbar module output 10
(CMPD_O)		Output		Analog comparator D output
(PWMA_2X)				PWM module A (NanoEdge), submodule 2, output X or input capture X

1. If CLKIN is selected as the device's external clock input, then both the GPS_C0 bit (in GPS1) and the EXT_SEL bit (in OCCS oscillator control register (OSCTL)) must be set. Also, the crystal oscillator should be powered down.

3 Signal groups

The input and output signals of the MC56F82348MLH are organized into functional groups, as detailed in Table 3.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins in 64LQFP
Power Inputs (V_{DD}, V_{DDA}), Power output(V_{CAP})	6
Ground (V_{SS}, V_{SSA})	4
Reset	1
eFlexPWM with NanoEdge ports not including fault pins (for 56F827xx)	8
eFlexPWM without NanoEdge ports not including fault pins	4
Queued Serial Peripheral Interface (QSPI0 and QSPI1) ports	9
Queued Serial Communications Interface (QSCI0 and QSCI1) ports	10
Inter-Integrated Circuit Interface (I^2C0) ports	6
12-bit Analog-to-Digital Converter inputs	16
Analog Comparator inputs/outputs	17/5
12-bit Digital-to-Analog output	2
Quad Timer Module (TMRA and TMRB) ports	4
Controller Area Network (MSCAN)	2

Table continues on the next page...

Field	Description	Values
Q	Qualification status	• MC = Fully qualified, general market flow • PC = Prequalification
56F8	DSC family with flash memory and DSP56800/ DSP56800E/DSP56800EX core	• 56F8
2	DSC subfamily	• 2
C	Maximum CPU frequency (MHz)	• 3 = 50 MHz
F	Primary program flash memory size	• 4 = 64 KB
P	Pin count	• 8 = 64
T	Temperature range (°C)	• M = –40 to 125
PP	Package identifier	• LH = 64LQFP
N	Packaging type	• R = Tape and reel • (Blank) = Trays

6 Terminology and guidelines

6.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

6.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

6.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

6.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

6.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

6.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

6.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

6.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

7.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed as per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 4. ESD/Latch-up Protection

Characteristic[1]	Min	Max	Unit
ESD for Human Body Model (HBM)	–2000	+2000	V
ESD for Machine Model (MM)	–200	+200	V
ESD for Charge Device Model (CDM)	–500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	–100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

7.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 5 may affect device reliability or cause permanent damage to the device.

Table 5. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		-0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.3	0.3	V

Table continues on the next page...

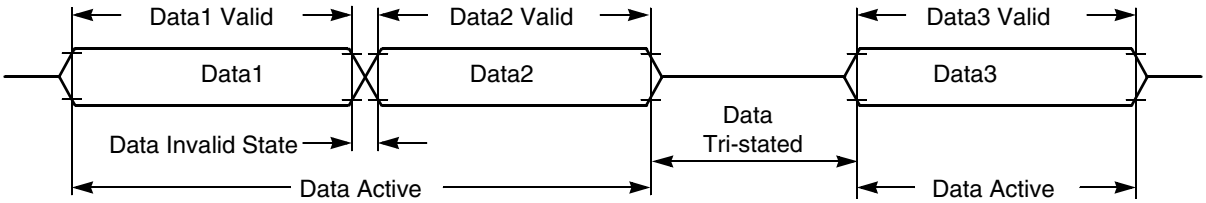


Figure 4. Signal states

8.3 Nonswitching electrical specifications

8.3.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 6. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
Supply voltage[2]	V_{DD}, V_{DDA}		2.7	3.3	3.6	V
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}		V_{DDA}-0.6		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔVDD		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔVSS		-0.1	0	0.1	V
Input Voltage High (digital inputs)	V_{IH}	Pin Group 1	0.7 x V_{DD}		5.5	V
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	Pin Group 2	0.7 x V_{DD}	—	V_{DD}	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.35 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	Pin Group 1 Pin Group 1	— —		-2 -9	mA
Output Source Current Low (at V_{OL} max.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	Pin Groups 1, 2 Pin Groups 1, 2	— —		2 9	mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output

Table 8. DC Electrical Characteristics at Recommended Operating Conditions (continued)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit	Test Conditions
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40mV	—	Typically V_{DDA} - 40mV	V	R_{LD} = 3 kΩ || C_{LD} = 400 pF
Output Current[1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 1	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	0.06 x V_{DD}	—	—	V	—

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC

8.3.4 Power mode transition operating behaviors

Parameters listed are guaranteed by design.

NOTE

All address and data buses described here are internal.

Table 9. Reset, stop, wait, and interrupt timing

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16[1]	—	ns	—
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	865 x T_{OSC} + 8 x T		ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	361.3	570.9	ns	—

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns. Recommended a capacitor of up to 0.1 µF on $\overline{\text{RESET}}$.

NOTE

In Table 9, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 50MHz, T=20 ns. At 4 MHz (used coming out of reset and stop modes), T=250 ns.

Board type	Symbol	Description	64 LQFP	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

9 Peripheral operating requirements and behaviors

9.1 Core modules

9.1.1 JTAG timing

Table 16. JTAG timing

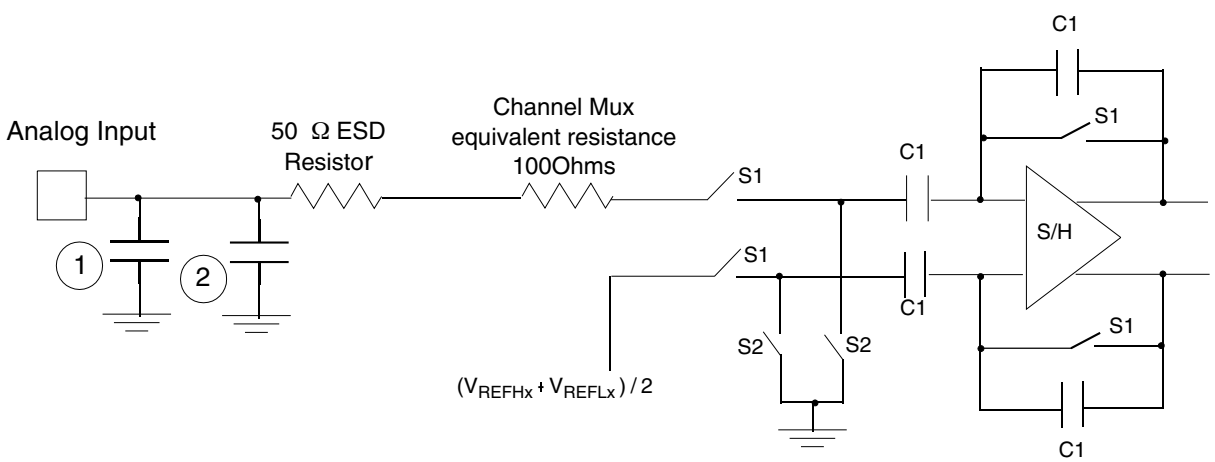
Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation	f_{OP}	DC	SYS_CLK/8	MHz	Figure 5
TCK clock pulse width	t_{PW}	50	—	ns	Figure 5
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 6
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 6
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 6
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 6

2. ADC clock duty cycle is 45% ~ 55%
3. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
4. In unipolar mode, positive input must be ensured to be always greater than negative input.
5. First conversion takes 10 clock cycles.
6. INL/DNL is measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$ using Histogram method at x1 gain setting
7. Least Significant Bit = 0.806 mV at 3.3 V V_{DDA}, x1 gain Setting
8. Offset measured at 2048 code
9. Measured converting a 1 kHz input full scale sine wave
10. When code runs from internal RAM
11. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC
12. Any off-channel with 50 kHz full-scale input to the channel being sampled with DC input (isolation crosstalk)
13. From a previously sampled channel with 50 kHz full-scale input to the channel being sampled with DC input (memory crosstalk).

9.5.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 are dependent on the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 4.8 \times 10^{-12}} + 100\ ohm + 50\ ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. S1 and S2 switch phases are non-overlapping and depend on the ADC clock frequency

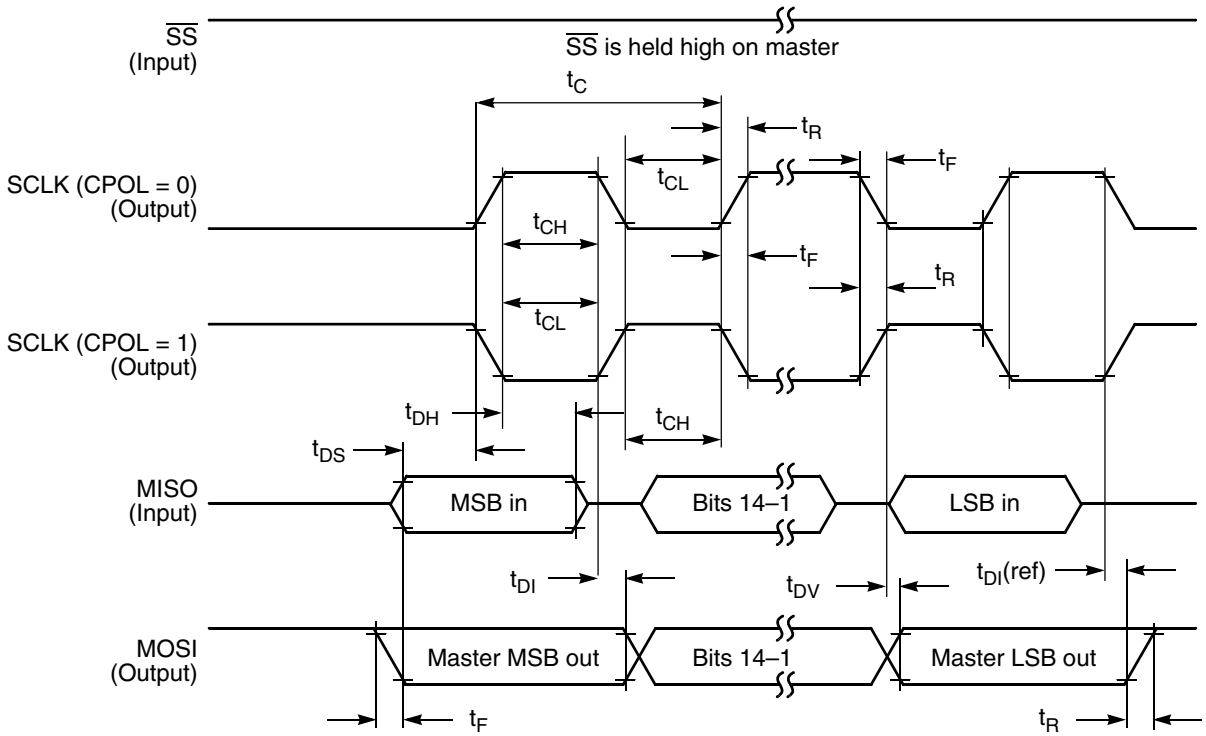


Figure 13. SPI master timing (CPHA = 0)

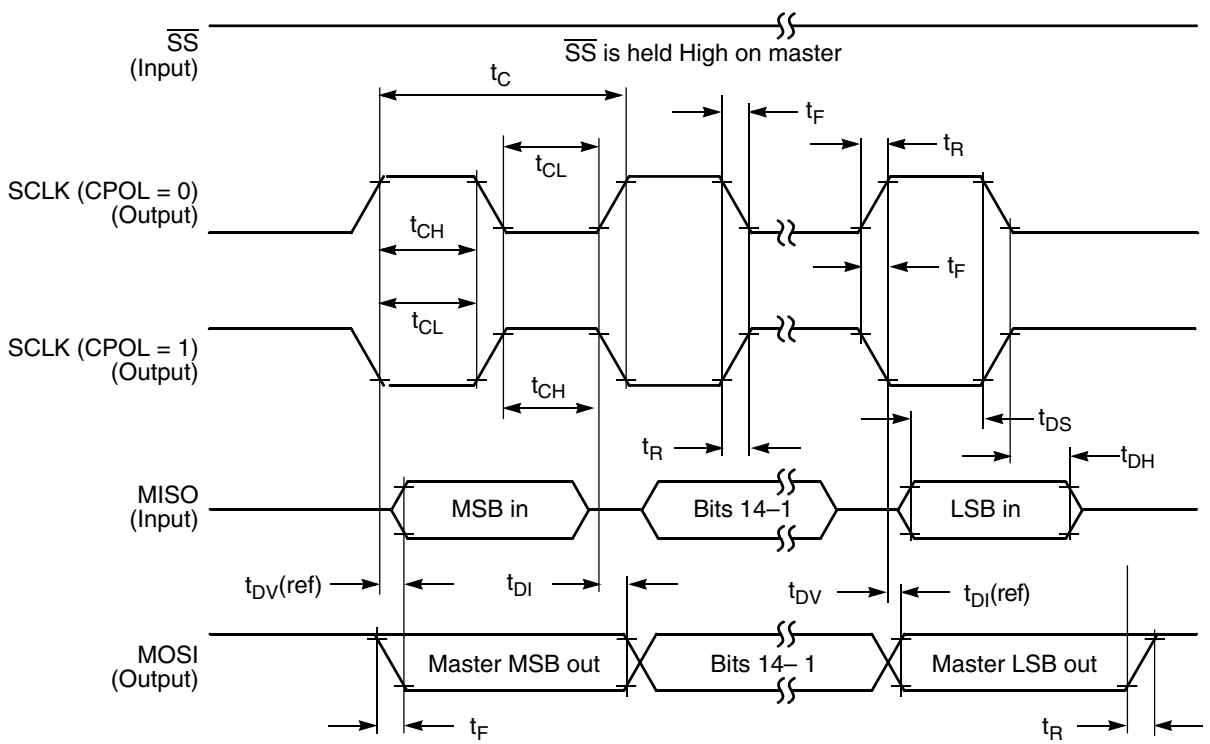


Figure 14. SPI master timing (CPHA = 1)

9.7.2 Queued Serial Communication Interface (SCI) timing

Parameters listed are guaranteed by design.

Table 32. SCI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud rate[1]	BR	—	(f_{MAX}/16)	Mbit/s	—
RXD pulse width	RXD_{PW}	0.965/BR	1.04/BR	ns	Figure 17
TXD pulse width	TXD_{PW}	0.965/BR	1.04/BR	ns	Figure 18
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1. f_{MAX} is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max.)50 MHz.

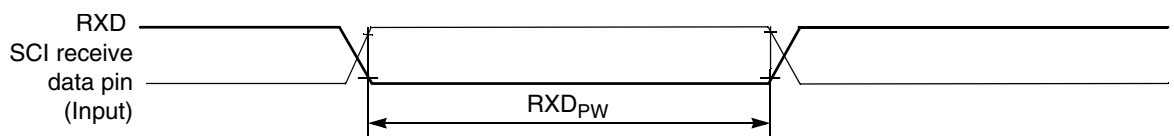


Figure 17. RXD pulse width

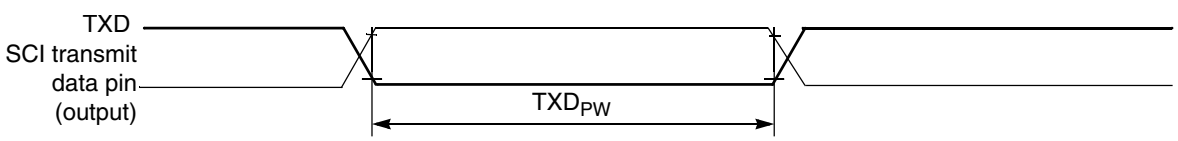


Figure 18. TXD pulse width

9.7.3 Modular/Scalable Controller Area Network (MSCAN)

Table 33. MSCAN Timing Parameters

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbit/s
CAN Wakeup dominant pulse filtered	T_{WAKEUP}	—	1.5	µs
CAN Wakeup dominant pulse pass	T_{WAKEUP}	5	—	µs

64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
46	GPIOE1	GPIOE1	PWM_0A			
47	GPIOE2	GPIOE2	PWM_1B			
48	GPIOE3	GPIOE3	PWM_1A			
49	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
50	GPIOF1	GPIOF1	CLKO1	XB_IN7		
51	GPIOE4	GPIOE4	PWM_2B	XB_IN2		
52	GPIOE5	GPIOE5	PWM_2A	XB_IN3		
53	GPIOE6	GPIOE6	PWM_3B	XB_IN4		
54	GPIOE7	GPIOE7	PWM_3A	XB_IN5		
55	GPIOC14	GPIOC14	SDA0	XB_OUT4	PWM_FAULT4	
56	GPIOC15	GPIOC15	SCL0	XB_OUT5	PWM_FAULT5	
57	VCAP	VCAP				
58	GPIOF6	GPIOF6		PWM_3X		XB_IN2
59	GPIOF7	GPIOF7		CMPC_O		XB_IN3
60	VDD	VDD				
61	VSS	VSS				
62	TDO	TDO	GPIOD1			
63	TMS	TMS	GPIOD3			
64	TDI	TDI	GPIOD0			

12.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

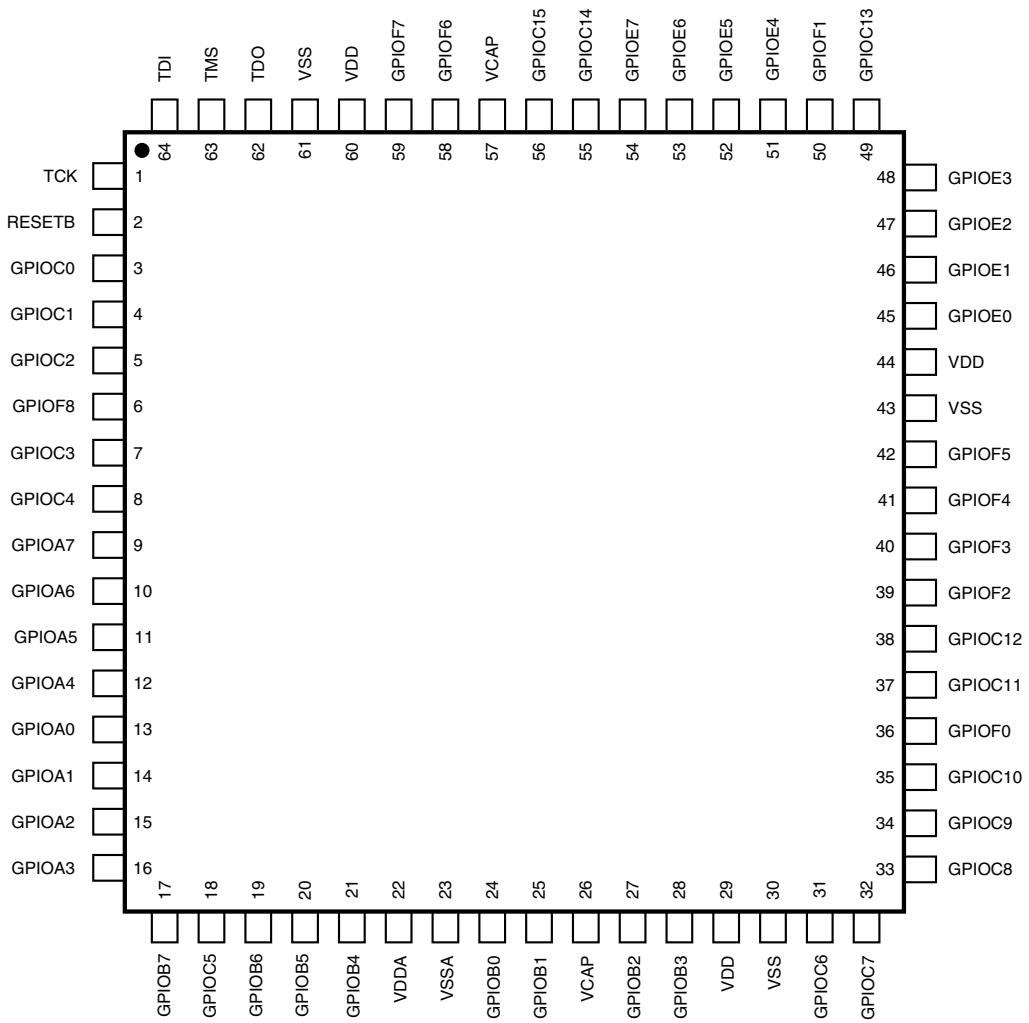


Figure 21. 64-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

13 Product documentation

The documents listed in Table 35 are required for a complete description and proper design with the device. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, or online at **freescale.com**.

Table 35. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
Reference Manual	Detailed functional description and programming model	MC56F827XXRM

Table continues on the next page...