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What is "<u>Embedded - Microcontrollers</u>"?

"<u>Embedded - Microcontrollers</u>" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
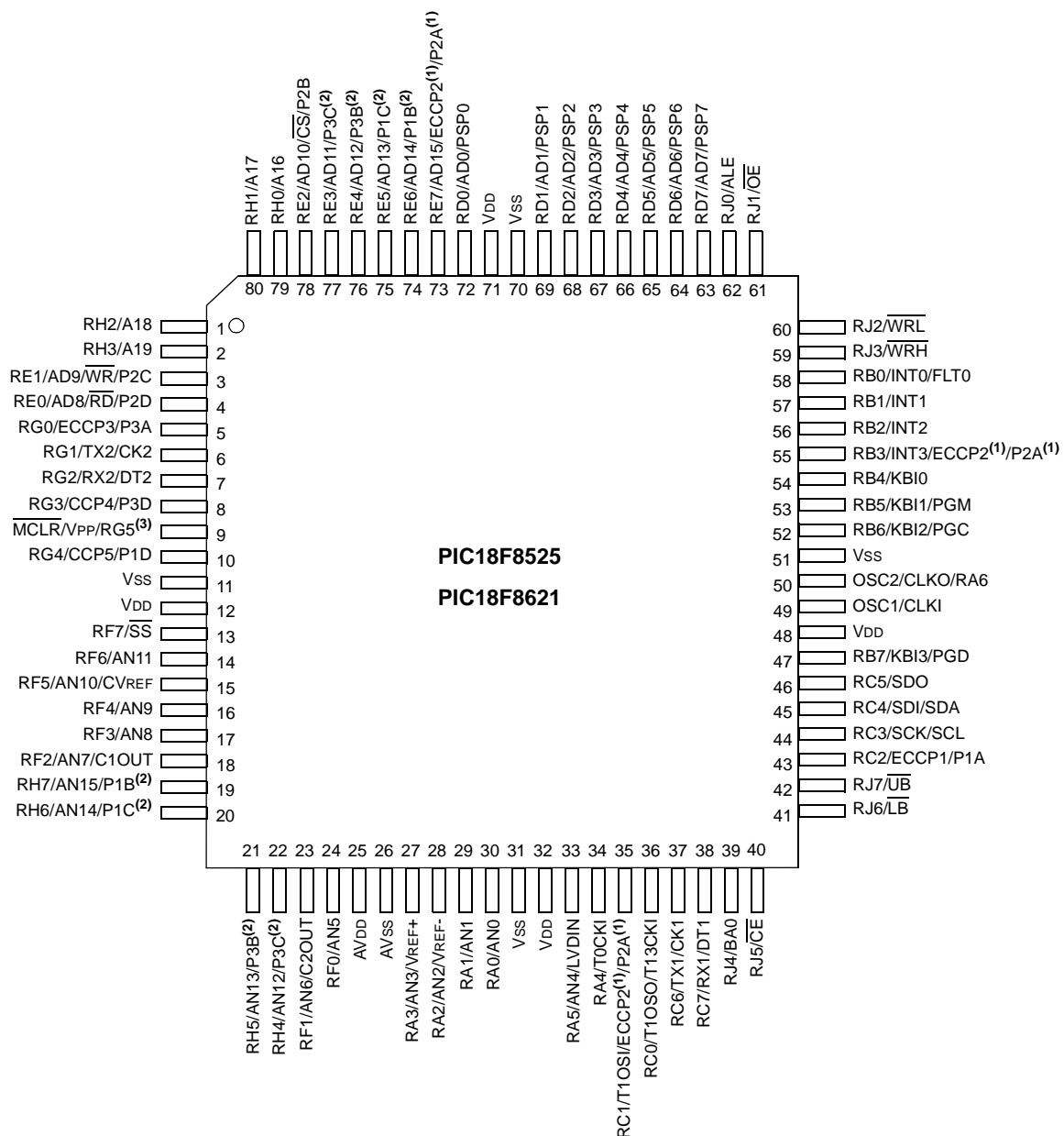
Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.75K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f8621-e-pt

Pin Diagrams (Cont.'d)

80-Pin TQFP

PIC18F8525
PIC18F8621

Top pins (80–61):
RH1/A17 (80), RH0/A16 (79), RE2/AD10/$\overline{CS}$/P2B (78), RE3/AD11/P3C[2] (77), RE4/AD12/P3B[2] (76), RE5/AD13/P1C[2] (75), RE6/AD14/P1B[2] (74), RE7/AD15/ECCP2[1]/P2A[1] (73), RD0/AD0/PSP0 (72), VDD (71), VSS (70), RD1/AD1/PSP1 (69), RD2/AD2/PSP2 (68), RD3/AD3/PSP3 (67), RD4/AD4/PSP4 (66), RD5/AD5/PSP5 (65), RD6/AD6/PSP6 (64), RD7/AD7/PSP7 (63), RJ0/ALE (62), RJ1/$\overline{OE}$ (61)

Left pins (1–20):
RH2/A18 (1), RH3/A19 (2), RE1/AD9/$\overline{WR}$/P2C (3), RE0/AD8/$\overline{RD}$/P2D (4), RG0/ECCP3/P3A (5), RG1/TX2/CK2 (6), RG2/RX2/DT2 (7), RG3/CCP4/P3D (8), $\overline{MCLR}$/VPP/RG5[3] (9), RG4/CCP5/P1D (10), VSS (11), VDD (12), RF7/$\overline{SS}$ (13), RF6/AN11 (14), RF5/AN10/CVREF (15), RF4/AN9 (16), RF3/AN8 (17), RF2/AN7/C1OUT (18), RH7/AN15/P1B[2] (19), RH6/AN14/P1C[2] (20)

Right pins (60–41):
RJ2/$\overline{WRL}$ (60), RJ3/$\overline{WRH}$ (59), RB0/INT0/FLT0 (58), RB1/INT1 (57), RB2/INT2 (56), RB3/INT3/ECCP2[1]/P2A[1] (55), RB4/KBI0 (54), RB5/KBI1/PGM (53), RB6/KBI2/PGC (52), VSS (51), OSC2/CLKO/RA6 (50), OSC1/CLKI (49), VDD (48), RB7/KBI3/PGD (47), RC5/SDO (46), RC4/SDI/SDA (45), RC3/SCK/SCL (44), RC2/ECCP1/P1A (43), RJ7/$\overline{UB}$ (42), RJ6/$\overline{LB}$ (41)

Bottom pins (21–40):
RH5/AN13/P3B[2] (21), RH4/AN12/P3C[2] (22), RF1/AN6/C2OUT (23), RF0/AN5 (24), AVDD (25), AVSS (26), RA3/AN3/VREF+ (27), RA2/AN2/VREF- (28), RA1/AN1 (29), RA0/AN0 (30), VSS (31), VDD (32), RA5/AN4/LVDIN (33), RA4/T0CKI (34), RC1/T1OSI/ECCP2[1]/P2A[1] (35), RC0/T1OSO/T13CKI (36), RC6/TX1/CK1 (37), RC7/RX1/DT1 (38), RJ4/BA0 (39), RJ5/$\overline{CE}$ (40)

Note 1: ECCP2/P2A are multiplexed with RC1 when CCP2MX is set; with RE7 when CCP2MX is cleared and the device is configured in Microcontroller mode; or with RB3 when CCP2MX is cleared in all other program memory modes.

2: P1B/P1C/P3B/P3C are multiplexed with RE6:RE3 when ECCPMX is set and with RH7:RH4 when ECCPMX is not set.

3: RG5 is multiplexed with $\overline{MCLR}$ and is only available when the $\overline{MCLR}$ Resets are disabled.

FIGURE 3-3: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V$_{DD}$ VIA 1 kΩ RESISTOR)
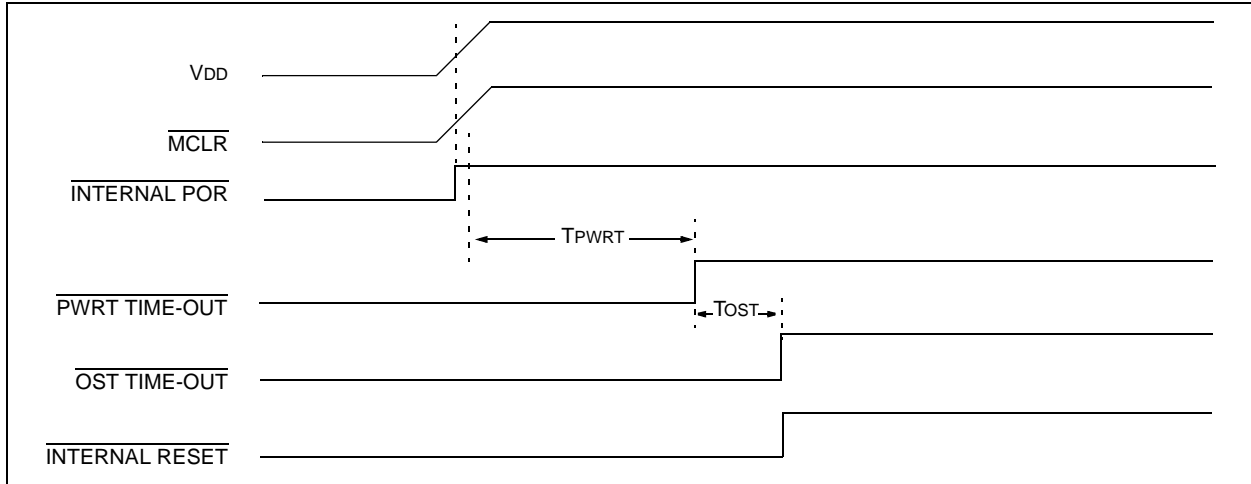

FIGURE 3-4: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V$_{DD}$): CASE 1
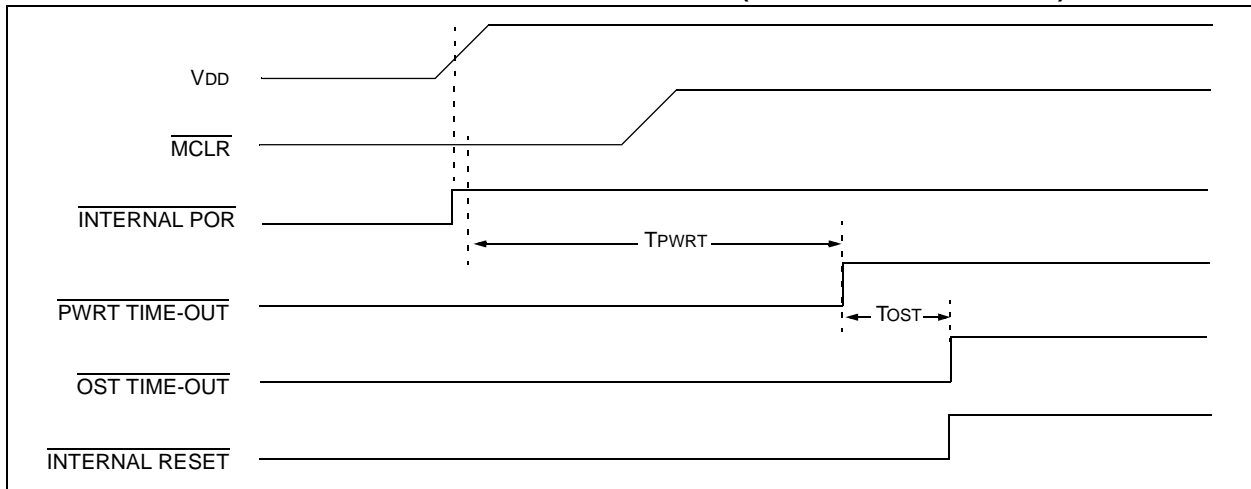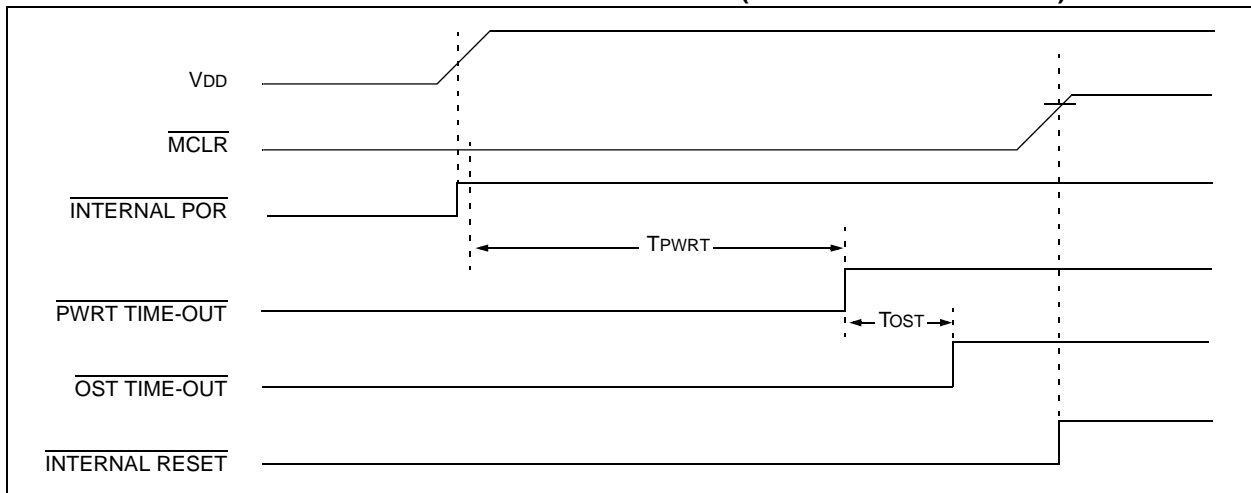

FIGURE 3-5: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V$_{DD}$): CASE 2

4.2 Return Address Stack

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC (Program Counter) is pushed onto the stack when a `CALL` or `RCALL` instruction is executed, or an interrupt is Acknowledged. The PC value is pulled off the stack on a `RETURN`, `RETLW` or a `RETFIE` instruction. PCLATU and PCLATH are not affected by any of the `RETURN` or `CALL` instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit Stack Pointer, with the Stack Pointer initialized to `00000b` after all Resets. There is no RAM associated with Stack Pointer `00000b`. This is only a Reset value. During a `CALL` type instruction causing a push onto the stack, the Stack Pointer is first incremented and the RAM location pointed to by the Stack Pointer is written with the contents of the PC. During a `RETURN` type instruction causing a pop from the stack, the contents of the RAM location pointed to by the STKPTR register are transferred to the PC and then the Stack Pointer is decremented.

The stack space is not part of either program or data space. The Stack Pointer is readable and writable and the address on the top of the stack is readable and writable through SFR registers. Data can also be pushed to, or popped from the stack using the Top-of-Stack SFRs. Status bits indicate if the Stack Pointer is at or beyond the 31 levels provided.

4.2.1 TOP-OF-STACK ACCESS

The top of the stack is readable and writable. Three register locations, TOSU, TOSH and TOSL, hold the contents of the stack location pointed to by the STKPTR register. This allows users to implement a software stack if necessary. After a `CALL,  RCALL` or interrupt, the software can read the pushed value by reading the TOSU, TOSH and TOSL registers. These values can be placed on a user defined software stack. At return time, the software can replace the TOSU, TOSH and TOSL and do a return.

The user must disable the global interrupt enable bits during this time to prevent inadvertent stack operations.

4.2.2 RETURN STACK POINTER (STKPTR)

The STKPTR register contains the Stack Pointer value, the STKFUL (Stack Full) status bit and the STKUNF (Stack Underflow) status bits. Register 4-2 shows the STKPTR register. The value of the Stack Pointer can be 0 through 31. The Stack Pointer increments when values are pushed onto the stack and decrements when values are popped off the stack. At Reset, the Stack Pointer value will be '0'. The user may read and write the Stack Pointer value. This feature can be used by a real-time operating system for return stack maintenance.

After the PC is pushed onto the stack 31 times (without popping any values off the stack), the STKFUL bit is set. The STKFUL bit can only be cleared in software or by a POR.

The action that takes place when the stack becomes full depends on the state of the STVREN (Stack Overflow Reset Enable) configuration bit. Refer to **Section 25.0 "Instruction Set Summary"** for a description of the device configuration bits. If STVREN is set (default), the 31st push will push the (PC + 2) value onto the stack, set the STKFUL bit and reset the device. The STKFUL bit will remain set and the Stack Pointer will be set to '0'.

If STVREN is cleared, the STKFUL bit will be set on the 31st push and the Stack Pointer will increment to 31. Any additional pushes will not overwrite the 31st push and STKPTR will remain at 31.

When the stack has been popped enough times to unload the stack, the next pop will return a value of zero to the PC and sets the STKUNF bit, while the Stack Pointer remains at '0'. The STKUNF bit will remain set until cleared in software or a POR occurs.

Note:	Returning a value of zero to the PC on an underflow has the effect of vectoring the program to the Reset vector, where the stack conditions can be verified and appropriate actions can be taken.

REGISTER 4-2: **STKPTR: STACK POINTER REGISTER**

| R/C-0	R/C-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STKFUL[(1)]	STKUNF[(1)]	—	SP4	SP3	SP2	SP1	SP0
bit 7							bit 0

bit 7 **STKFUL:** Stack Full Flag bit[(1)]

1 = Stack became full or overflowed
0 = Stack has not become full or overflowed

bit 6 **STKUNF:** Stack Underflow Flag bit[(1)]

1 = Stack underflow occurred
0 = Stack underflow did not occur

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **SP4:SP0:** Stack Pointer Location bits

> **Note 1:** Bit 7 and bit 6 can only be cleared in user software or by a POR.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

FIGURE 4-4: **RETURN ADDRESS STACK AND ASSOCIATED REGISTERS**
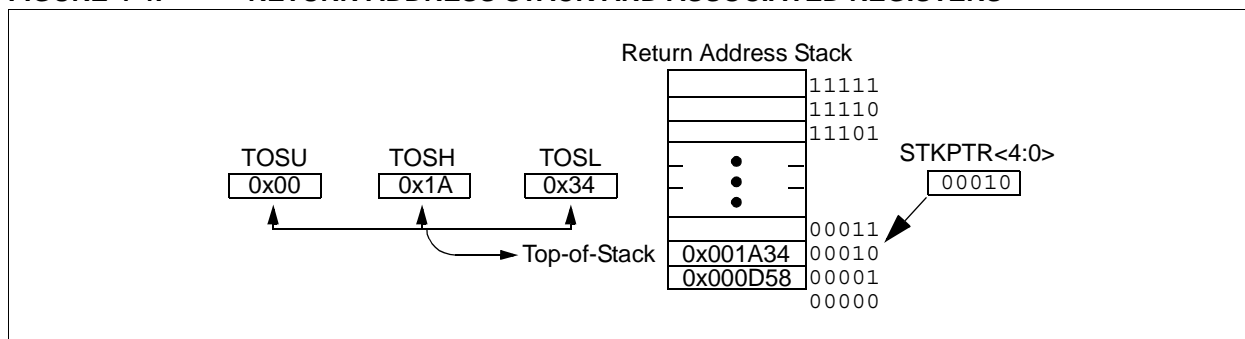
4.2.3 PUSH AND POP INSTRUCTIONS

Since the Top-of-Stack (TOS) is readable and writable, the ability to push values onto the stack and pull values off the stack, without disturbing normal program execution, is a desirable option. To push the current PC value onto the stack, a PUSH instruction can be executed. This will increment the Stack Pointer and load the current PC value onto the stack. TOSU, TOSH and TOSL can then be modified to place a return address on the stack.

The ability to pull the TOS value off of the stack and replace it with the value that was previously pushed onto the stack, without disturbing normal execution, is achieved by using the POP instruction. The POP instruction discards the current TOS by decrementing the Stack Pointer. The previous value pushed onto the stack then becomes the TOS value.

4.2.4 STACK FULL/UNDERFLOW RESETS

These Resets are enabled by programming the STVREN configuration bit. When the STVREN bit is disabled, a full or underflow condition will set the appropriate STKFUL or STKUNF bit, but not cause a device Reset. When the STVREN bit is enabled, a full or underflow condition will set the appropriate STKFUL or STKUNF bit and then cause a device Reset. The STKFUL or STKUNF bits are only cleared by the user software or a Power-on Reset.

FIGURE 6-6: **EXTERNAL MEMORY BUS TIMING FOR SLEEP (MICROPROCESSOR MODE)**

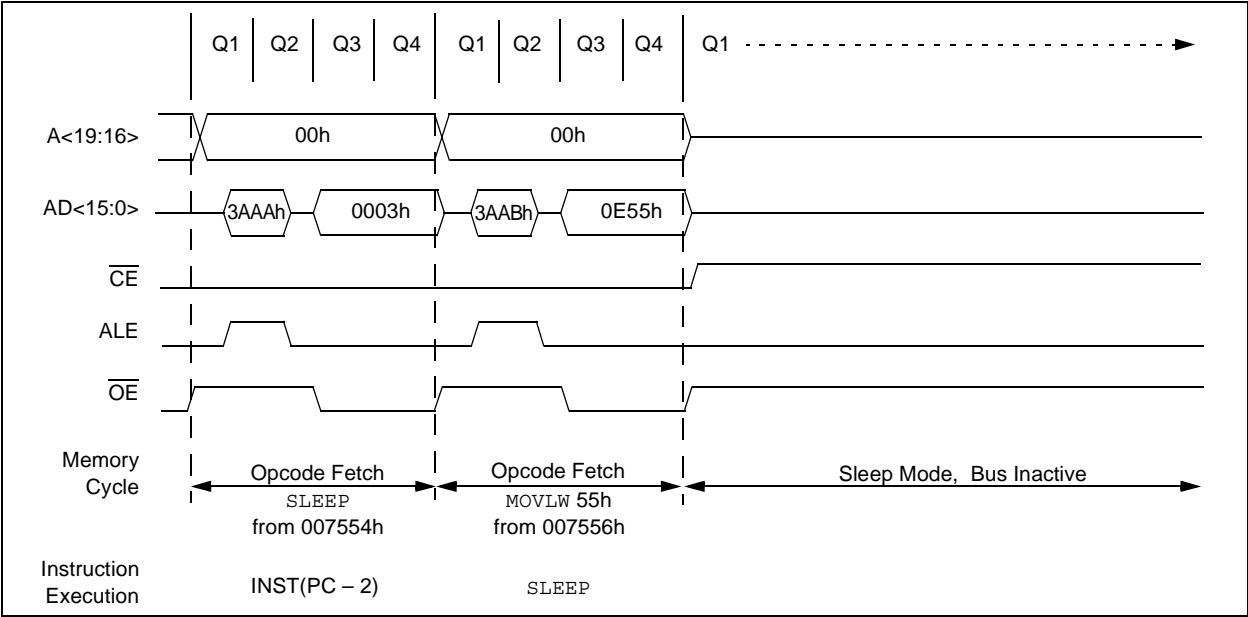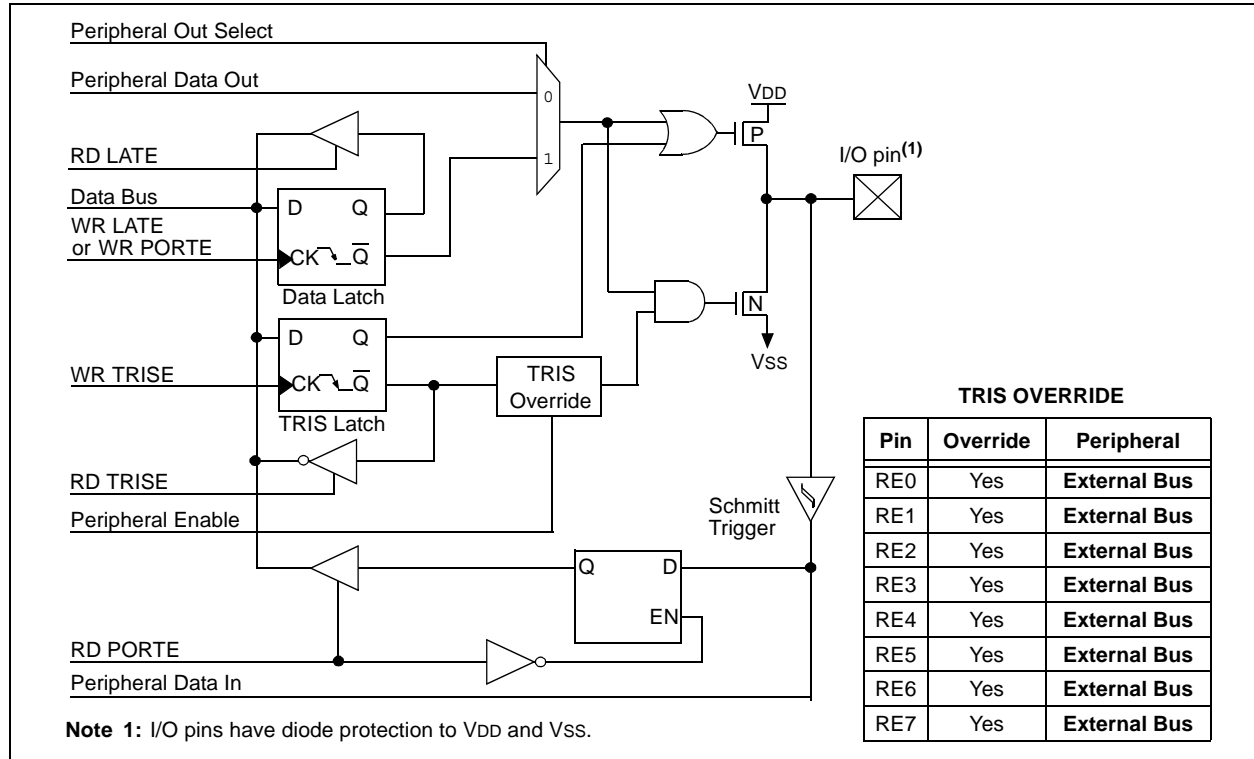**FIGURE 10-11:** **PORTE BLOCK DIAGRAM IN I/O MODE**

TRIS OVERRIDE

Pin	Override	Peripheral
RE0	Yes	**External Bus**
RE1	Yes	**External Bus**
RE2	Yes	**External Bus**
RE3	Yes	**External Bus**
RE4	Yes	**External Bus**
RE5	Yes	**External Bus**
RE6	Yes	**External Bus**
RE7	Yes	**External Bus**

Note 1: I/O pins have diode protection to VDD and VSS.

FIGURE 10-12: **PORTE BLOCK DIAGRAM IN SYSTEM BUS MODE**

Note 1: I/O pins have protection diodes to VDD and VSS.
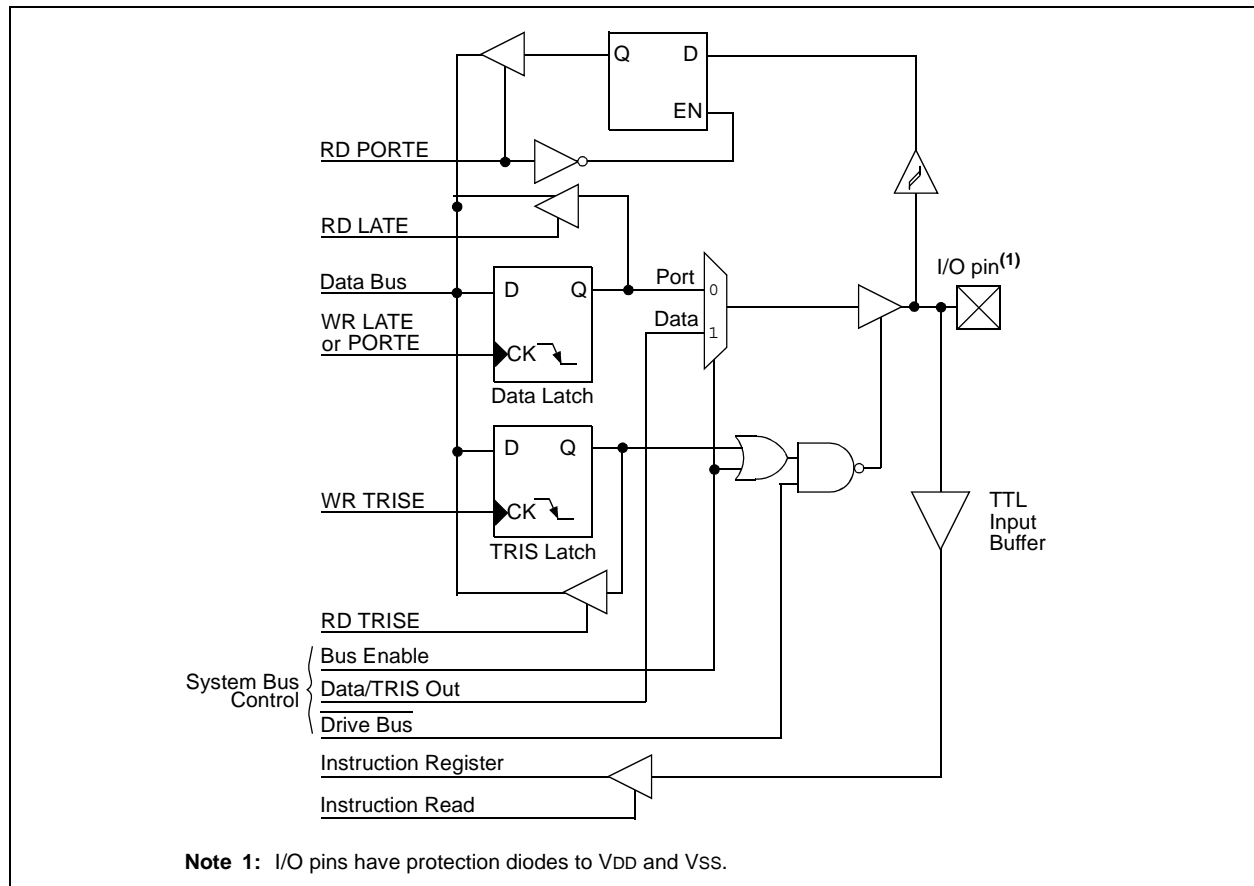
FIGURE 17-8: PWM DIRECTION CHANGE

Note 1: The direction bit in the ECCP1 Control register (CCP1CON<7>) is written any time during the PWM cycle.

2: When changing directions, the P1A and P1C signals switch before the end of the current PWM cycle at intervals of 4 TOSC, 16 TOSC or 64 TOSC, depending on the Timer2 prescaler value. The modulated P1B and P1D signals are inactive at this time.
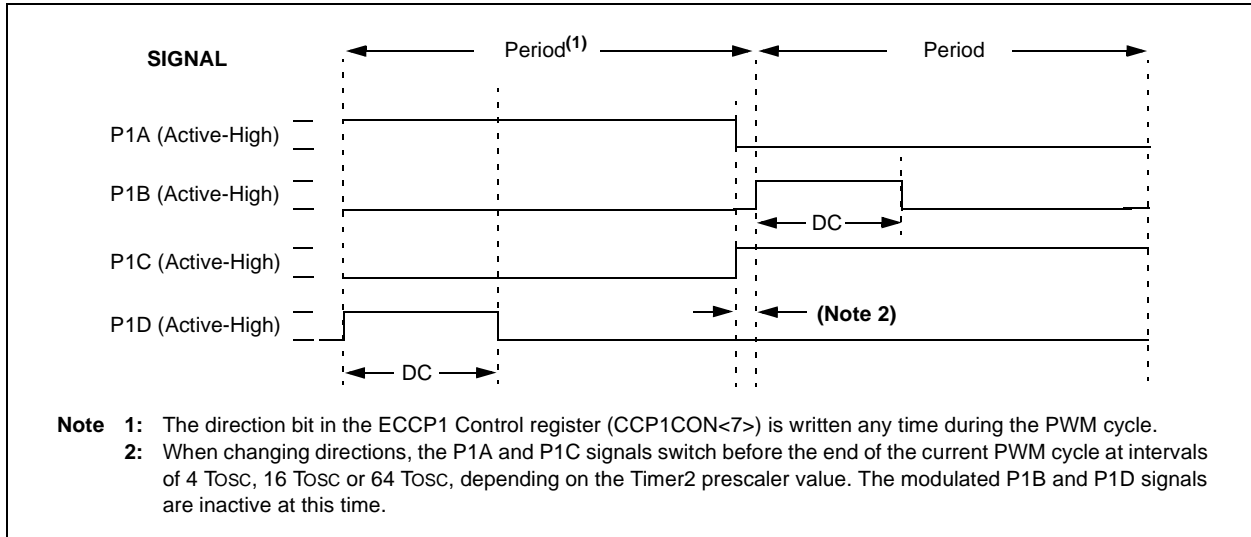
FIGURE 17-9: PWM DIRECTION CHANGE AT NEAR 100% DUTY CYCLE

Note 1: All signals are shown as active-high.

2: t_{ON} is the turn-on delay of power switch QC and its driver.

3: t_{OFF} is the turn-off delay of power switch QD and its driver.
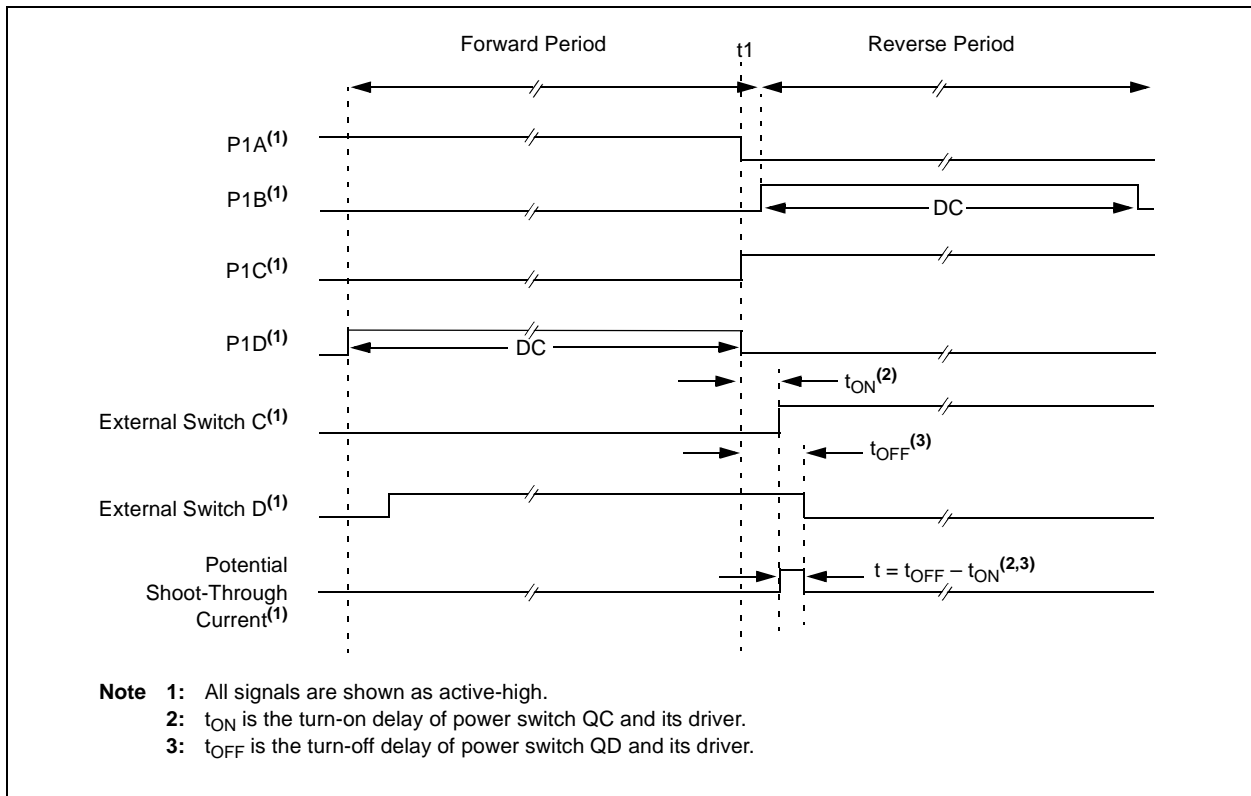
REGISTER 17-3: **ECCPxAS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPxASE	ECCPxAS2	ECCPxAS1	ECCPxAS0	PSSxAC1	PSSxAC0	PSSxBD1	PSSxBD0

bit 7   bit 0

bit 7   **ECCPxASE:** ECCP Auto-Shutdown Event Status bit
0 = ECCP outputs are operating
1 = A shutdown event has occurred; ECCP outputs are in shutdown state

bit 6-4   **ECCPxAS2:ECCPxAS0:** ECCP Auto-Shutdown Source Select bits
000 = Auto-shutdown is disabled
001 = Comparator 1 output
010 = Comparator 2 output
011 = Either Comparator 1 or 2
100 = INT0/FLT0
101 = INT0/FLT0 or Comparator 1
110 = INT0/FLT0 or Comparator 2
111 = INT0/FLT0 or Comparator 1 or Comparator 2

bit 3-2   **PSSxAC1:PSSxAC0:** Pins A and C Shutdown State Control bits
00 = Drive Pins A and C to '0'
01 = Drive Pins A and C to '1'
1x = Pins A and C tri-state

bit 1-0   **PSSxBD1:PSSxBD0:** Pins B and D Shutdown State Control bits
00 = Drive Pins B and D to '0'
01 = Drive Pins B and D to '1'
1x = Pins B and D tri-state

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

REGISTER 18-2: **SSPCON1: MSSP CONTROL REGISTER 1 (SPI MODE)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0

bit 7   bit 0

bit 7   **WCOL:** Write Collision Detect bit (Transmit mode only)

1 = The SSPBUF register is written while it is still transmitting the previous word
    (must be cleared in software)
0 = No collision

bit 6   **SSPOV:** Receive Overflow Indicator bit

SPI Slave mode:

1 = A new byte is received while the SSPBUF register is still holding the previous data. In case
    of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. The user
    must read the SSPBUF, even if only transmitting data, to avoid setting overflow (must be
    cleared in software).
0 = No overflow

> **Note:** In Master mode, the overflow bit is not set since each new reception (and
> transmission) is initiated by writing to the SSPBUF register.

bit 5   **SSPEN:** Master Synchronous Serial Port Enable bit

1 = Enables serial port and configures SCK, SDO, SDI and $\overline{SS}$ as serial port pins
0 = Disables serial port and configures these pins as I/O port pins

> **Note:** When enabled, these pins must be properly configured as input or output.

bit 4   **CKP:** Clock Polarity Select bit

1 = Idle state for clock is a high level
0 = Idle state for clock is a low level

bit 3-0 **SSPM3:SSPM0:** Master Synchronous Serial Port Mode Select bits

0101 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control disabled, $\overline{SS}$ can be used as I/O pin
0100 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control enabled
0011 = SPI Master mode, clock = TMR2 output/2
0010 = SPI Master mode, clock = FOSC/64
0001 = SPI Master mode, clock = FOSC/16
0000 = SPI Master mode, clock = FOSC/4

> **Note:** Bit combinations not specifically listed here are either reserved or implemented in
> I²C mode only.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

18.4.8 I²C MASTER MODE START CONDITION TIMING

To initiate a Start condition, the user sets the Start condition enable bit, SEN (SSPCON2<0>). If the SDA and SCL pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and starts its count. If SCL and SDA are both sampled high when the Baud Rate Generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low while SCL is high is the Start condition and causes the S bit (SSPSTAT<3>) to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit (SSPCON2<0>) will be automatically cleared by hardware, the Baud Rate Generator is suspended, leaving the SDA line held low and the Start condition is complete.

> **Note:** If at the beginning of the Start condition, the SDA and SCL pins are already sampled low, or if during the Start condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLIF, is set, the Start condition is aborted and the I²C module is reset into its Idle state.

18.4.8.1 WCOL Status Flag

If the user writes the SSPBUF when a Start sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

> **Note:** Because queueing of events is not allowed, writing to the lower 5 bits of SSPCON2 is disabled until the Start condition is complete.

FIGURE 18-19: FIRST START BIT TIMING
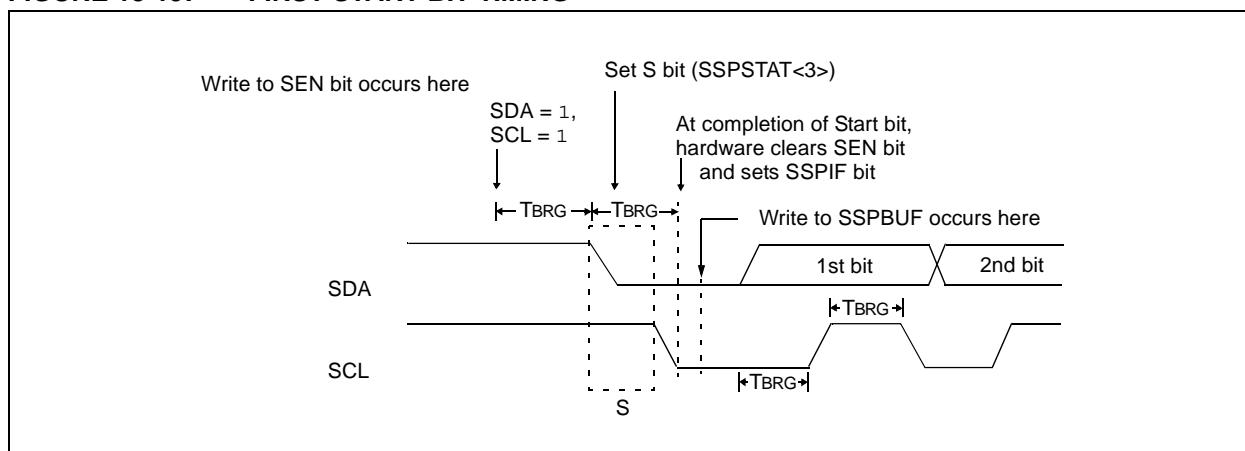
20.4 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers control the operation of the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

Note 1:	When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as a digital input will convert as an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.
2:	Analog levels on any pin defined as a digital input may cause the input buffer to consume current out of the device's specification limits.

20.5 A/D Conversions

Figure 20-3 shows the operation of the A/D converter after the GO/$\overline{DONE}$ bit has been set. Clearing the GO/$\overline{DONE}$ bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. That is, the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers). After the A/D conversion is aborted, a 2 T_{AD} wait is required before the next acquisition is started. After this 2 T_{AD} wait, acquisition on the selected channel is automatically started.

Note:	The GO/$\overline{DONE}$ bit should **NOT** be set in the same instruction that turns on the A/D.

FIGURE 20-3: **A/D CONVERSION T_{AD} CYCLES**
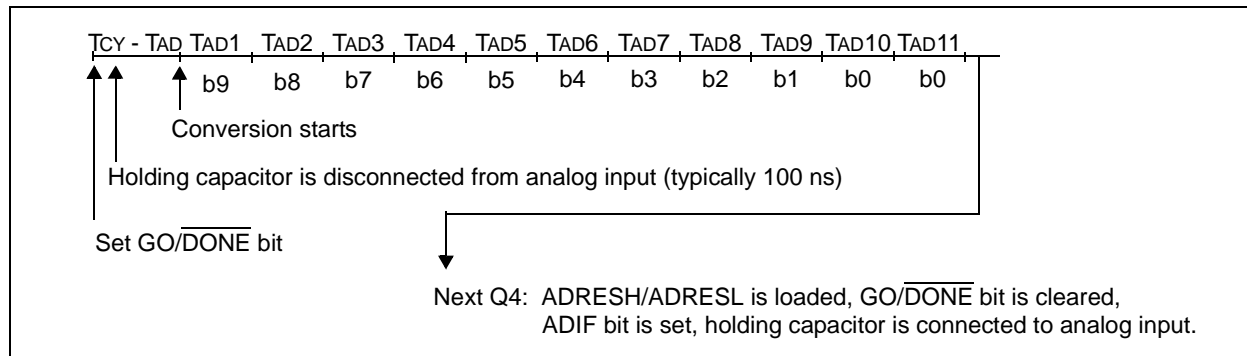
21.7 Comparator Operation During Sleep

When a comparator is active and the device is placed in Sleep mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will wake-up the device from Sleep mode when enabled. While the comparator is powered up, higher Sleep currents than shown in the power-down current specification will occur. Each operational comparator will consume additional current, as shown in the comparator specifications. To minimize power consumption while in Sleep mode, turn off the comparators, CM<2:0> = 111, before entering Sleep. If the device wakes up from Sleep, the contents of the CMCON register are not affected.

21.8 Effects of a Reset

A device Reset forces the CMCON register to its Reset state, causing the comparator module to be in the comparator Reset mode, CM<2:0> = 000. This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at Reset time. The comparators will be powered down during the Reset interval.

21.9 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 21-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up condition may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

FIGURE 21-4: COMPARATOR ANALOG INPUT MODEL

Legend:
CPIN = Input Capacitance
VT = Threshold Voltage
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC = Interconnect Resistance
RS = Source Impedance
VA = Analog Voltage
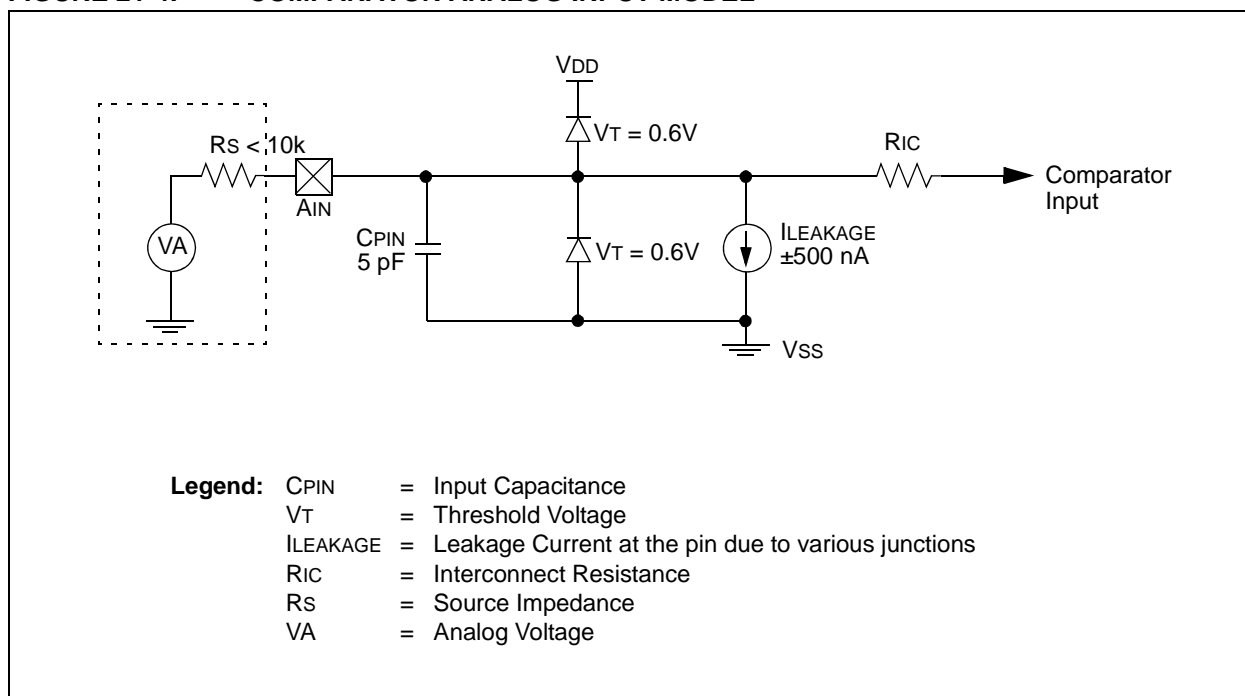
FIGURE 23-2:   **LOW-VOLTAGE DETECT (LVD) BLOCK DIAGRAM**
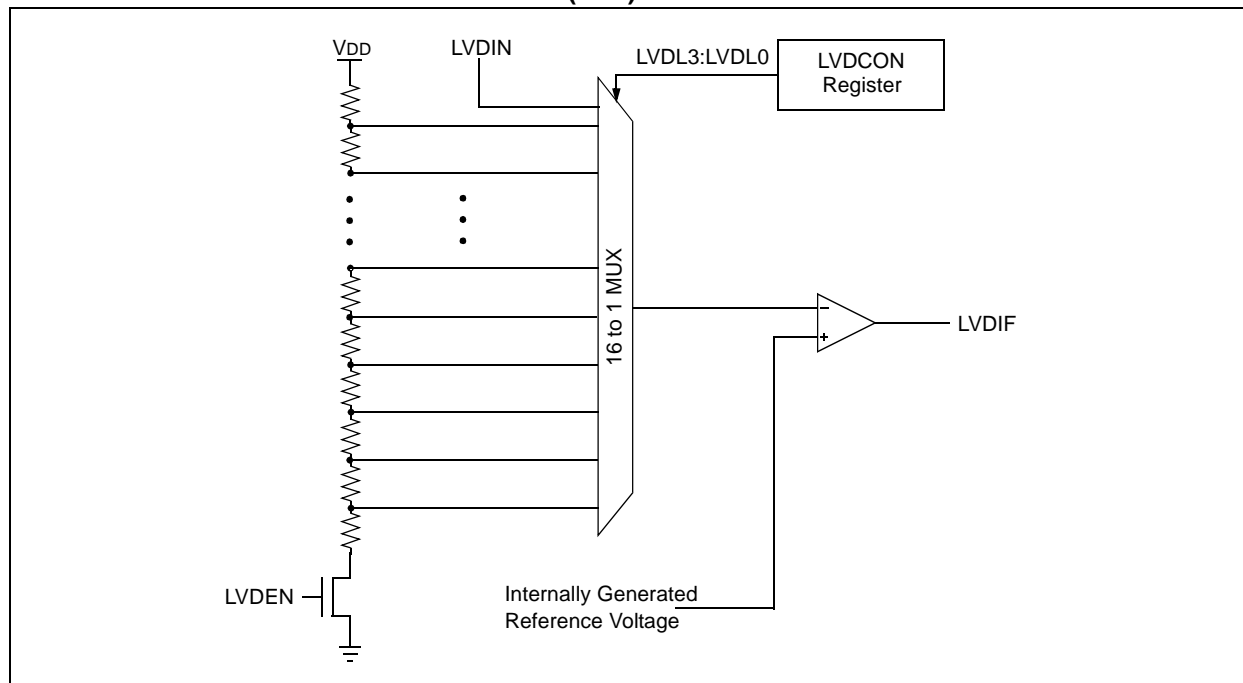
The LVD module has an additional feature that allows the user to supply the trip voltage to the module from an external source. This mode is enabled when bits LVDL3:LVDL0 are set to '1111'. In this state, the comparator input is multiplexed from the external input pin, LVDIN (Figure 23-3). This gives users flexibility because it allows them to configure the Low-Voltage Detect interrupt to occur at any voltage in the valid operating range.

FIGURE 23-3:   **LOW-VOLTAGE DETECT (LVD) WITH EXTERNAL INPUT BLOCK DIAGRAM**
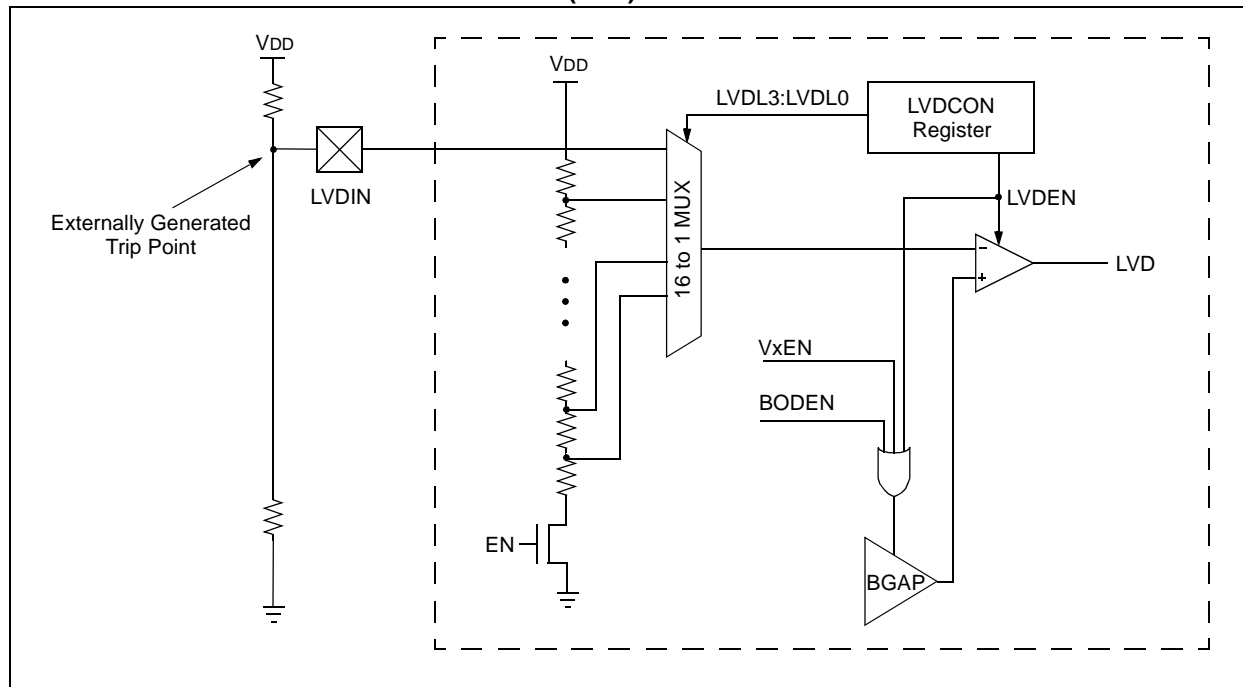
26.0   DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

• Integrated Development Environment
  - MPLAB® IDE Software
• Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
  - MPLAB C30 C Compiler
  - MPLAB ASM30 Assembler/Linker/Library
• Simulators
  - MPLAB SIM Software Simulator
  - MPLAB dsPIC30 Software Simulator
• Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB ICE 4000 In-Circuit Emulator
• In-Circuit Debugger
  - MPLAB ICD 2
• Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Development Programmer
  - MPLAB PM3 Device Programmer
• Low-Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM.net™ Demonstration Board
  - PICDEM 2 Plus Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 4 Demonstration Board
  - PICDEM 17 Demonstration Board
  - PICDEM 18R Demonstration Board
  - PICDEM LIN Demonstration Board
  - PICDEM USB Demonstration Board
• Evaluation Kits
  - KEELOQ® Evaluation and Programming Tools
  - PICDEM MSC
  - microID® Developer Kits
  - CAN
  - PowerSmart® Developer Kits
  - Analog

26.1   MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit micro-controller market. The MPLAB IDE is a Windows® based application that contains:

• An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
• A full-featured editor with color coded context
• A multiple project manager
• Customizable data windows with direct edit of contents
• High-level source code debugging
• Mouse over variable inspection
• Extensive on-line help

The MPLAB IDE allows you to:

• Edit your source files (either assembly or C)
• One touch assemble (or compile) and download to PIC emulator and simulator tools (automatically updates all project information)
• Debug using:
  - source files (assembly or C)
  - mixed assembly and C
  - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

26.2   MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

• Integration into MPLAB IDE projects
• User defined macros to streamline assembly code
• Conditional assembly for multi-purpose source files
• Directives that allow complete control over the assembly process

26.14 PICSTART Plus Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus development programmer supports most PIC devices up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

26.15 PICDEM 1 PIC MCU Demonstration Board

The PICDEM 1 demonstration board demonstrates the capabilities of the PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The sample microcontrollers provided with the PICDEM 1 demonstration board can be programmed with a PRO MATE II device programmer or a PICSTART Plus development programmer. The PICDEM 1 demonstration board can be connected to the MPLAB ICE in-circuit emulator for testing. A prototype area extends the circuitry for additional application components. Features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs.

26.16 PICDEM.net Internet/Ethernet Demonstration Board

The PICDEM.net demonstration board is an Internet/Ethernet demonstration board using the PIC18F452 microcontroller and TCP/IP firmware. The board supports any 40-pin DIP device that conforms to the standard pinout used by the PIC16F877 or PIC18C452. This kit features a user friendly TCP/IP stack, web server with HTML, a 24L256 Serial EEPROM for Xmodem download to web pages into Serial EEPROM, ICSP/MPLAB ICD 2 interface connector, an Ethernet interface, RS-232 interface and a 16 x 2 LCD display. Also included is the book and CD-ROM *"TCP/IP Lean, Web Servers for Embedded Systems,"* by Jeremy Bentham

26.17 PICDEM 2 Plus Demonstration Board

The PICDEM 2 Plus demonstration board supports many 18, 28 and 40-pin microcontrollers, including PIC16F87X and PIC18FXX2 devices. All the necessary hardware and software is included to run the demonstration programs. The sample microcontrollers provided with the PICDEM 2 demonstration board can be programmed with a PRO MATE II device programmer, PICSTART Plus development programmer, or MPLAB ICD 2 with a Universal Programmer Adapter. The MPLAB ICD 2 and MPLAB ICE in-circuit emulators may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area extends the circuitry for additional application components. Some of the features include an RS-232 interface, a 2 x 16 LCD display, a piezo speaker, an on-board temperature sensor, four LEDs and sample PIC18F452 and PIC16F877 Flash microcontrollers.

26.18 PICDEM 3 PIC16C92X Demonstration Board

The PICDEM 3 demonstration board supports the PIC16C923 and PIC16C924 in the PLCC package. All the necessary hardware and software is included to run the demonstration programs.

26.19 PICDEM 4 8/14/18-Pin Demonstration Board

The PICDEM 4 can be used to demonstrate the capabilities of the 8, 14 and 18-pin PIC16XXXX and PIC18XXXX MCUs, including the PIC16F818/819, PIC16F87/88, PIC16F62XA and the PIC18F1320 family of microcontrollers. PICDEM 4 is intended to showcase the many features of these low pin count parts, including LIN and Motor Control using ECCP. Special provisions are made for low-power operation with the supercapacitor circuit and jumpers allow on-board hardware to be disabled to eliminate current draw in this mode. Included on the demo board are provisions for Crystal, RC or Canned Oscillator modes, a five volt regulator for use with a nine volt wall adapter or battery, DB-9 RS-232 interface, ICD connector for programming via ICSP and development with MPLAB ICD 2, 2 x 16 liquid crystal display, PCB footprints for H-Bridge motor driver, LIN transceiver and EEPROM. Also included are: header for expansion, eight LEDs, four potentiometers, three push buttons and a prototyping area. Included with the kit is a PIC16F627A and a PIC18F1320. Tutorial firmware is included along with the User's Guide.

PIC18F6525/6621/8525/8621

27.3 DC Characteristics: PIC18F6525/6621/8525/8621 (Industrial, Extended) PIC18LF6X2X/8X2X (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended			
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
D080	VOL	**Output Low Voltage** I/O ports	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083		OSC2/CLKO (RC mode)	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A			—	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C
D090	VOH	**Output High Voltage**[3] I/O ports	VDD – 0.7	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD – 0.7	—	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092		OSC2/CLKO (RC mode)	VDD – 0.7	—	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD – 0.7	—	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
D150	VOD	**Open-Drain High Voltage**	—	8.5	V	RA4 pin
D100[4]	COSC2	**Capacitive Loading Specs on Output Pins** OSC2 pin	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins and OSC2 (in RC mode)	—	50	pF	To meet the AC Timing Specifications
D102	CB	SCL, SDA	—	400	pF	In I2C™ mode

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC® device be driven with an external clock while in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Parameter is characterized but not tested.

Param. No	Symbol	Characteristics	Min	Typ	Max	Units
171	TalH2csL	Chip Enable Active to ALE ↓	—	—	10	ns
171A	TubL2oeH	AD Valid to Chip Enable Active	0.25 T$_{CY}$ – 20	—	—	ns

FIGURE 27-9: **RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**

Note: Refer to Figure 27-4 for load conditions.
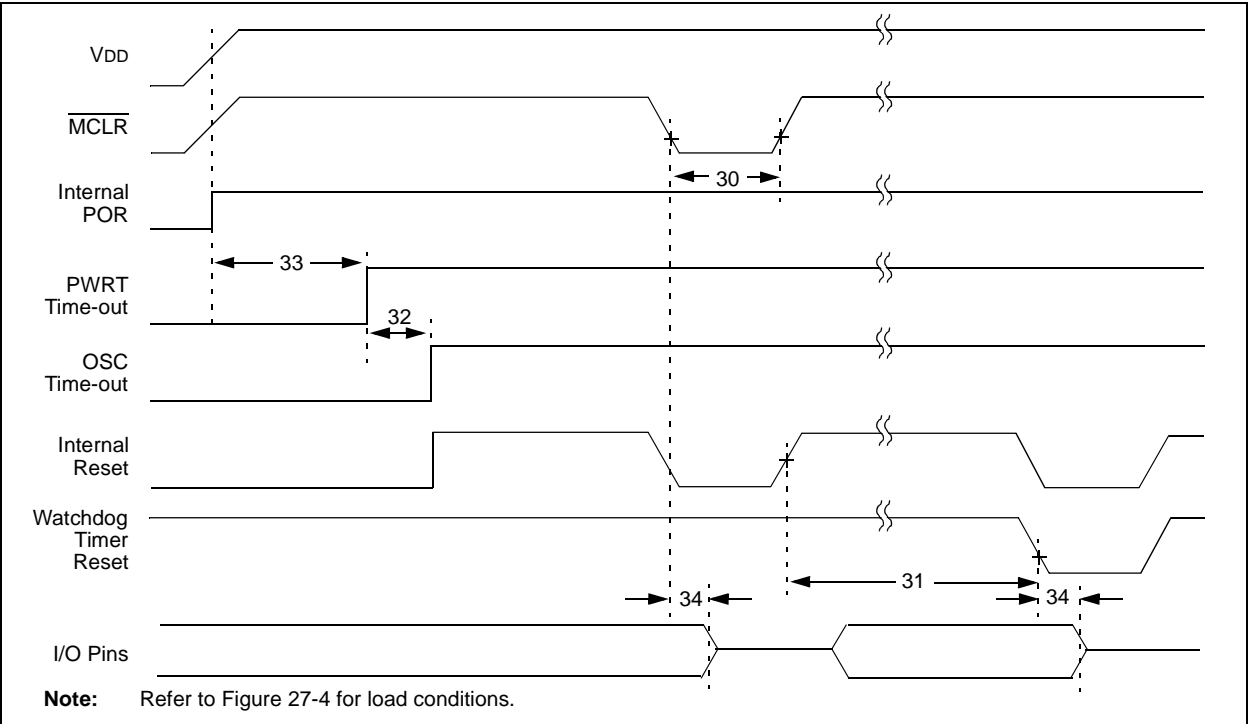
FIGURE 27-10: **BROWN-OUT RESET TIMING**
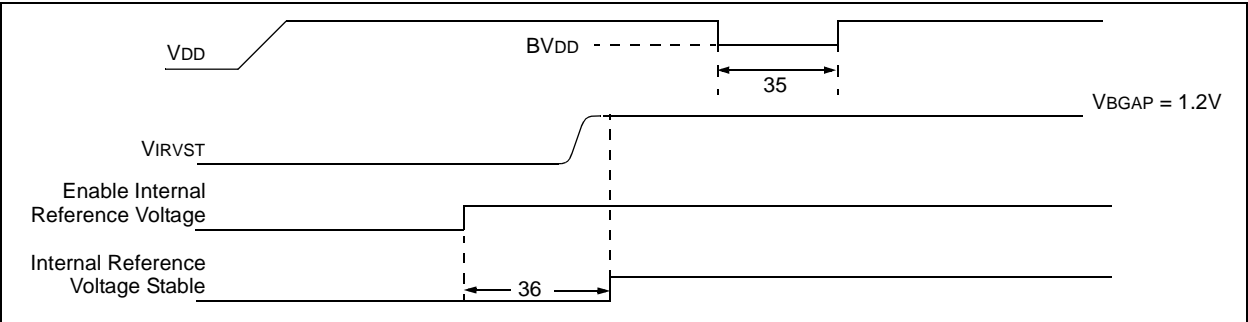
FIGURE 28-13: **AVERAGE F**OSC **vs. V**DD **FOR VARIOUS R**S **(RC MODE, C = 100 pF, TEMP = 25°C)**
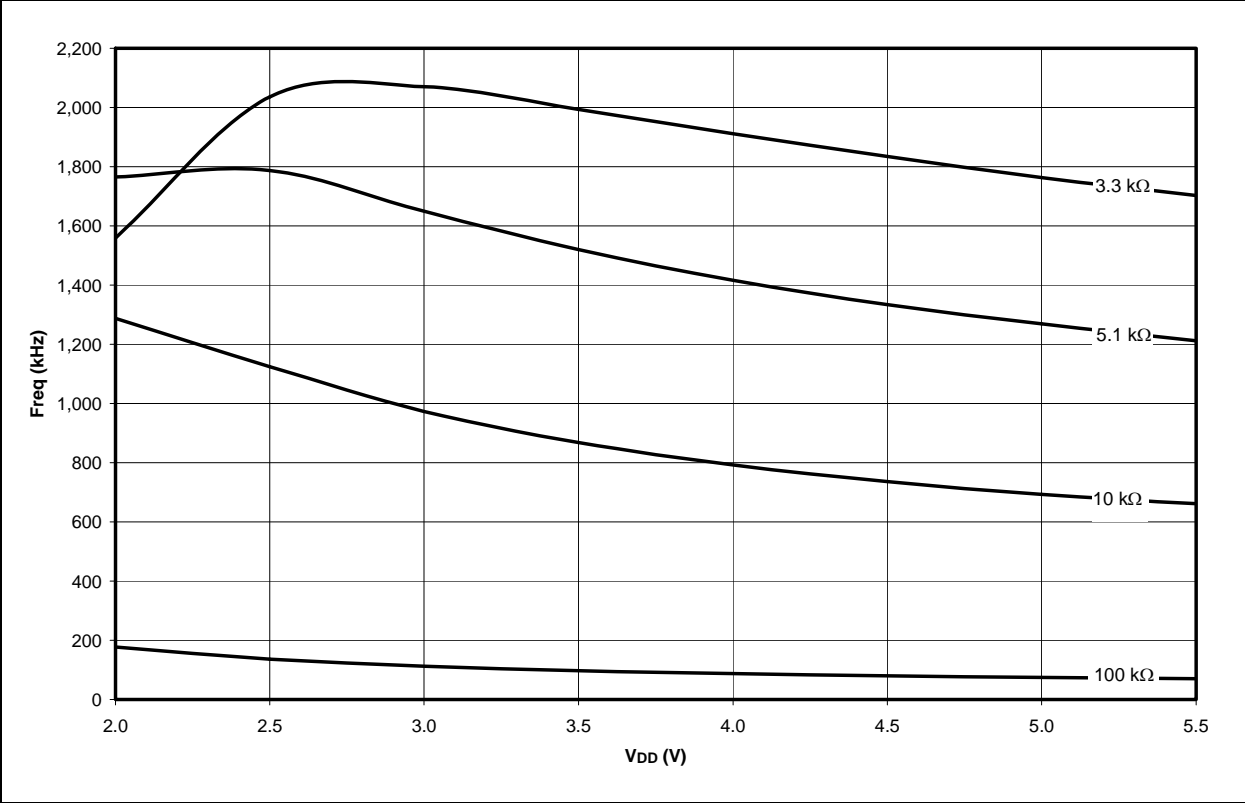
FIGURE 28-14: **AVERAGE F**OSC **vs. V**DD **FOR VARIOUS R**S **(RC MODE, C = 300 pF, TEMP = 25°C)**

PIC18F6525/6621/8525/8621 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–	X	/XX	XXX
Device		Temperature Range	Package	Pattern

Device	PIC18F6525/6621/8525/8621[1], PIC18F6525/6621/8525/8621T[2]; V_{DD} range 4.2V to 5.5V PIC18LF6X2X/8X2X[1], PIC18LF6X2X/8X2XT[2]; V_{DD} range 2.0V to 5.5V
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package	PT = TQFP (Thin Quad Flatpack)
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18LF6621-I/PT 301 = Industrial temp., TQFP package, Extended V_{DD} limits, QTP pattern #301.

b) PIC18F8621-E/PT = Extended temp., TQFP package, standard V_{DD} limits.

Note 1: F = Standard Voltage Range
LF = Extended Voltage Range

2: T = in tape and reel