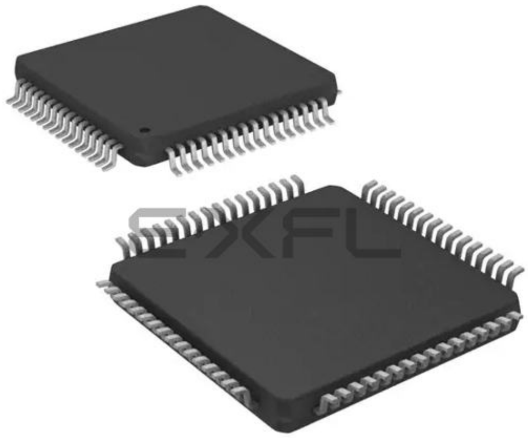
Silicon Labs - EFM32GG11B110F2048GQ64-A Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b110f2048gq64-a

- **Timers/Counters**
  - 7× 16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels (4 + 4 on one timer instance)
    - Dead-Time Insertion on several timer instances
  - 4× 32-bit Timer/Counter
  - 32-bit Real Time Counter and Calendar (RTCC)
  - 24-bit Real Time Counter (RTC)
  - 32-bit Ultra Low Energy CRYOTIMER for periodic wakeup from any Energy Mode
  - 2× 16-bit Low Energy Timer for waveform generation
  - 3× 16-bit Pulse Counter with asynchronous operation
  - 2× Watchdog Timer with dedicated RC oscillator
- **Low Energy Sensor Interface (LESENSE)**
  - Autonomous sensor monitoring in Deep Sleep Mode
  - Wide range of sensors supported, including LC sensors and capacitive buttons
  - Up to 16 inputs
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
  - 2-pin Serial Wire Debug interface
  - 1-pin Serial Wire Viewer
  - 4-pin JTAG interface
  - Embedded Trace Macrocell (ETM)
- **Pre-Programmed USB/UART Bootloader**
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - Standard (-40 °C to 85 °C T_{AMB}) and Extended (-40 °C to 125 °C T_J) temperature grades available
- **Packages**
  - QFN64 (9x9 mm)
  - TQFP64 (10x10 mm)
  - TQFP100 (14x14 mm)
  - BGA112 (10x10 mm)
  - BGA120 (7x7 mm)
  - BGA152 (8x8 mm)
  - BGA192 (7x7mm)

4.1.7 Current Consumption

4.1.7.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.7. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	72 MHz HFRCO, CPU running Prime from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	120	TBD	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	140	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	123	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	122	TBD	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	126	TBD	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	131	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	319	TBD	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	107	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	262	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	72 MHz HFRCO	—	57	TBD	µA/MHz
		50 MHz crystal	—	60	—	µA/MHz
		48 MHz HFRCO	—	59	TBD	µA/MHz
		32 MHz HFRCO	—	61	—	µA/MHz
		26 MHz HFRCO	—	63	TBD	µA/MHz
		16 MHz HFRCO	—	68	—	µA/MHz
		1 MHz HFRCO	—	255	TBD	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	55	—	µA/MHz
		1 MHz HFRCO	—	210	—	µA/MHz

4.1.7.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.9. Current Consumption 1.8 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	72 MHz HFRCO, CPU running Prime from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	140	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	122	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	122	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	126	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	131	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	315	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	107	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	259	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	72 MHz HFRCO	—	57	—	µA/MHz
		50 MHz crystal	—	59	—	µA/MHz
		48 MHz HFRCO	—	59	—	µA/MHz
		32 MHz HFRCO	—	61	—	µA/MHz
		26 MHz HFRCO	—	63	—	µA/MHz
		16 MHz HFRCO	—	68	—	µA/MHz
		1 MHz HFRCO	—	252	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	55	—	µA/MHz
		1 MHz HFRCO	—	207	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	3.7	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	4.0	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.5	—	µA

4.1.17 Current Digital to Analog Converter (IDAC)

Table 4.25. Current Digital to Analog Converter (IDAC)

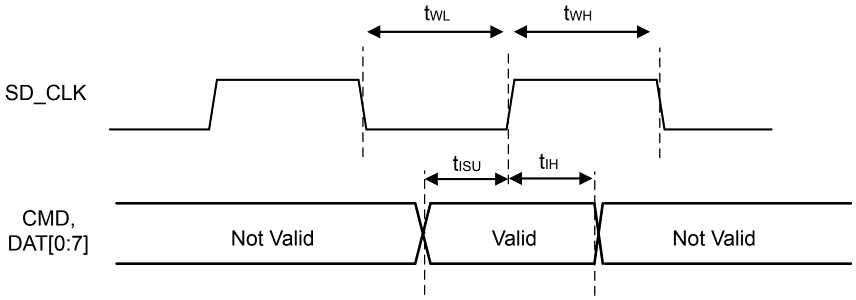
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of ranges	N_{IDAC_RANGES}		—	4	—	ranges
Output current	I_{IDAC_OUT}	RANGSEL[1] = RANGE0	0.05	—	1.6	µA
		RANGSEL[1] = RANGE1	1.6	—	4.7	µA
		RANGSEL[1] = RANGE2	0.5	—	16	µA
		RANGSEL[1] = RANGE3	2	—	64	µA
Linear steps within each range	N_{IDAC_STEPS}		—	32	—	steps
Step size	SS_{IDAC}	RANGSEL[1] = RANGE0	—	50	—	nA
		RANGSEL[1] = RANGE1	—	100	—	nA
		RANGSEL[1] = RANGE2	—	500	—	nA
		RANGSEL[1] = RANGE3	—	2	—	µA
Total accuracy, STEPSEL[1] = 0x10	ACC_{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	TBD	—	TBD	%
		EM0 or EM1, Across operating temperature range	TBD	—	TBD	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-2.7	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-2.5	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-1.5	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-1.0	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-1.1	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-1.1	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.9	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.9	—	%

4.1.24 USART SPI

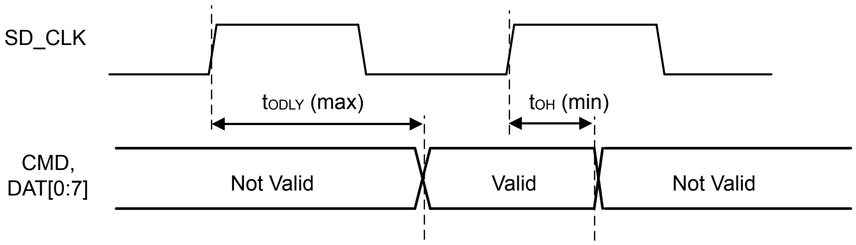
SPI Master Timing

Table 4.34. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}	All USARTs except USART2	2 * $t_{HFPERCLK}$	—	—	ns
		USART2	2 * $t_{HFPERBCLK}$	—	—	ns
CS to MOSI [1] [3]	t_{CS_MO}	USART2, location 4, IOVDD = 1.8 V	-3.2	—	6.8	ns
		USART2, location 4, IOVDD = 3.0 V	-2.3	—	6.0	ns
		USART2, location 5, IOVDD = 1.8 V	-8.1	—	6.3	ns
		USART2, location 5, IOVDD = 3.0 V	-7.3	—	4.4	ns
		All other USARTs and locations, IOVDD = 1.8 V	-15	—	13	ns
		All other USARTs and locations, IOVDD = 3.0 V	-13	—	11	ns
SCLK to MOSI [1] [3]	t_{SCLK_MO}	USART2, location 4, IOVDD = 1.8 V	-0.3	—	9.2	ns
		USART2, location 4, IOVDD = 3.0 V	-0.3	—	8.6	ns
		USART2, location 5, IOVDD = 1.8 V	-3.6	—	5.0	ns
		USART2, location 5, IOVDD = 3.0 V	-3.4	—	3.2	ns
		All other USARTs and locations, IOVDD = 1.8 V	-10	—	11	ns
		All other USARTs and locations, IOVDD = 3.0 V	-9	—	11	ns
MISO setup time [1] [3]	t_{SU_MI}	USART2, location 4, IOVDD = 1.8 V	39.7	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	22.4	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	49.2	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	30.0	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	55	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	36	—	—	ns



Input Timing



Output Timing

Figure 4.14. SDIO HS Mode Timing

SDIO MMC SDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.51. SDIO MMC SDR Mode Timing (Location 0, 3V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	48	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	9.4	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	9.4	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.96	3.87	—	ns
Clock fall time	t_F		1.67	3.31	—	ns
Input setup time, CMD, DAT[0:7] valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:7] change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:7] valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD, DAT[0:7] change	t_{OH}		3	—	—	ns

QSPI SDR Mode Timing (Locations 1, 2)

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 34, RX DLL = 59, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.55. QSPI SDR Mode Timing (Locations 1, 2)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Full SCLK period	T		$(1/F_{SCLK})$ * 0.95	—	—	ns
Output valid	t_{OV}		—	—	T/2 - 2.1	ns
Output hold	t_{OH}		T/2 - 42.3	—	—	ns
Input setup	t_{SU}		48.2 - T/2	—	—	ns
Input hold	t_H		T/2 - 5.1	—	—	ns

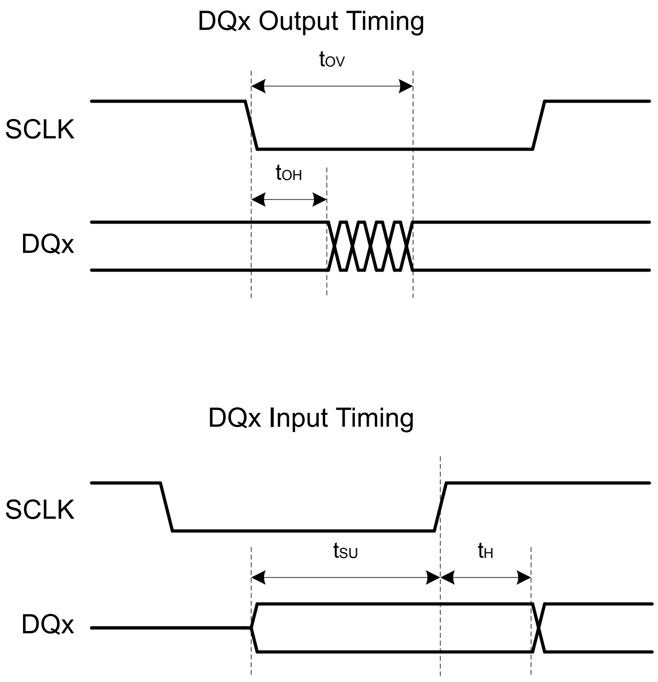


Figure 4.21. QSPI SDR Timing Diagrams

QSPI SDR Flash Timing Example

This example uses timing values for location 0 (SDR mode) to demonstrate the calculation of allowable flash timing using the QSPI in SDR mode.

- Using a configured SCLK frequency (F_{SCLK}) of 19 MHz:
- The resulting minimum period, T(min) = $(1/F_{SCLK})$ * 0.95 = 50.0 ns.
- Flash will see a minimum setup time of T/2 – t_{OV} = T/2 – (T/2 – 2.4) = 2.4 ns.
- Flash will see a minimum hold time of T/2 + t_{OH} = T/2 + (T/2 – 32.9) = T – 32.9 = 50.0 – 32.9 = 17.1 ns.
- Flash can have a maximum output valid time of T/2 – t_{SU} = T/2 – (36.2 – T/2) = T – 36.2 = 50.0 – 36.2 = 13.8 ns.
- Flash can have a minimum output hold time of t_H – T/2 = (T/2 – 3.3) – T/2 = - 3.3 ns.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	M2	GPIO	PB3	M3	GPIO
PC6	M14	GPIO	VREGVSS	M15 N16	Voltage regulator VSS
VREGSW	M16	DCDC regulator switching node	PB4	N1	GPIO
PB5	N2	GPIO	PB6	N3	GPIO
PD5	N14	GPIO	PD4	N15	GPIO
PC0	P1	GPIO (5V)	PC1	P2	GPIO (5V)
PC2	P3	GPIO (5V)	PA8	P4	GPIO
PA11	P5	GPIO	PA13	P6	GPIO (5V)
PB9	P7	GPIO (5V)	PB12	P8	GPIO
PH2	P9	GPIO (5V)	PH5	P10	GPIO
PH8	P11	GPIO (5V)	PH11	P12	GPIO (5V)
PH13	P13	GPIO (5V)	PD0	P14	GPIO (5V)
PD3	P15	GPIO	PD8	P16	GPIO
PB7	R1	GPIO	PC3	R2	GPIO (5V)
PC5	R3	GPIO	PA9	R4	GPIO
BODEN	R5	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	RESETn	R6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB10	R7	GPIO (5V)	PH0	R8	GPIO (5V)
PH3	R9	GPIO (5V)	PH6	R10	GPIO
PH9	R11	GPIO (5V)	PH12	R12	GPIO (5V)
PH14	R13	GPIO (5V)	PH15	R14	GPIO (5V)
PD2	R15	GPIO (5V)	PD7	R16	GPIO
PB8	T1	GPIO	PC4	T2	GPIO
PA7	T3	GPIO	PA10	T4	GPIO
PA12	T5	GPIO (5V)	PA14	T6	GPIO
PB11	T7	GPIO	PH1	T8	GPIO (5V)
PH4	T9	GPIO	PH7	T10	GPIO (5V)
PH10	T11	GPIO (5V)	PB13	T12	GPIO
PB14	T13	GPIO	AVDD	T14	Analog power supply.
PD1	T15	GPIO	PD6	T16	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PD15	J2	GPIO (5V)	PC6	J12	GPIO
DECOUPLE	J13	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC0	K1	GPIO (5V)
PC1	K2	GPIO (5V)	PD8	K13	GPIO
PC2	L1	GPIO (5V)	PC3	L2	GPIO (5V)
PA7	L3	GPIO	PB9	L15	GPIO (5V)
PB10	L16	GPIO (5V)	PD0	L17	GPIO (5V)
PD1	L18	GPIO	PD4	L19	GPIO
PD7	L20	GPIO	PB7	M1	GPIO
PC4	M2	GPIO	PA8	M3	GPIO
PA10	M4	GPIO	PA13	M5	GPIO (5V)
PA14	M6	GPIO	RESETn	M7	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	M9 M10 N11	Analog power supply.	PD3	M12	GPIO
PD6	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	PB12	N7	GPIO
PB13	N9	GPIO	PB14	N10	GPIO
PD2	N12	GPIO (5V)	PD5	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA12	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	PB12	22	GPIO
AVDD	24	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	28	GPIO (5V)
PD1	29	GPIO	PD2	30	GPIO (5V)
PD3	31	GPIO	PD4	32	GPIO
PD5	33	GPIO	PD6	34	GPIO
PD8	35	GPIO	VREGVSS	36	Voltage regulator VSS
VREGSW	37	DCDC regulator switching node	VREGVDD	38	Voltage regulator VDD input
DVDD	39	Digital power supply.	DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	41	GPIO	PE5	42	GPIO
PE6	43	GPIO	PE7	44	GPIO
VREGI	45	Input to 5 V regulator.	VREGO	46	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PF10	47	GPIO (5V)	PF11	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.
PF12	53	GPIO	PF5	54	GPIO
PE8	57	GPIO	PE9	58	GPIO
PE10	59	GPIO	PE11	60	GPIO
PE12	61	GPIO	PE13	62	GPIO
PE14	63	GPIO	PE15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.14 EFM32GG11B4xx in QFP64 Device Pinout

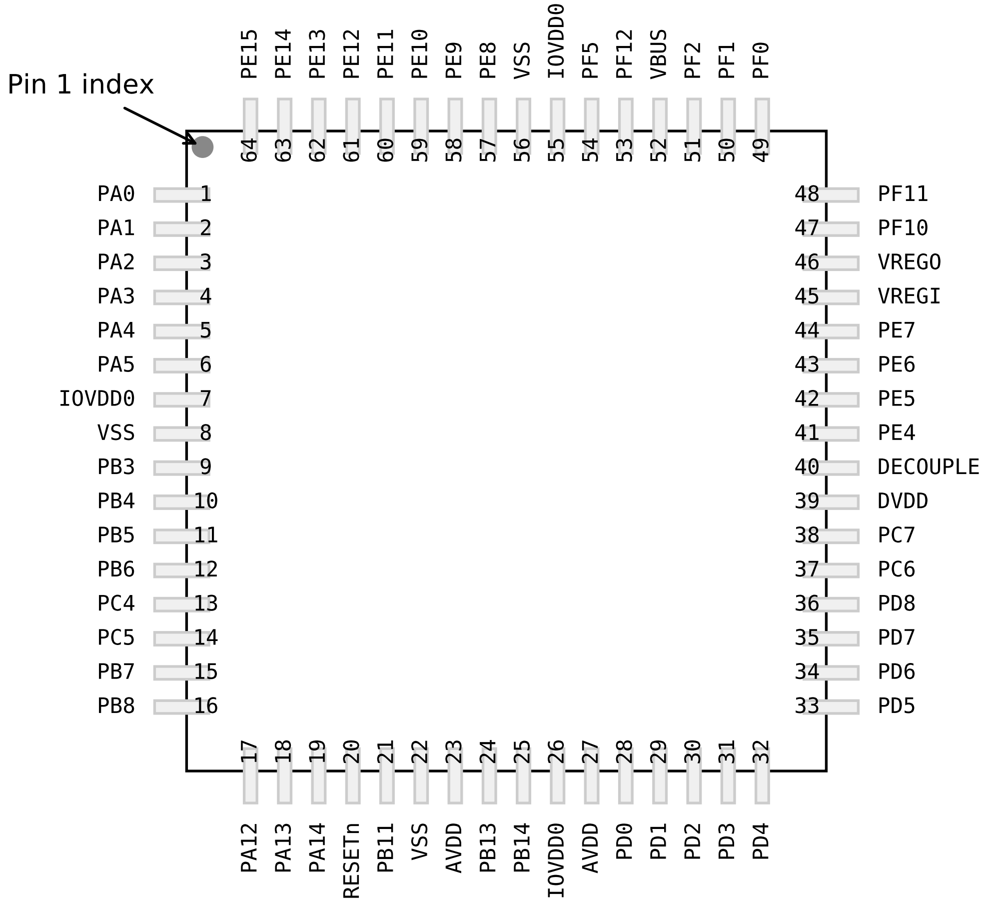


Figure 5.14. EFM32GG11B4xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.14. EFM32GG11B4xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 26 55	Digital IO power supply 0.	VSS	8 22 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

5.16 EFM32GG11B8xx in QFN64 Device Pinout

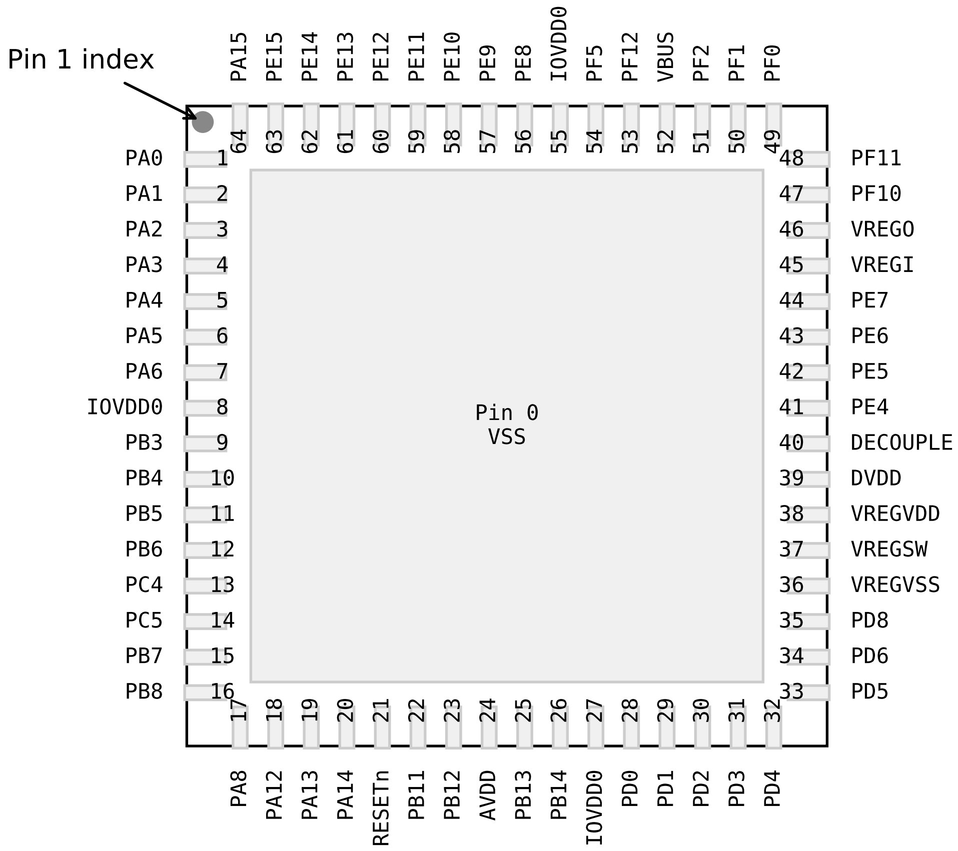


Figure 5.16. EFM32GG11B8xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.16. EFM32GG11B8xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 27 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA12	18	GPIO (5V)	PA13	19	GPIO (5V)
PA14	20	GPIO	RESETn	21	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	22	GPIO	PB12	23	GPIO
AVDD	24	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	28	GPIO (5V)
PD1	29	GPIO	PD2	30	GPIO (5V)
PD3	31	GPIO	PD4	32	GPIO
PD5	33	GPIO	PD6	34	GPIO
PD7	35	GPIO	PD8	36	GPIO
PC7	37	GPIO	VREGVSS	38	Voltage regulator VSS
VREGSW	39	DCDC regulator switching node	VREGVDD	40	Voltage regulator VDD input
DVDD	41	Digital power supply.	DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	43	GPIO	PE5	44	GPIO
PE6	45	GPIO	PE7	46	GPIO
PC12	47	GPIO (5V)	PC13	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	PF3	52	GPIO
PF4	53	GPIO	PF5	54	GPIO
PE8	56	GPIO	PE9	57	GPIO
PE10	58	GPIO	PE11	59	GPIO
PE12	60	GPIO	PE13	61	GPIO
PE14	62	GPIO	PE15	63	GPIO
PA15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO (5V)
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	VREGI	45	Input to 5 V regulator.
VREGO	46	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs	PF10	47	GPIO (5V)
PF11	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.	PF12	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_TSUTMR-TOG	0: PB6 1: PB15 2: PC3 3: PF9		Ethernet IEEE1588 Timer Toggle.
ETM_TCLK	0: PD7 1: PF8 2: PC6 3: PA6	4: PE11 5: PG15	Embedded Trace Module ETM clock .
ETM_TD0	0: PD6 1: PF9 2: PC7 3: PA2	4: PE12 5: PG14	Embedded Trace Module ETM data 0.
ETM_TD1	0: PD3 1: PD13 2: PD3 3: PA3	4: PE13 5: PG13	Embedded Trace Module ETM data 1.
ETM_TD2	0: PD4 1: PB15 2: PD4 3: PA4	4: PE14 5: PG12	Embedded Trace Module ETM data 2.
ETM_TD3	0: PD5 1: PF3 2: PD5 3: PA5	4: PE15 5: PG11	Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU5	0: PE13		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4

Table 5.25. ACMP2 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP2X																									PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
APORT0Y	BUSACMP2Y																									PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

8. BGA120 Package Specifications

8.1 BGA120 Package Dimensions

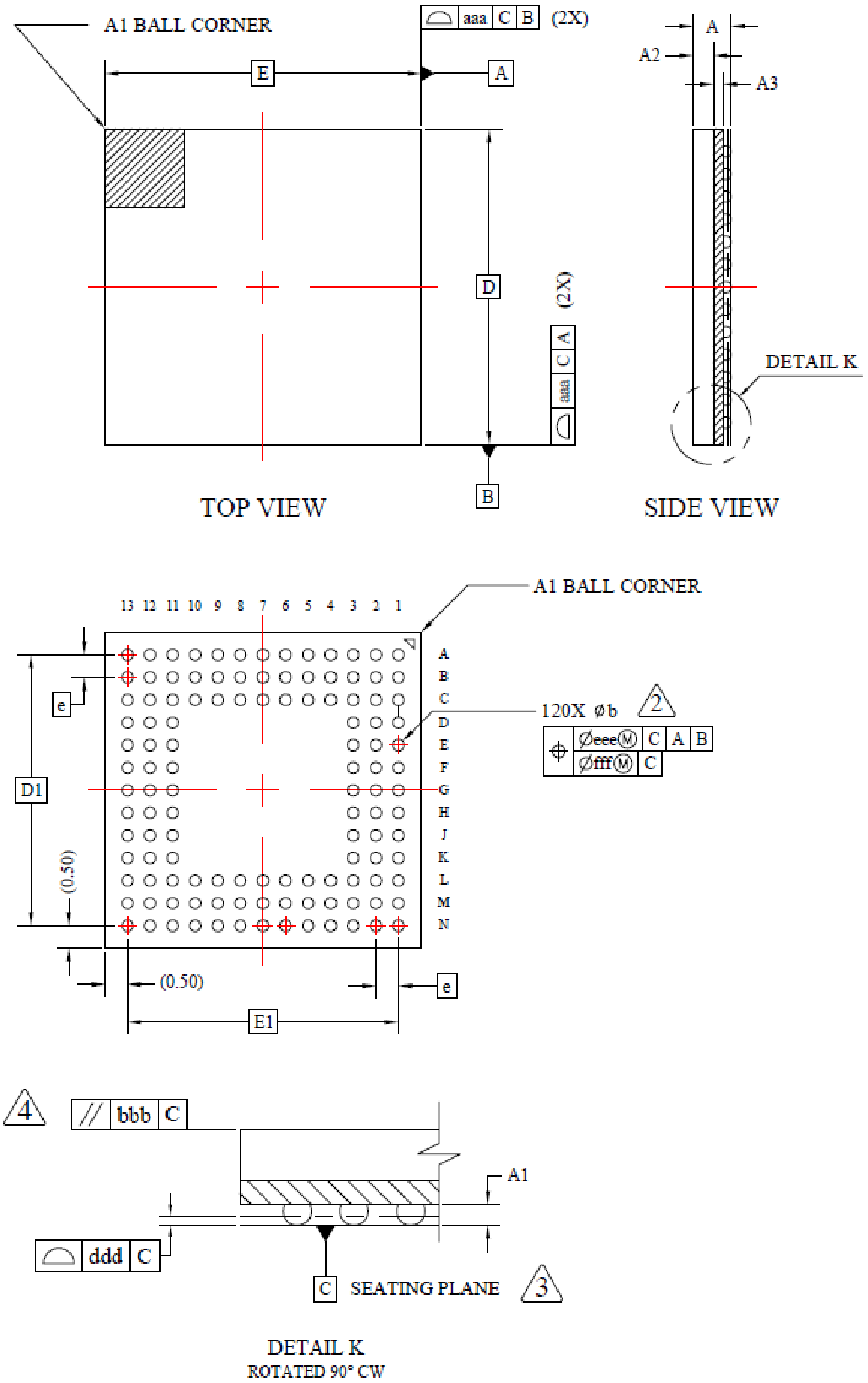


Figure 8.1. BGA120 Package Drawing

8.2 BGA120 PCB Land Pattern

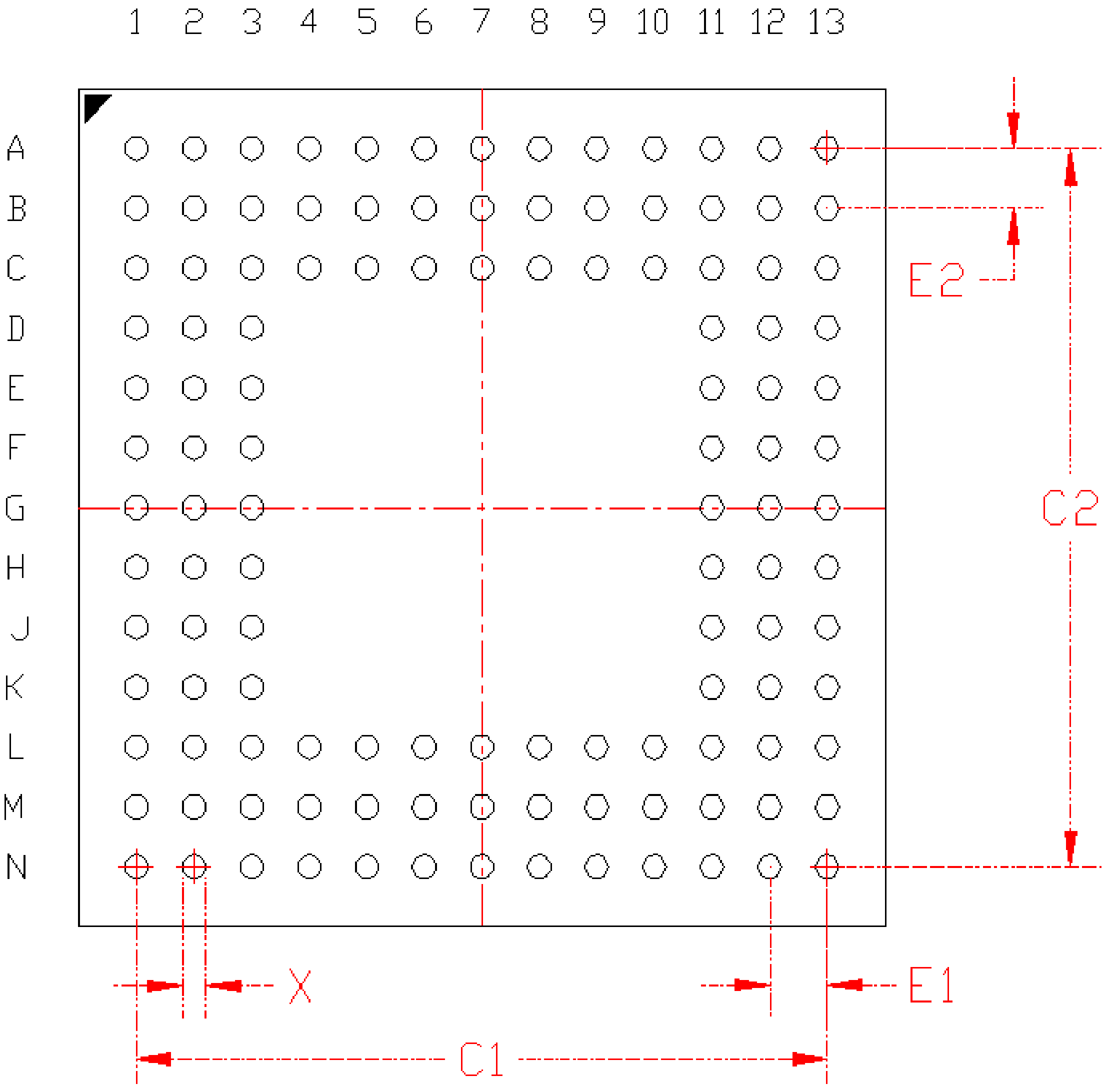


Figure 8.2. BGA120 PCB Land Pattern Drawing

Table 12.2. QFN64 PCB Land Pattern Dimensions

Dimension	Typ
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	7.30
Y2	7.30

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
8. A 3x3 array of 1.45 mm square openings on a 2.00 mm pitch can be used for the center ground pad.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.