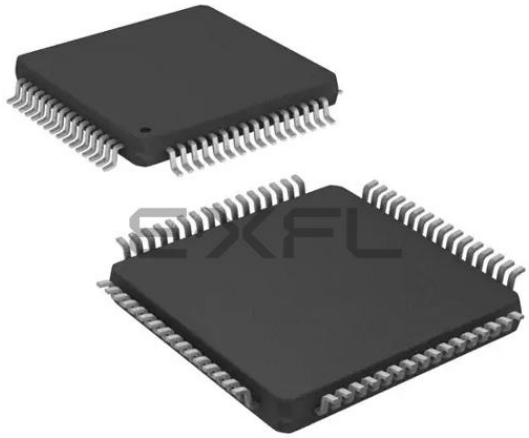

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b110f2048iq64-a

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	3.9	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	4.3	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.8	TBD	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFRCO	—	3.6	TBD	µA
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	1.08	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.69	—	µA
		128 byte RAM retention, no RTCC	—	0.69	TBD	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.16	TBD	µA
Current consumption of peripheral power domain 1, with voltage scaling enabled	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[1]	—	0.68	—	µA
Current consumption of peripheral power domain 2, with voltage scaling enabled	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[1]	—	0.28	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.4 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.8 Wake Up Times

Table 4.10. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	11.8	—	µs
		Code execution from RAM	—	4.1	—	µs
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	11.8	—	µs
		Code execution from RAM	—	4.1	—	µs
Wake up from EM4H[1]	t_{EM4H_WU}	Executing from flash	—	94	—	µs
Wake up from EM4S[1]	t_{EM4S_WU}	Executing from flash	—	294	—	µs
Time from release of reset source to first instruction execution	t_{RESET}	Soft Pin Reset released	—	55	—	µs
		Any other reset released	—	359	—	µs
Power mode scaling time	t_{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz[4] [2]	—	31.8	—	µs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz[3]	—	4.3	—	µs

Note:

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/µs for approximately 20 µs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 µs + 29 HFCLKs.
4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 µs + 28 HFCLKs.

4.1.12 General-Purpose I/O (GPIO)

Table 4.20. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	GPIO pins	—	—	IOVDD*0.3	V
Input high voltage	V_{IH}	GPIO pins	IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	TBD	nA
		All GPIO except LFXO pins, GPIO ≤ IOVDD, T > 85 °C	—	—	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T > 85 °C	—	—	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	TBD	µA
I/O pin pull-up/pull-down resistor	R_{PUD}		TBD	40	TBD	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		15	25	35	ns

4.1.21 Pulse Counter (PCNT)

Table 4.29. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	20	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.22 Analog Port (APORT)

Table 4.30. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current[2] [1]	I_{APORT}	Operation in EM0/EM1	—	7	—	µA
		Operation in EM2/EM3	—	915	—	nA

Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.
2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

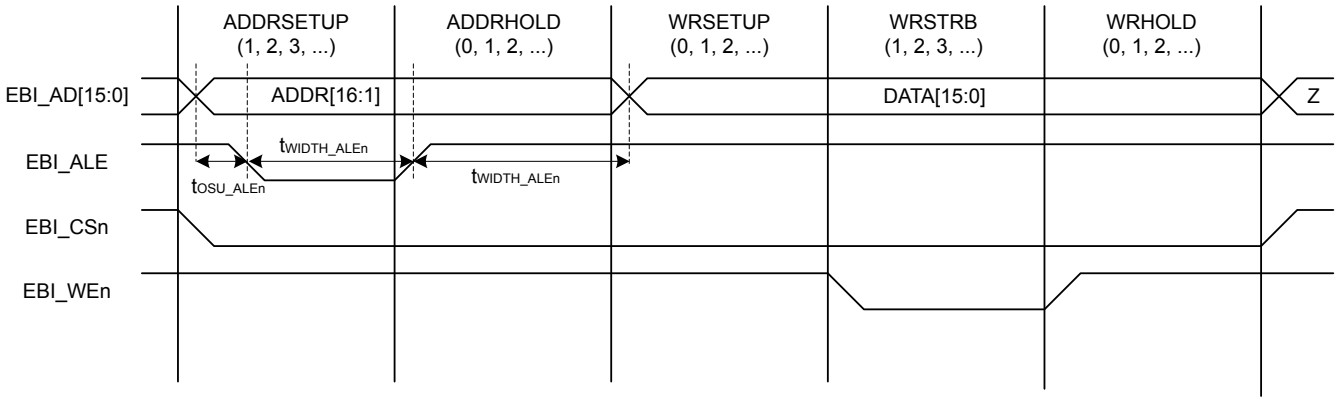

Figure 4.4. EBI Address Latch Enable Output Timing Diagram

4.1.27 Serial Data I/O Host Controller (SDIO)

SDIO DS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.46. SDIO DS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	23	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.69	3.23	—	ns
Clock fall time	t_F		1.42	2.79	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}		0	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}		0	—	14	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}		5	—	—	ns

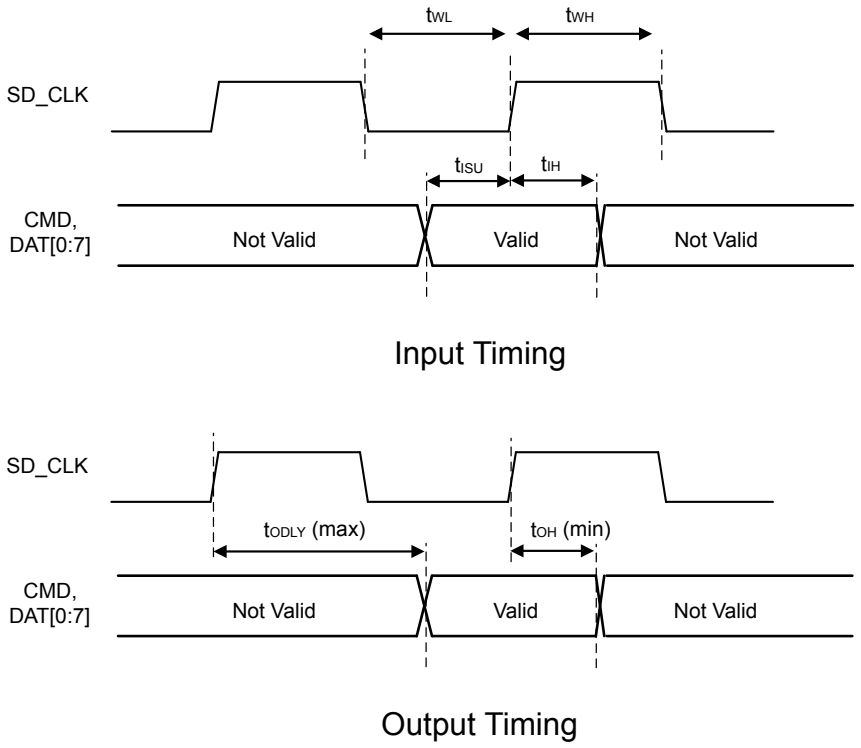

Figure 4.17. SDIO MMC SDR Mode Timing

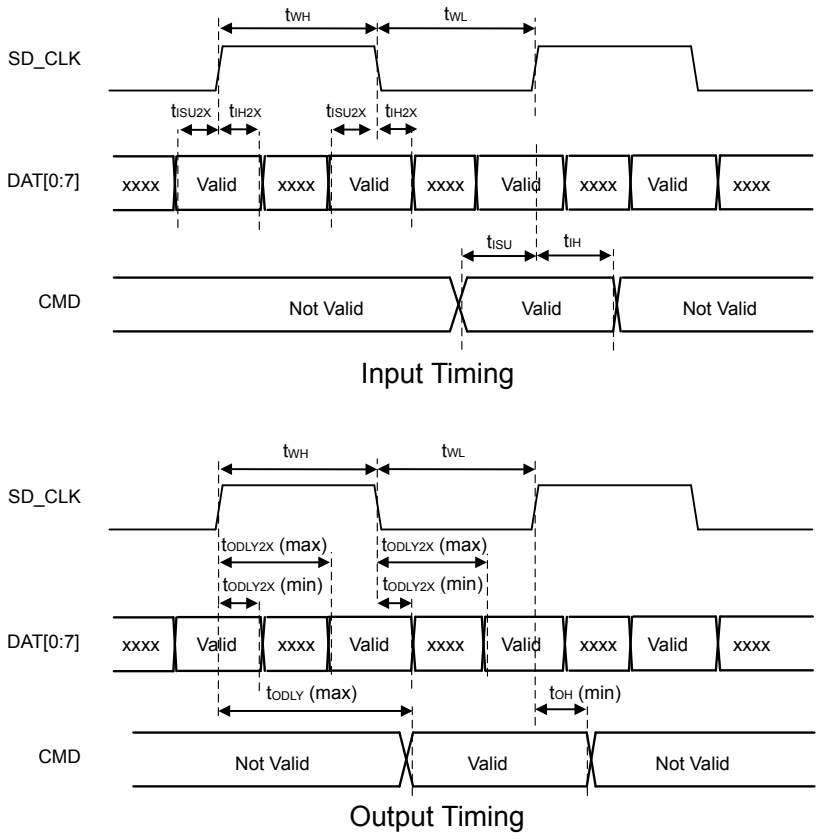

Figure 4.20. SDIO MMC DDR Mode Timing

4.1.28 Quad SPI (QSPI)

4.1.28.1 QSPI SDR Mode

QSPI SDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 23, RX DLL = 48, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.54. QSPI SDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Full SCLK period	T		$(1/F_{SCLK})$ * 0.95	—	—	ns
Output valid	t_{OV}		—	—	T/2 - 2.4	ns
Output hold	t_{OH}		T/2 - 32.9	—	—	ns
Input setup	t_{SU}		36.2 - T/2	—	—	ns
Input hold	t_H		T/2 - 3.3	—	—	ns

5.12 EFM32GG11B8xx in QFP64 Device Pinout

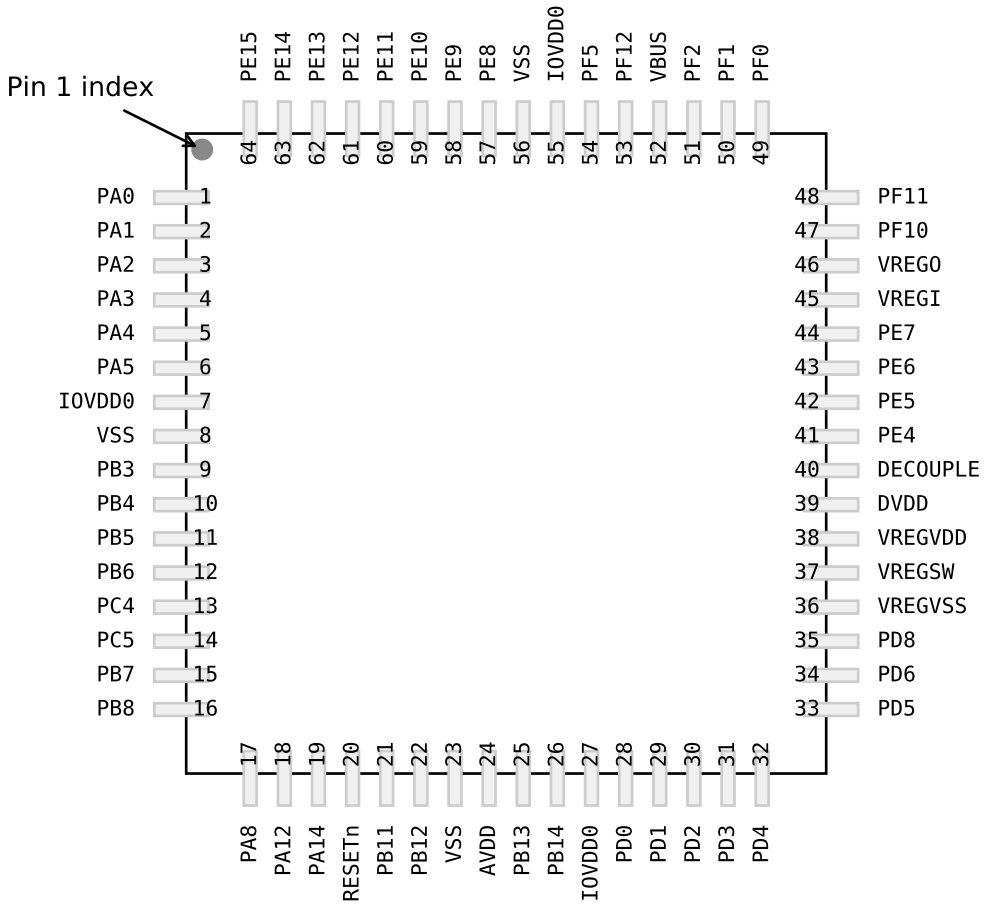

Figure 5.12. EFM32GG11B8xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.12. EFM32GG11B8xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

5.20 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 5.21 Alternate Functionality Overview for a list of GPIO locations available for each function.

Table 5.20. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PA15	BUSAY BUSBX LCD_SEG12	EBI_AD08 #0	TIM3_CC2 #0	ETH_MIIRXCLK #0 ETH_MDIO #3 US2_CLK #3	PRS_CH15 #0
PE15	BUSCY BUSDX LCD_SEG11	EBI_AD07 #0	TIM2_CDTI2 #2 TIM3_CC1 #0	ETH_RMIITXD0 #0 ETH_MIIRXD3 #0 SDIO_CMD #1 US0_RTS #0 QSPI0_DQS #1 LEU0_RX #2	PRS_CH14 #2 ETM_TD3 #4
PE14	BUSDY BUSCX LCD_SEG10	EBI_AD06 #0	TIM2_CDTI1 #2 TIM3_CC0 #0	ETH_RMIITXD1 #0 ETH_MIIRXD2 #0 SDIO_CLK #1 US0_CTS #0 QSPI0_SCLK #1 LEU0_TX #2	PRS_CH13 #2 ETM_TD2 #4
PE13	BUSCY BUSDX LCD_SEG9	EBI_AD05 #0	TIM1_CC3 #1 TIM2_CC2 #3 LE-TIM0_OUT1 #4	SDIO_CLK #0 ETH_MIIRXD1 #0 US0_TX #3 US0_CS #0 U1_RX #4 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 ETM_TD1 #4 GPIO_EM4WU5
PE12	BUSDY BUSCX LCD_SEG8	EBI_AD04 #0	TIM1_CC2 #1 TIM2_CC1 #3 WTIM0_CDTI2 #0 LETIM0_OUT0 #4	SDIO_CMD #0 ETH_MIIRXD0 #0 US0_RX #3 US0_CLK #0 U1_TX #4 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_ALTEX6 PRS_CH1 #3 ETM_TD0 #4
PE11	BUSCY BUSDX LCD_SEG7	EBI_AD03 #0 EBI_CS3 #4	TIM1_CC1 #1 TIM4_CC2 #7 WTIM0_CDTI1 #0	SDIO_DAT0 #0 QSPI0_DQ7 #0 ETH_MIIRXDV #0 US0_RX #0	LES_ALTEX5 PRS_CH3 #2 ETM_TCLK #4
PE10	BUSDY BUSCX LCD_SEG6	EBI_AD02 #0 EBI_CS2 #4	TIM1_CC0 #1 TIM4_CC1 #7 WTIM0_CDTI0 #0	SDIO_DAT1 #0 QSPI0_DQ6 #0 ETH_MIIRXER #0 US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9
PE9	BUSCY BUSDX LCD_SEG5	EBI_AD01 #0 EBI_CS1 #4	TIM4_CC0 #7 PCNT2_S1IN #1	SDIO_DAT2 #0 QSPI0_DQ5 #0 US5_RX #0	PRS_CH8 #2
PE8	BUSDY BUSCX LCD_SEG4	EBI_AD00 #0 EBI_CS0 #4	TIM2_CDTI0 #2 TIM4_CC2 #6 PCNT2_S0IN #1	SDIO_DAT3 #0 QSPI0_DQ4 #0 US5_TX #0 I2C2_SDA #0	PRS_CH3 #1
PI9		EBI_A14 #2	TIM1_CC3 #7 TIM4_CC1 #3	US4_CS #3	
PI6		EBI_A11 #2	TIM1_CC0 #7 TIM4_CC1 #2 WTIM3_CC0 #5	US4_TX #3	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD4	BUSADC0Y BUSADC0X OPA2_P	EBI_A08 #1 EBI_A17 #3	TIM6_CC0 #7 WTIM0_CDTI0 #4 WTIM1_CC2 #1 WTIM2_CC1 #5	CAN1_TX #2 US1_CTS #1 US3_CLK #2 LEU0_TX #0 I2C1_SDA #3	CMU_CLKI0 #0 PRS_CH10 #2 ETM_TD2 #0 ETM_TD2 #2
PC0	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSACMP0Y BUSACMP0X	EBI_AD07 #1 EBI_CS0 #2 EBI_REn #3 EBI_A23 #0	TIM0_CC1 #3 TIM2_CC1 #4 PCNT0_S0IN #2	ETH_MDIO #2 CAN0_RX #0 US0_TX #5 US1_TX #0 US1_CS #4 US2_RTS #0 US3_CS #3 I2C0_SDA #4	LES_CH0 PRS_CH2 #0
PC1	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSACMP0Y BUSACMP0X	EBI_AD08 #1 EBI_CS1 #2 EBI_BL0 #3 EBI_A24 #0	TIM0_CC2 #3 TIM2_CC2 #4 WTIM0_CC0 #7 PCNT0_S1IN #2	ETH_MDC #2 CAN0_TX #0 US0_RX #5 US1_TX #4 US1_RX #0 US2_CTS #0 US3_RTS #1 I2C0_SCL #4	LES_CH1 PRS_CH3 #0
PC2	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSACMP0Y BUSACMP0X	EBI_AD09 #1 EBI_CS2 #2 EBI_NANDWEn #3 EBI_A25 #0	TIM0_CDTI0 #3 TIM2_CC0 #5 WTIM0_CC1 #7 LETIM1_OUT0 #3	ETH_TSUEXTCLK #2 CAN1_RX #0 US1_RX #4 US2_TX #0	LES_CH2 PRS_CH10 #1
PA8	BUSBY BUSAX LCD_SEG36	EBI_AD14 #1 EBI_A02 #3 EBI_DCLK #0	TIM2_CC0 #0 TIM0_CC0 #6 LETIM0_OUT0 #6 PCNT1_S1IN #4	US2_RX #2 US4_RTS #0	PRS_CH8 #0
PA11	BUSAY BUSBX LCD_SEG39	EBI_CS1 #1 EBI_A05 #3 EBI_HSNC #0	WTIM2_CC2 #0 LETIM1_OUT0 #1	US2_CTS #2	PRS_CH11 #0
PA13	BUSAY BUSBX	EBI_WEn #1 EBI_NANDWEn #2 EBI_A01 #0 EBI_A07 #3	TIM0_CC2 #7 TIM2_CC1 #1 WTIM0_CDTI1 #2 WTIM2_CC1 #1 LETIM1_OUT1 #1 PCNT1_S1IN #5	CAN1_TX #5 US0_CS #5 US2_TX #3	PRS_CH13 #0
PB9	BUSAY BUSBX	EBI_ALE #1 EBI_NANDREn #2 EBI_A00 #1 EBI_A03 #0 EBI_A09 #3	WTIM2_CC0 #2 LETIM0_OUT0 #7	SDIO_WP #3 CAN0_RX #3 US1_CTS #0 U1_TX #2	PRS_CH13 #1 ACMP1_O #5
PB12	BUSBY BUSAX VDAC0_OUT1 / OPA1_OUT	EBI_A03 #1 EBI_A12 #3 EBI_CSTFT #2	TIM1_CC3 #3 WTIM2_CC0 #3 LETIM0_OUT1 #1 PCNT0_S0IN #7 PCNT1_S1IN #6	US2_CTS #1 US5_RTS #0 U1_RTS #2 I2C1_SCL #1	PRS_CH16 #1
PH2	BUSADC1Y BUSADC1X	EBI_VSNC #2	TIM6_CC0 #3	US1_CTS #6	
PH5	BUSADC1Y BUSADC1X	EBI_A17 #2	TIM6_CDTI0 #3 WTIM2_CC1 #6	US4_RX #4	
PH8	BUSACMP3Y BUSACMP3X	EBI_A20 #2	TIM6_CC0 #4 WTIM1_CC0 #6 WTIM2_CC1 #7	US4_CTS #4	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PH11	BUSACMP3Y BUSACMP3X	EBI_A23 #2	TIM5_CC1 #1 WTIM1_CC3 #6	US5_RX #3 U1_TX #5 I2C1_SDA #5	
PH13	BUSACMP3Y BUSACMP3X	EBI_A25 #2	TIM5_CC0 #2 WTIM1_CC1 #7 PCNT2_S1IN #7	US5_CS #3 U1_CTS #5 I2C1_SDA #6	
PD0	VDAC0_OUT0ALT / OPA0_OUTALT #4 OPA2_OUTALT BUSADC0Y BUSADC0X	EBI_A04 #1 EBI_A13 #3	TIM4_CDTI0 TIM6_CC2 #5 WTIM1_CC2 #0 PCNT2_S0IN #0	CAN0_RX #2 US1_TX #1	
PD3	BUSADC0Y BUSADC0X OPA2_N	EBI_A07 #1 EBI_A16 #3	TIM4_CDTI2 TIM0_CC2 #2 TIM6_CC2 #6 WTIM1_CC1 #1 WTIM2_CC0 #5	CAN1_RX #2 US1_CS #1 LEU1_RX #2	ETM_TD1 #0 ETM_TD1 #2
PD8	BU_VIN	EBI_A12 #1	WTIM1_CC2 #2	US2_RTS #5	CMU_CLK1 #1 PRS_CH12 #2 ACMP2_O #0
PB7	LFXTAL_P		TIM0_CDTI0 #4 TIM1_CC0 #3	US0_TX #4 US1_CLK #0 US3_RX #2 US4_TX #0 U0_CTS #4	PRS_CH22 #0
PC3	VDAC0_OUT0ALT / OPA0_OUTALT #3 BUSACMP0Y BUSACMP0X	EBI_AD10 #1 EBI_CS3 #2 EBI_BL1 #3 EBI_NANDREn #0	TIM0_CDTI1 #3 TIM2_CC1 #5 WTIM0_CC2 #7 LETIM1_OUT1 #3	ETH_TSUTMRTOG #2 CAN1_TX #0 US1_CLK #4 US2_RX #0	LES_CH3 PRS_CH11 #1
PC5	BUSACMP0Y BUSACMP0X OPA0_N	EBI_AD12 #1 EBI_WEn #2 EBI_NANDWEn #0 EBI_A00 #3	TIM0_CC1 #5 LETIM0_OUT1 #3 PCNT1_S1IN #3	SDIO_WP #1 US2_CS #0 US4_CS #0 U0_RX #4 U1_RTS #4 I2C1_SCL #0	LES_CH5 PRS_CH19 #2
PA9	BUSAY BUSBX LCD_SEG37	EBI_AD15 #1 EBI_A03 #3 EBI_DTEN #0	TIM2_CC1 #0 TIM0_CC1 #6 WTIM2_CC0 #0 LETIM0_OUT1 #6	US2_CLK #2	PRS_CH9 #0
PB10	BUSBY BUSAX	EBI_BL0 #2 EBI_A01 #1 EBI_A04 #0 EBI_A10 #3	WTIM2_CC1 #2 LETIM0_OUT1 #7	SDIO_CD #3 CAN0_TX #3 US1_RTS #0 US2_CTS #3 U1_RX #2	PRS_CH9 #2 ACMP1_O #6
PH0	BUSADC1Y BUSADC1X	EBI_DCLK #2	WTIM2_CC2 #4	US0_CTS #6 LEU1_TX #5	
PH3	BUSADC1Y BUSADC1X	EBI_HSNC #2	TIM6_CC1 #3	US1_RTS #6	
PH6	BUSADC1Y BUSADC1X	EBI_A18 #2	TIM6_CDTI1 #3 WTIM2_CC2 #6	US4_CLK #4	
PH9	BUSACMP3Y BUSACMP3X	EBI_A21 #2	TIM6_CC1 #4 WTIM1_CC1 #6 WTIM2_CC2 #7	US4_RTS #4	
PH12	BUSACMP3Y BUSACMP3X	EBI_A24 #2	TIM5_CC2 #1 WTIM1_CC0 #7	US5_CLK #3 U1_RX #5 I2C1_SCL #5	

5.21 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 5.20 GPIO Functionality Table for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.21. Alternate Functionality Overview

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ACMP0_O	0: PE13 1: PE2 2: PD6 3: PB11	4: PA6 5: PB0 6: PB2 7: PB3	Analog comparator ACMP0, digital output.
ACMP1_O	0: PF2 1: PE3 2: PD7 3: PA12	4: PA14 5: PB9 6: PB10 7: PA5	Analog comparator ACMP1, digital output.
ACMP2_O	0: PD8 1: PE0 2: PE1 3: PI0	4: PI1 5: PI2	Analog comparator ACMP2, digital output.
ACMP3_O	0: PF0 1: PC15 2: PC14 3: PC13	4: PI4 5: PI5	Analog comparator ACMP3, digital output.
ADC0_EXTN	0: PD7		Analog to digital converter ADC0 external reference input negative pin.
ADC0_EXTP	0: PD6		Analog to digital converter ADC0 external reference input positive pin.
ADC1_EXTN	0: PD7		Analog to digital converter ADC1 external reference input negative pin.
ADC1_EXTP	0: PD6		Analog to digital converter ADC1 external reference input positive pin.
BOOT_RX	0: PF1		Bootloader RX.
BOOT_TX	0: PF0		Bootloader TX.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_TSUTMR-TOG	0: PB6 1: PB15 2: PC3 3: PF9		Ethernet IEEE1588 Timer Toggle.
ETM_TCLK	0: PD7 1: PF8 2: PC6 3: PA6	4: PE11 5: PG15	Embedded Trace Module ETM clock .
ETM_TD0	0: PD6 1: PF9 2: PC7 3: PA2	4: PE12 5: PG14	Embedded Trace Module ETM data 0.
ETM_TD1	0: PD3 1: PD13 2: PD3 3: PA3	4: PE13 5: PG13	Embedded Trace Module ETM data 1.
ETM_TD2	0: PD4 1: PB15 2: PD4 3: PA4	4: PE14 5: PG12	Embedded Trace Module ETM data 2.
ETM_TD3	0: PD5 1: PF3 2: PD5 3: PA5	4: PE15 5: PG11	Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU5	0: PE13		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
QSPI0_DQ7	0: PE11 1: PB6 2: PG8		Quad SPI 0 Data 7.
QSPI0_DQS	0: PF9 1: PE15 2: PG11		Quad SPI 0 Data S.
QSPI0_SCLK	0: PF6 1: PE14 2: PG0		Quad SPI 0 Serial Clock.
SDIO_CD	0: PF8 1: PC4 2: PA6 3: PB10		SDIO Card Detect.
SDIO_CLK	0: PE13 1: PE14		SDIO Serial Clock.
SDIO_CMD	0: PE12 1: PE15		SDIO Command.
SDIO_DAT0	0: PE11 1: PA0		SDIO Data 0.
SDIO_DAT1	0: PE10 1: PA1		SDIO Data 1.
SDIO_DAT2	0: PE9 1: PA2		SDIO Data 2.
SDIO_DAT3	0: PE8 1: PA3		SDIO Data 3.
SDIO_DAT4	0: PD12 1: PA4		SDIO Data 4.
SDIO_DAT5	0: PD11 1: PA5		SDIO Data 5.
SDIO_DAT6	0: PD10 1: PB3		SDIO Data 6.

7. BGA152 Package Specifications

7.1 BGA152 Package Dimensions

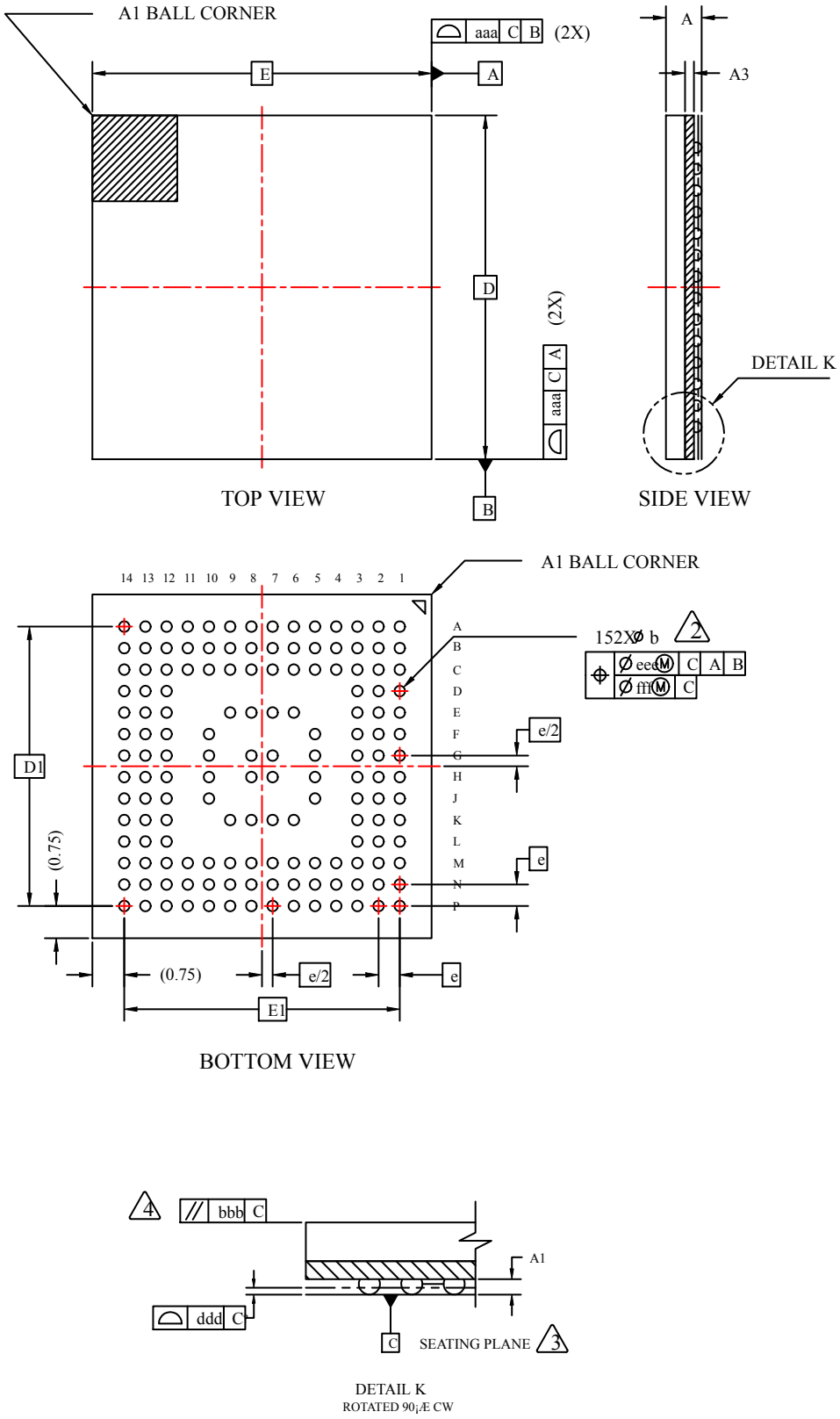

Figure 7.1. BGA152 Package Drawing

Table 9.1. BGA112 Package Dimensions

Dimension	Min	Typ	Max
A	-	-	1.30
A1	0.55	0.60	0.65
A2		0.21 BSC	
A3	0.30	0.35	0.40
d	0.43	0.48	0.53
D		10.00 BSC	
D1		8.00 BSC	
E		10.00 BSC	
E1		8.00 BSC	
e1		0.80 BSC	
e2		0.80 BSC	
L1		1.00 REF	
L2		1.00 REF	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12.2 QFN64 PCB Land Pattern

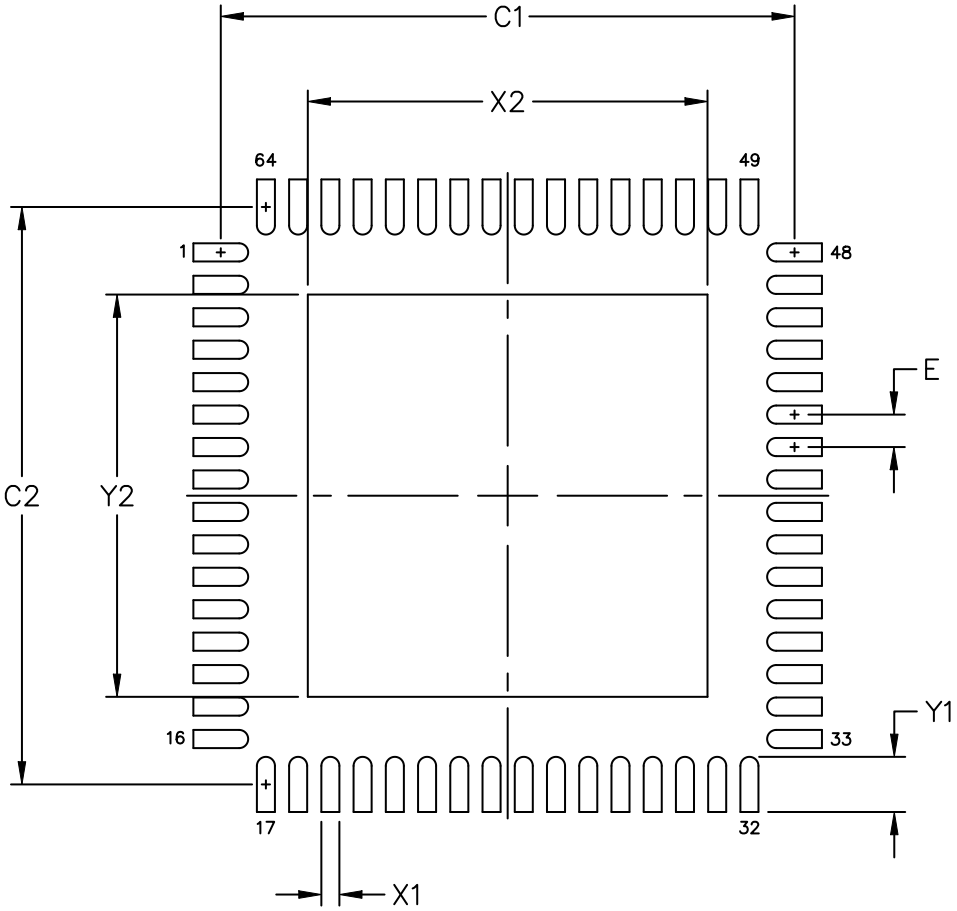

Figure 12.2. QFN64 PCB Land Pattern Drawing

Table 12.2. QFN64 PCB Land Pattern Dimensions

Dimension	Typ
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	7.30
Y2	7.30

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
8. A 3x3 array of 1.45 mm square openings on a 2.00 mm pitch can be used for the center ground pad.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.