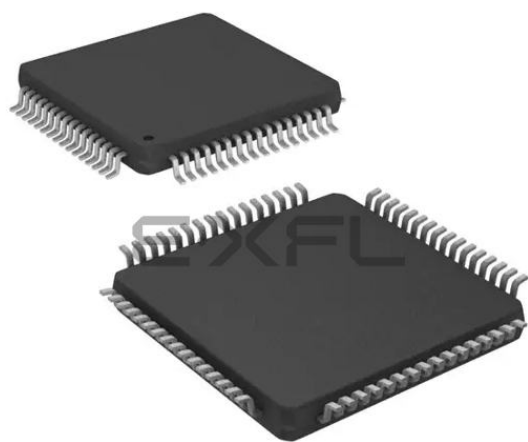




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b110f2048iq64-b

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4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD $\leq$ AVDD
- IOVDD $\leq$ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range ⁶	T_A	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage ²	V_{AVDD}		1.8	3.3	3.8	V
VREGVDD operating supply voltage ^{2 1}	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	$I_{VREGVDD}$	DCDC in bypass, $T \leq 85^\circ\text{C}$	—	—	200	mA
		DCDC in bypass, $T > 85^\circ\text{C}$	—	—	100	mA
DVDD operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage	V_{IOVDD}	All IOVDD pins ⁵	1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor ^{3 4}	$C_{DECOUPLE}$		0.75	1.0	2.75	μF
HFCORECLK frequency	f_{CORE}	VSCALE2, MODE = WS3	—	—	72	MHz
		VSCALE2, MODE = WS2	—	—	54	MHz
		VSCALE2, MODE = WS1	—	—	36	MHz
		VSCALE2, MODE = WS0	—	—	18	MHz
		VSCALE0, MODE = WS2	—	—	20	MHz
		VSCALE0, MODE = WS1	—	—	14	MHz
		VSCALE0, MODE = WS0	—	—	7	MHz
HFCLK frequency	f_{HFCLK}	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFSRCCLK frequency	$f_{HFSRCCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFBUSCLK frequency	$f_{HFBUSCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERCLK frequency	$f_{HFPERCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERBCLK frequency	$f_{HFPERBCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFPERCCLK frequency	$f_{HFPERCCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4H mode, with voltage scaling enabled	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.94	—	μA
		128 byte RAM retention, CRYO-TIMER running from ULFRCO	—	0.62	—	μA
		128 byte RAM retention, no RTCC	—	0.62	—	μA
Current consumption in EM4S mode	I _{EM4S}	No RAM retention, no RTCC	—	0.13	—	μA
Current consumption of peripheral power domain 1, with voltage scaling enabled, DCDC in LP mode ³	I _{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled ⁴	—	0.68	—	μA
Current consumption of peripheral power domain 2, with voltage scaling enabled, DCDC in LP mode ³	I _{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled ⁴	—	0.28	—	μA

Note:

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.2.4 EM2 and EM3 Power Domains](#) for a list of the peripherals in each power domain.
5. CMU_LFRCCOCTRL_ENVREF = 1, CMU_LFRCCOCTRL_VREFUPDATE = 1

4.1.11 Flash Memory Characteristics⁵

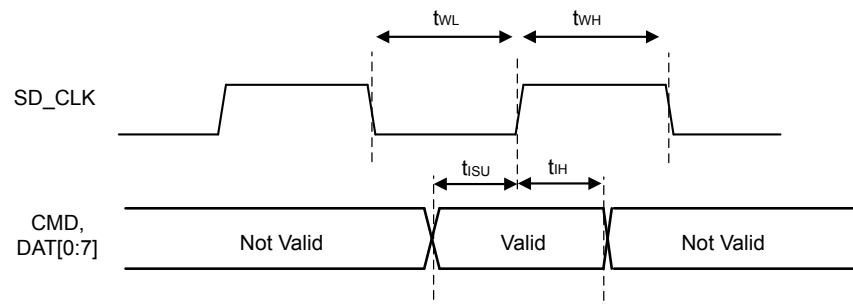
Table 4.19. Flash Memory Characteristics⁵

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC _{FLASH}		10000	—	—	cycles
Flash data retention	RET _{FLASH}	T ≤ 85 °C	10	—	—	years
		T ≤ 125 °C	10	—	—	years
Word (32-bit) programming time	t _{W_PROG}	Burst write, 128 words, average time per word	20	26.2	32	μs
		Single word	59	68.7	83	μs
Page erase time ⁴	t _{PERASE}		20	26.8	35	ms
Mass erase time ¹	t _{MERASE}		20	26.9	35	ms
Device erase time ^{2 3}	t _{DERASE}	T ≤ 85 °C	—	80.7	95	ms
		T ≤ 125 °C	—	80.7	100	ms
Erase current ⁶	I _{ERASE}	Page Erase	—	—	1.7	mA
		Mass or Device Erase	—	—	2.1	mA
Write current ⁶	I _{WRITE}		—	—	3.9	mA
Supply voltage during flash erase and write	V _{FLASH}		1.62	—	3.6	V

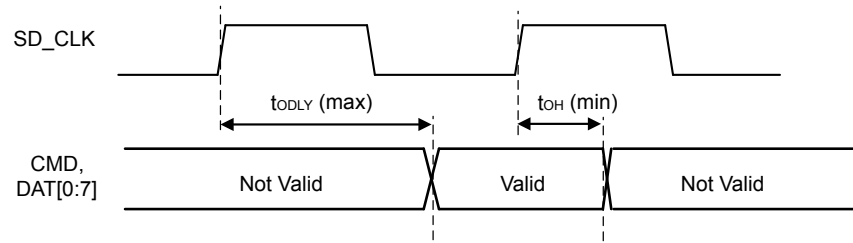
Note:

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
4. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
5. Flash data retention information is published in the Quarterly Quality and Reliability Report.
6. Measured at 25 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz	SNDR _{DAC}	500 ksps, single-ended, internal 1.25V reference	—	60.4	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	61.6	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	63.3	—	dB
		500 ksps, differential, internal 2.5V reference	—	64.4	—	dB
		500 ksps, differential, 3.3V VDD reference	—	65.8	—	dB
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz	SNDR _{DAC_BAND}	500 ksps, single-ended, internal 1.25V reference	—	65.3	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	66.7	—	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	—	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	—	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0	—	dB
Total harmonic distortion	THD		—	70.2	—	dB
Differential non-linearity ³	DNL _{DAC}		TBD	—	TBD	LSB
Integral non-linearity	INL _{DAC}		TBD	—	TBD	LSB
Offset error ⁵	V _{OFFSET}	T = 25 °C	TBD	—	TBD	mV
		Across operating temperature range	TBD	—	TBD	mV
Gain error ⁵	V _{GAIN}	T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	TBD	—	TBD	%
		Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	TBD	—	TBD	%
External load capacitance, OUTSCALE=0	C _{LOAD}		—	—	75	pF



Input Timing



Output Timing

Figure 4.18. SDIO MMC SDR Mode Timing

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF13	B9	GPIO (5V)
PF4	B10	GPIO	PF3	B11	GPIO
VBUS	B12	USB VBUS signal and auxiliary input to 5 V regulator.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 L12 L15	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L16	Digital IO power supply 0.
PF2	C10	GPIO	PF1	C11	GPIO (5V)
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PF0	D11	GPIO (5V)
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PC9	E11	GPIO (5V)
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE6	F11	GPIO
PE7	F12	GPIO	PC8	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE3	G11	GPIO
PE4	G12	GPIO	PE5	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
DECOUPLE	H13	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PD14	J1	GPIO (5V)
PD15	J2	GPIO (5V)	PE1	J12	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PD8	H8	GPIO	PD5	H9	GPIO
PD6	H10	GPIO	PD7	H11	GPIO
PC1	J1	GPIO (5V)	PC3	J2	GPIO (5V)
PD15	J3	GPIO (5V)	PA12	J4	GPIO (5V)
PA9	J5	GPIO	PA10	J6	GPIO
PB9	J7	GPIO (5V)	PB10	J8	GPIO (5V)
PD2	J9	GPIO (5V)	PD3	J10	GPIO
PD4	J11	GPIO	PB7	K1	GPIO
PC4	K2	GPIO	PA13	K3	GPIO (5V)
PA11	K5	GPIO	RESETn	K6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	K8 K9 L10	Analog power supply.	PD1	K11	GPIO
PB8	L1	GPIO	PC5	L2	GPIO
PA14	L3	GPIO	PB11	L5	GPIO
PB12	L6	GPIO	PB13	L8	GPIO
PB14	L9	GPIO	PD0	L11	GPIO (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.19 EFM32GG11B1xx in QFN64 Device Pinout

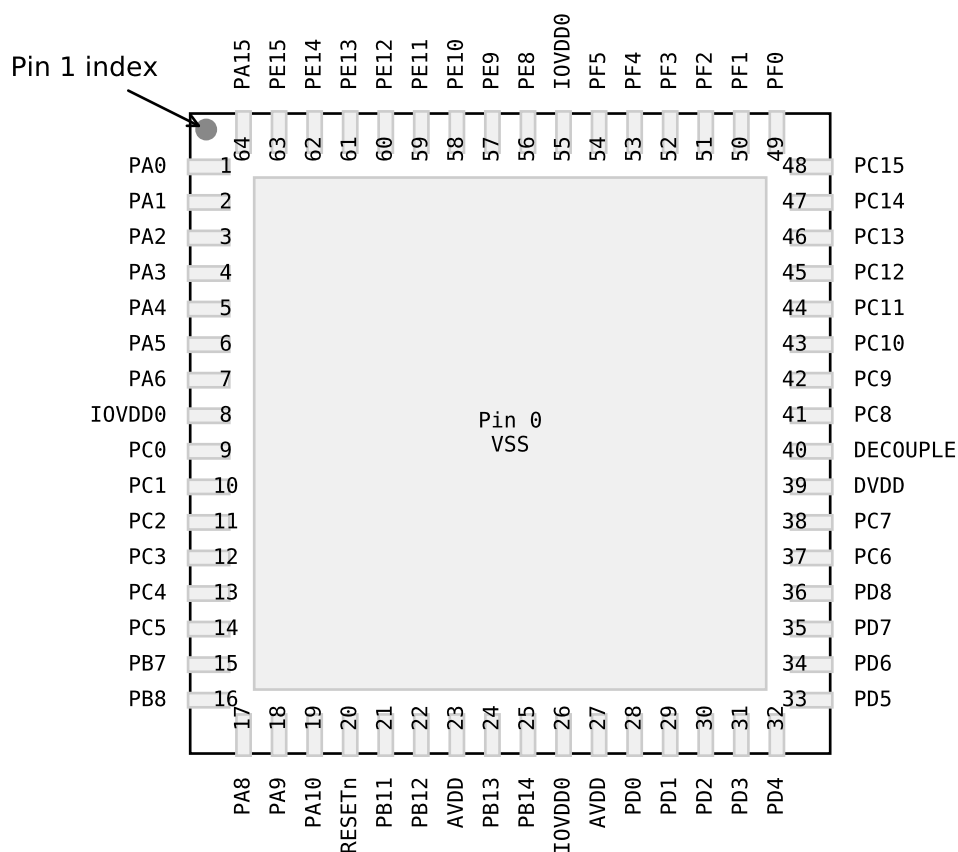


Figure 5.19. EFM32GG11B1xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.19. EFM32GG11B1xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PC0	9	GPIO (5V)
PC1	10	GPIO (5V)	PC2	11	GPIO (5V)

5.20 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to [5.21 Alternate Functionality Overview](#) for a list of GPIO locations available for each function.

Table 5.20. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PA15	BUSAY BUSBX LCD_SEG12	EBI_AD08 #0	TIM3_CC2 #0	ETH_MIIRXCLK #0 ETH_MDIO #3 US2_CLK #3	PRS_CH15 #0
PE15	BUSCY BUSDX LCD_SEG11	EBI_AD07 #0	TIM2_CDTI2 #2 TIM3_CC1 #0	ETH_RMIITXD0 #0 ETH_MIIRXD3 #0 SDIO_CMD #1 US0_RTS #0 QSPI0_DQS #1 LEU0_RX #2	PRS_CH14 #2 ETM_TD3 #4
PE14	BUSDY BUSCX LCD_SEG10	EBI_AD06 #0	TIM2_CDTI1 #2 TIM3_CC0 #0	ETH_RMIITXD1 #0 ETH_MIIRXD2 #0 SDIO_CLK #1 US0_CTS #0 QSPI0_SCLK #1 LEU0_TX #2	PRS_CH13 #2 ETM_TD2 #4
PE13	BUSCY BUSDX LCD_SEG9	EBI_AD05 #0	TIM1_CC3 #1 TIM2_CC2 #3 LE- TIM0_OUT1 #4	SDIO_CLK #0 ETH_MIIRXD1 #0 US0_TX #3 US0_CS #0 U1_RX #4 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 ETM_TD1 #4 GPIO_EM4WU5
PE12	BUSDY BUSCX LCD_SEG8	EBI_AD04 #0	TIM1_CC2 #1 TIM2_CC1 #3 WTIM0_CDTI2 #0 LETIM0_OUT0 #4	SDIO_CMD #0 ETH_MIIRXD0 #0 US0_RX #3 US0_CLK #0 U1_TX #4 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_ALTEX6 PRS_CH1 #3 ETM_TD0 #4
PE11	BUSCY BUSDX LCD_SEG7	EBI_AD03 #0 EBI_CS3 #4	TIM1_CC1 #1 TIM4_CC2 #7 WTIM0_CDTI1 #0	SDIO_DAT0 #0 QSPI0_DQ7 #0 ETH_MIIRXDV #0 US0_RX #0	LES_ALTEX5 PRS_CH3 #2 ETM_TCLK #4
PE10	BUSDY BUSCX LCD_SEG6	EBI_AD02 #0 EBI_CS2 #4	TIM1_CC0 #1 TIM4_CC1 #7 WTIM0_CDTI0 #0	SDIO_DAT1 #0 QSPI0_DQ6 #0 ETH_MIIRXER #0 US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9
PE9	BUSCY BUSDX LCD_SEG5	EBI_AD01 #0 EBI_CS1 #4	TIM4_CC0 #7 PCNT2_S1IN #1	SDIO_DAT2 #0 QSPI0_DQ5 #0 US5_RX #0	PRS_CH8 #2
PE8	BUSDY BUSCX LCD_SEG4	EBI_AD00 #0 EBI_CS0 #4	TIM2_CDTI0 #2 TIM4_CC2 #6 PCNT2_S0IN #1	SDIO_DAT3 #0 QSPI0_DQ4 #0 US5_TX #0 I2C2_SDA #0	PRS_CH3 #1
PI9		EBI_A14 #2	TIM1_CC3 #7 TIM4_CC1 #3	US4_CS #3	
PI6		EBI_A11 #2	TIM1_CC0 #7 TIM4_CC1 #2 WTIM3_CC0 #5	US4_TX #3	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PB0	BUSBY BUSAX LCD_SEG32	EBI_AD00 #1 EBI_CS0 #3 EBI_A16 #0	TIM2_CDTI0 #0 TIM1_CC0 #2 TIM3_CC2 #7 WTIM0_CC0 #5 PCNT0_S0IN #5 PCNT1_S1IN #2	LEU1_TX #3	PRS_CH4 #1 ACMP0_O #5
PE0	BUSDY BUSCX	EBI_A00 #2 EBI_A07 #0	TIM3_CC0 #1 WTIM1_CC1 #3 PCNT0_S0IN #1	CAN0_RX #6 U0_TX #1 I2C1_SDA #2	PRS_CH22 #1 ACMP2_O #1
PC7	BUSACMP0Y BU- SACMP0X OPA3_N	EBI_A06 #0 EBI_A13 #1 EBI_A21 #3	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 LEU1_RX #0 I2C0_SCL #2	LES_CH7 PRS_CH15 #1 ETM_TD0 #2
PB1	BUSAY BUSBX LCD_SEG33	EBI_AD01 #1 EBI_CS1 #3 EBI_A17 #0	TIM2_CDTI1 #0 TIM1_CC1 #2 WTIM0_CC1 #5 LE- TIM1_OUT1 #5 PCNT0_S1IN #5	ETH_MIICRS #0 US5_RX #2 LEU1_RX #3	PRS_CH5 #1
PB2	BUSBY BUSAX LCD_SEG34	EBI_AD02 #1 EBI_CS2 #3 EBI_A18 #0	TIM2_CDTI2 #0 TIM1_CC2 #2 WTIM0_CC2 #5 LE- TIM1_OUT0 #5	ETH_MIICOL #0 US1_CS #6	PRS_CH18 #0 ACMP0_O #6
PB3	BUSAY BUSBX LCD_SEG20 / LCD_COM4	EBI_AD03 #1 EBI_CS3 #3 EBI_A19 #0	TIM1_CC3 #2 WTIM0_CC0 #6 PCNT1_S0IN #1	ETH_MIICRS #2 ETH_MDIO #0 SDIO_DAT6 #1 US2_TX #1 US3_TX #2 QSPI0_DQ4 #1	PRS_CH19 #0 ACMP0_O #7
PC6	BUSACMP0Y BU- SACMP0X OPA3_P	EBI_A05 #0	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 LEU1_TX #0 I2C0_SDA #2	LES_CH6 PRS_CH14 #1 ETM_TCLK #2
PB4	BUSBY BUSAX LCD_SEG21 / LCD_COM5	EBI_AD04 #1 EBI_ARDY #3 EBI_A20 #0	WTIM0_CC1 #6 PCNT1_S1IN #1	ETH_MIICOL #2 ETH_MDC #0 SDIO_DAT7 #1 US2_RX #1 QSPI0_DQ5 #1 LEU1_TX #4	PRS_CH20 #0
PB5	BUSAY BUSBX LCD_SEG22 / LCD_COM6	EBI_AD05 #1 EBI_ALE #3 EBI_A21 #0	WTIM0_CC2 #6 LE- TIM1_OUT0 #4 PCNT0_S0IN #6	ETH_TSUEXTCLK #0 US0_RTS #4 US2_CLK #1 QSPI0_DQ6 #1 LEU1_RX #4	PRS_CH21 #0
PB6	BUSBY BUSAX LCD_SEG23 / LCD_COM7	EBI_AD06 #1 EBI_WEn #3 EBI_A22 #0	TIM0_CC0 #3 TIM2_CC0 #4 WTIM3_CC0 #6 LE- TIM1_OUT1 #4 PCNT0_S1IN #6	ETH_TSUTMRTOG #0 US0_CTS #4 US2_CS #1 QSPI0_DQ7 #1	PRS_CH12 #1
PD5	BUSADC0Y BU- SADC0X OPA2_OUT	EBI_A09 #1 EBI_A18 #3	TIM6_CC1 #7 WTIM0_CDTI1 #4 WTIM1_CC3 #1 WTIM2_CC2 #5	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3	PRS_CH11 #2 ETM_TD3 #0 ETM_TD3 #2

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PF6		LCD segment line 24.
LCD_SEG25	0: PF7		LCD segment line 25.
LCD_SEG26	0: PF8		LCD segment line 26.
LCD_SEG27	0: PF9		LCD segment line 27.
LCD_SEG28	0: PD9		LCD segment line 28.
LCD_SEG29	0: PD10		LCD segment line 29.
LCD_SEG30	0: PD11		LCD segment line 30.
LCD_SEG31	0: PD12		LCD segment line 31.
LCD_SEG32	0: PB0		LCD segment line 32.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_CH11	0: PC11		LESENSE channel 11.
LES_CH12	0: PC12		LESENSE channel 12.
LES_CH13	0: PC13		LESENSE channel 13.
LES_CH14	0: PC14		LESENSE channel 14.
LES_CH15	0: PC15		LESENSE channel 15.
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4	4: PE12 5: PC14 6: PA8 7: PB9	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9 7: PB10	Low Energy Timer LETIM0, output channel 1.
LETIM1_OUT0	0: PA7 1: PA11 2: PA12 3: PC2	4: PB5 5: PB2 6: PG0 7: PG2	Low Energy Timer LETIM1, output channel 0.
LETIM1_OUT1	0: PA6 1: PA13 2: PA14 3: PC3	4: PB6 5: PB1 6: PG1 7: PG3	Low Energy Timer LETIM1, output channel 1.
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	0: PC7 1: PA6 2: PD3 3: PB1	4: PB5 5: PH1	LEUART1 Receive input.
LEU1_TX	0: PC6 1: PA5 2: PD2 3: PB0	4: PB4 5: PH0	LEUART1 Transmit output. Also used as receive input in half duplex communication.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
U0_TX	0: PF6 1: PE0 2: PA3 3: PC14	4: PC4 5: PF1 6: PD7	UART0 Transmit output. Also used as receive input in half duplex communication.
U1_CTS	0: PC14 1: PF9 2: PB11 3: PE4	4: PC4 5: PH13	UART1 Clear To Send hardware flow control input.
U1_RTS	0: PC15 1: PF8 2: PB12 3: PE5	4: PC5 5: PH14	UART1 Request To Send hardware flow control output.
U1_RX	0: PC13 1: PF11 2: PB10 3: PE3	4: PE13 5: PH12	UART1 Receive input.
U1_TX	0: PC12 1: PF10 2: PB9 3: PE2	4: PE12 5: PH11	UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	0: PE12 1: PE5 2: PC9 3: PC15	4: PB13 5: PA12 6: PG14	USART0 clock input / output.
US0_CS	0: PE13 1: PE4 2: PC8 3: PC14	4: PB14 5: PA13 6: PG15	USART0 chip select input / output.
US0_CTS	0: PE14 1: PE3 2: PC7 3: PC13	4: PB6 5: PB11 6: PH0	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PE15 1: PE2 2: PC6 3: PC12	4: PB5 5: PD6 6: PH1	USART0 Request To Send hardware flow control output.
US0_RX	0: PE11 1: PE6 2: PC10 3: PE12	4: PB8 5: PC1 6: PG13	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PE10 1: PE7 2: PC11 3: PE13	4: PB7 5: PC0 6: PG12	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PB7 1: PD2 2: PF0 3: PC15	4: PC3 5: PB11 6: PE5	USART1 clock input / output.
US1_CS	0: PB8 1: PD3 2: PF1 3: PC14	4: PC0 5: PE4 6: PB2	USART1 chip select input / output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM3_CC2	0: PD11 1: PC10 2: PC13 3: PF11	4: PI5 5: PF6 6: PF12 7: PF15	Wide timer 3 Capture Compare input / output channel 2.

Certain alternate function locations may have non-interference priority. These locations will take precedence over any other functions selected on that pin (i.e. another alternate function enabled to the same pin inadvertently).

Some alternate functions may also have high speed priority on certain locations. These locations ensure the fastest possible paths to the pins for timing-critical signals.

The following table lists the alternate functions and locations with special priority.

Table 5.22. Alternate Functionality Priority

Alternate Functionality	Location	Priority
CMU_CLK2	1: PA3 5: PD10	High Speed High Speed
CMU_CLKI0	1: PA3 5: PD10	High Speed High Speed
ETH_RMII CRS DV	0: PA4 1: PD11	High Speed High Speed
ETH_RMII REF CLK	0: PA3 1: PD10	High Speed High Speed
ETH_RMII RX D0	0: PA2 1: PD9	High Speed High Speed
ETH_RMII RX D1	0: PA1 1: PF9	High Speed High Speed
ETH_RMII RX ER	0: PA5 1: PD12	High Speed High Speed
ETH_RMII TX D0	0: PE15 1: PF7	High Speed High Speed
ETH_RMII TX D1	0: PE14 1: PF6	High Speed High Speed
ETH_RMII TX EN	0: PA0 1: PF8	High Speed High Speed
QSPI0_CS0	0: PF7	High Speed
QSPI0_CS1	0: PF8	High Speed
QSPI0_DQ0	0: PD9	High Speed
QSPI0_DQ1	0: PD10	High Speed
QSPI0_DQ2	0: PD11	High Speed
QSPI0_DQ3	0: PD12	High Speed
QSPI0_DQ4	0: PE8	High Speed
QSPI0_DQ5	0: PE9	High Speed
QSPI0_DQ6	0: PE10	High Speed
QSPI0_DQ7	0: PE11	High Speed

Table 5.27. ADC0 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSADC0Y	BUSADC0X	Bus
	PF15	PF15			PB15	PB15				CH31
PF14			PF14	PB14			PB14			CH30
	PF13	PF13			PB13	PB13				CH29
PF12			PF12	PB12			PB12			CH28
	PF11	PF11			PB11	PB11				CH27
PF10			PF10	PB10			PB10			CH26
	PF9	PF9			PB9	PB9				CH25
PF8			PF8							CH24
	PF7	PF7								CH23
PF6			PF6	PB6			PB6			CH22
	PF5	PF5			PB5	PB5				CH21
PF4			PF4	PB4			PB4			CH20
	PF3	PF3			PB3	PB3				CH19
PF2			PF2	PB2			PB2			CH18
	PF1	PF1			PB1	PB1				CH17
PF0			PF0	PB0			PB0			CH16
	PE15	PE15			PA15	PA15				CH15
PE14			PE14	PA14			PA14			CH14
	PE13	PE13			PA13	PA13				CH13
PE12			PE12	PA12			PA12			CH12
	PE11	PE11			PA11	PA11				CH11
PE10			PE10	PA10			PA10			CH10
	PE9	PE9			PA9	PA9				CH9
PE8			PE8	PA8			PA8			CH8
	PE7	PE7			PA7	PA7		PD7	PD7	CH7
PE6			PE6	PA6			PA6	PD6	PD6	CH6
	PE5	PE5			PA5	PA5		PD5	PD5	CH5
PE4			PE4	PA4			PA4	PD4	PD4	CH4
					PA3	PA3		PD3	PD3	CH3
				PA2			PA2	PD2	PD2	CH2
	PE1	PE1			PA1	PA1		PD1	PD1	CH1
PE0			PE0	PA0			PA0	PD0	PD0	CH0

Table 5.29. CSEN Bus and Pin Mapping

Port	CEXT																																			
	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0			
	BUSCY	BUSCX	BUSAY	BUSAX	PF15	PF14	PF13	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
	BUSBY	BUSBX	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0		
CEXT_SENSE																																				
APORT4Y	APORT4X	APORT2Y	APORT2X																																	
BUSDY	BUSDX	BUSBY	BUSBX																																	
	PF15		PB15																																	
PF14		PB14																																		
	PF13		PB13																																	
PF12		PB12																																		
	PF11		PB11																																	
PF10		PB10																																		
	PF9		PB9																																	
PF8																																				
	PF7																																			
PF6		PB6																																		
	PF5		PB5																																	
PF4		PB4																																		
	PF3		PB3																																	
PF2		PB2																																		
	PF1		PB1																																	
PF0		PB0																																		
	PE15		PA15																																	
PE14		PA14																																		
	PE13		PA13																																	
PE12		PA12																																		
	PE11		PA11																																	
PE10		PA10																																		
	PE9		PA9																																	
PE8		PA8																																		
	PE7		PA7																																	
PE6		PA6																																		
	PE5		PA5																																	
PE4		PA4																																		
			PA3																																	
		PA2																																		
	PE1		PA1																																	
PE0		PA0																																		

Table 5.30. IDAC0 Bus and Pin Mapping

APORT1Y	APORT1X	Port
BUSCY	BUSCX	Bus
PF15		CH31
	PF14	CH30
PF13		CH29
	PF12	CH28
PF11		CH27
	PF10	CH26
PF9		CH25
	PF8	CH24
PF7		CH23
	PF6	CH22
PF5		CH21
	PF4	CH20
PF3		CH19
	PF2	CH18
PF1		CH17
	PF0	CH16
PE15		CH15
	PE14	CH14
PE13		CH13
	PE12	CH12
PE11		CH11
	PE10	CH10
PE9		CH9
	PE8	CH8
PE7		CH7
	PE6	CH6
PE5		CH5
	PE4	CH4
		CH3
		CH2
PE1		CH1
	PE0	CH0

Table 6.1. BGA192 Package Dimensions

Dimension	Min	Typ	Max
A	0.77	0.83	0.89
A1	0.13	0.18	0.23
A3	0.16	0.20	0.24
A2	0.45 REF		
D	7.00 BSC		
e	0.40 BSC		
E	7.00 BSC		
D1	6.00 BSC		
E1	6.00 BSC		
b	0.20	0.25	0.30
aaa	0.10		
bbb	0.10		
ddd	0.08		
eee	0.15		
fff	0.05		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. TQFP64 Package Specifications

11.1 TQFP64 Package Dimensions

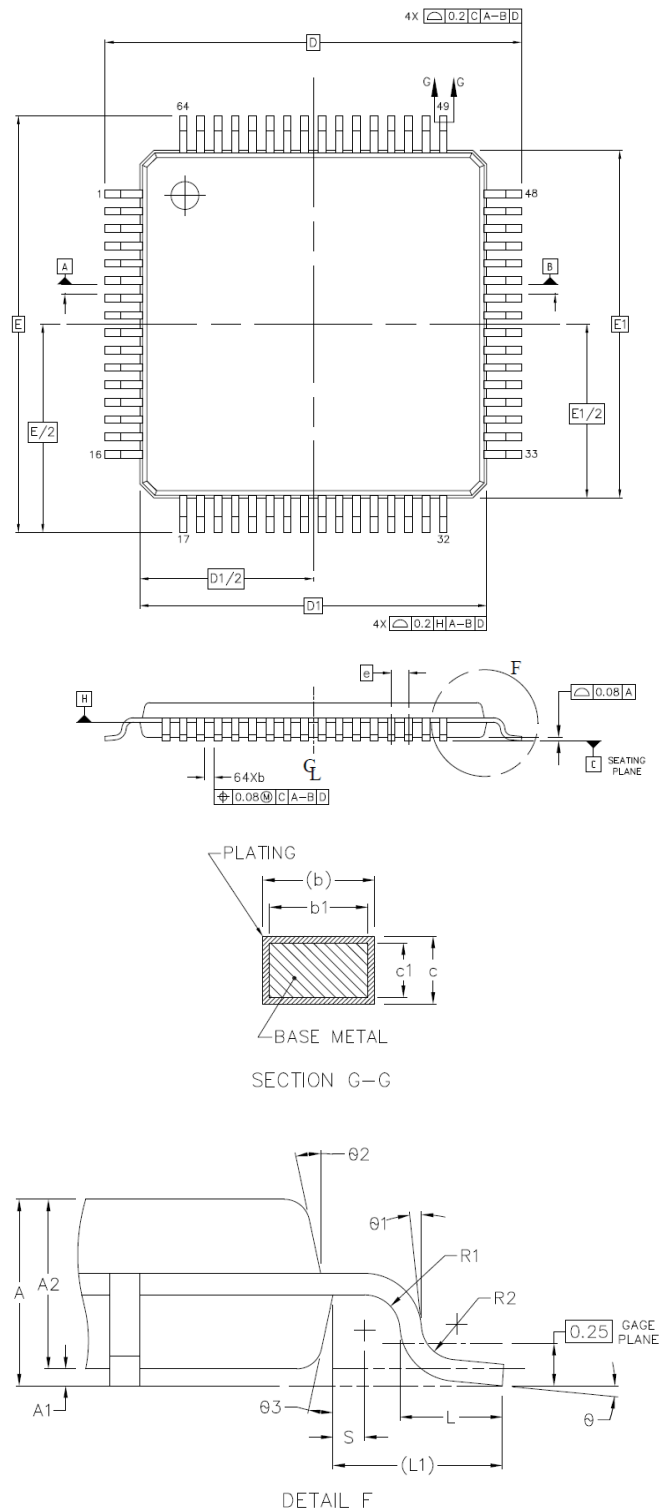


Figure 11.1. TQFP64 Package Drawing