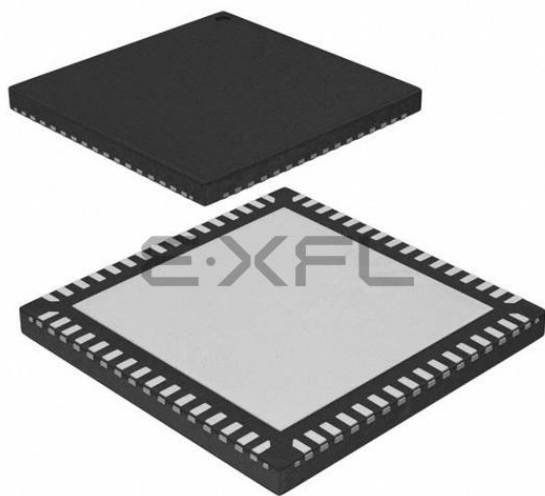




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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	56
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b120f2048gm64-ar

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Converter	USB	Ethernet	QSPI	SDIO	LCD	GPIO	Package	Temp Range
EFM32GG11B820F2048GL192-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	144	BGA192	-40 to +85°C
EFM32GG11B840F1024GL192-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	144	BGA192	-40 to +85°C
EFM32GG11B820F2048GL152-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +85°C
EFM32GG11B820F2048IL152-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +125°C
EFM32GG11B840F1024GL152-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +85°C
EFM32GG11B840F1024IL152-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +125°C
EFM32GG11B820F2048GL120-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +85°C
EFM32GG11B820F2048IL120-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +125°C
EFM32GG11B840F1024GL120-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +85°C
EFM32GG11B840F1024IL120-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +125°C
EFM32GG11B820F2048GQ100-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +85°C
EFM32GG11B820F2048IQ100-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +125°C
EFM32GG11B840F1024GQ100-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +85°C
EFM32GG11B840F1024IQ100-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +125°C
EFM32GG11B820F2048GQ64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +85°C
EFM32GG11B820F2048GM64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +85°C
EFM32GG11B820F2048IQ64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +125°C
EFM32GG11B820F2048IM64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +125°C
EFM32GG11B840F1024GQ64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +85°C
EFM32GG11B840F1024GM64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +85°C
EFM32GG11B840F1024IQ64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +125°C
EFM32GG11B840F1024IM64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +125°C
EFM32GG11B520F2048GL120-A	2048	512	Yes	No	No	No	No	Yes	95	BGA120	-40 to +85°C
EFM32GG11B510F2048GL120-A	2048	384	Yes	No	No	No	No	Yes	95	BGA120	-40 to +85°C
EFM32GG11B520F2048IL120-A	2048	512	Yes	No	No	No	No	Yes	95	BGA120	-40 to +125°C
EFM32GG11B510F2048IL120-A	2048	384	Yes	No	No	No	No	Yes	95	BGA120	-40 to +125°C
EFM32GG11B520F2048GQ100-A	2048	512	Yes	No	No	No	No	Yes	83	QFP100	-40 to +85°C
EFM32GG11B510F2048GQ100-A	2048	384	Yes	No	No	No	No	Yes	83	QFP100	-40 to +85°C
EFM32GG11B520F2048IQ100-A	2048	512	Yes	No	No	No	No	Yes	83	QFP100	-40 to +125°C
EFM32GG11B510F2048IQ100-A	2048	384	Yes	No	No	No	No	Yes	83	QFP100	-40 to +125°C

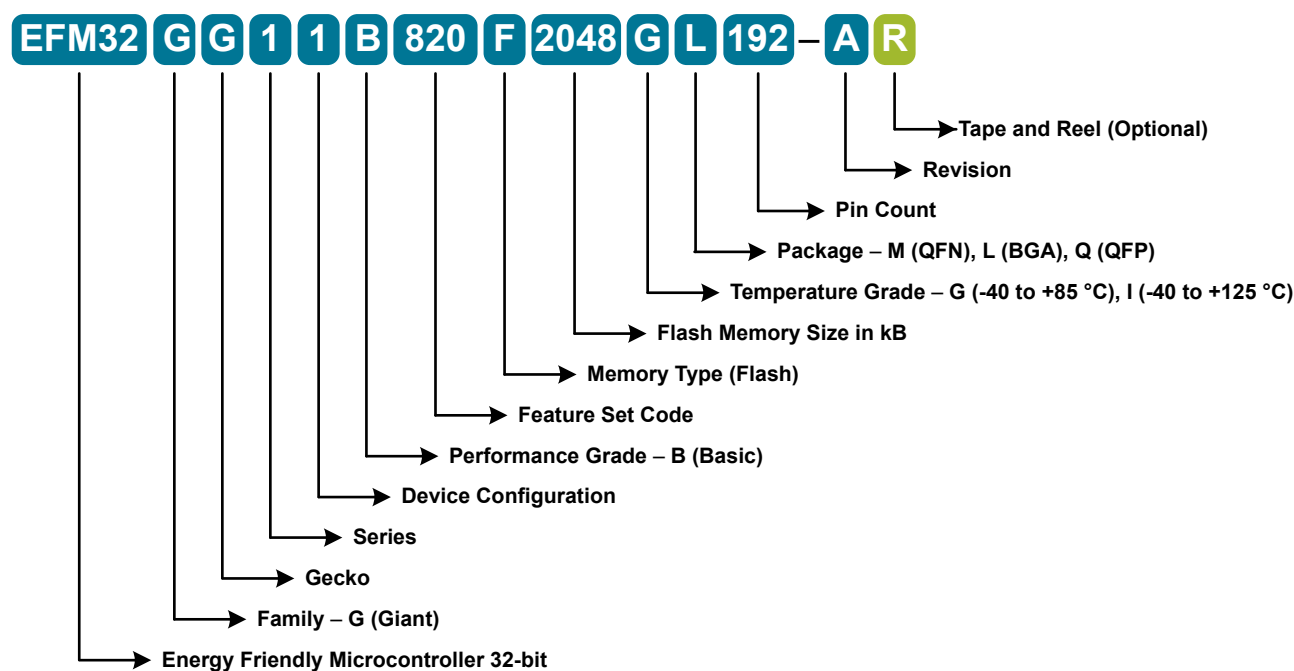


Figure 2.1. Ordering Code Key

3.2 Power

The EFM32GG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

3.4.2 Internal and External Oscillators

The EFM32GG11 supports two crystal oscillators and fully integrates five RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 50 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated auxiliary high frequency RC oscillator (USHFRCO) is available for timing the USB, SDIO and QSPI peripherals. The USHFRCO can be synchronized to the host's USB clock to allow the USB to operate in device mode without the additional cost of an external crystal.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

4.1.10.4 High-Frequency RC Oscillator (HFRCO)

Table 4.15. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{\text{HFRCO_ACC}}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	t_{HFRCO}	$f_{\text{HFRCO}} \geq 19 \text{ MHz}$	—	300	—	ns
		$4 < f_{\text{HFRCO}} < 19 \text{ MHz}$	—	1	—	μs
		$f_{\text{HFRCO}} \leq 4 \text{ MHz}$	—	2.5	—	μs
Maximum DPLL lock time ¹	$t_{\text{DPLL_LOCK}}$	$f_{\text{REF}} = 32.768 \text{ kHz}$, $f_{\text{HFRCO}} = 39.98 \text{ MHz}$, $N = 1219$, $M = 0$	—	183	—	μs
Current consumption on all supplies	I_{HFRCO}	$f_{\text{HFRCO}} = 72 \text{ MHz}$	—	608	TBD	μA
		$f_{\text{HFRCO}} = 64 \text{ MHz}$	—	545	TBD	μA
		$f_{\text{HFRCO}} = 56 \text{ MHz}$	—	478	TBD	μA
		$f_{\text{HFRCO}} = 48 \text{ MHz}$	—	413	TBD	μA
		$f_{\text{HFRCO}} = 38 \text{ MHz}$	—	341	TBD	μA
		$f_{\text{HFRCO}} = 32 \text{ MHz}$	—	286	TBD	μA
		$f_{\text{HFRCO}} = 26 \text{ MHz}$	—	240	TBD	μA
		$f_{\text{HFRCO}} = 19 \text{ MHz}$	—	191	TBD	μA
		$f_{\text{HFRCO}} = 16 \text{ MHz}$	—	164	TBD	μA
		$f_{\text{HFRCO}} = 13 \text{ MHz}$	—	143	TBD	μA
		$f_{\text{HFRCO}} = 7 \text{ MHz}$	—	103	TBD	μA
		$f_{\text{HFRCO}} = 4 \text{ MHz}$	—	42	TBD	μA
		$f_{\text{HFRCO}} = 2 \text{ MHz}$	—	33	TBD	μA
		$f_{\text{HFRCO}} = 1 \text{ MHz}$	—	28	TBD	μA
		$f_{\text{HFRCO}} = 72 \text{ MHz}$, DPLL enabled	—	927	TBD	μA
		$f_{\text{HFRCO}} = 40 \text{ MHz}$, DPLL enabled	—	526	TBD	μA
		$f_{\text{HFRCO}} = 32 \text{ MHz}$, DPLL enabled	—	419	TBD	μA
		$f_{\text{HFRCO}} = 16 \text{ MHz}$, DPLL enabled	—	233	TBD	μA
		$f_{\text{HFRCO}} = 4 \text{ MHz}$, DPLL enabled	—	59	TBD	μA
		$f_{\text{HFRCO}} = 1 \text{ MHz}$, DPLL enabled	—	36	TBD	μA
Coarse trim step size (% of period)	$SS_{\text{HFRCO_COARSE}}$		—	0.8	—	%
Fine trim step size (% of period)	$SS_{\text{HFRCO_FINE}}$		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS

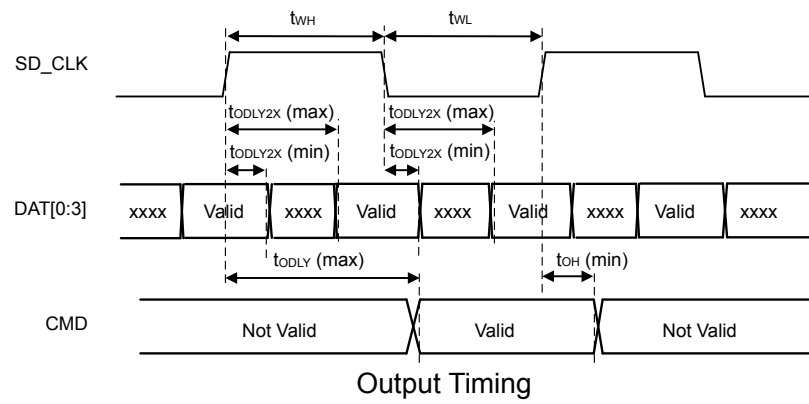
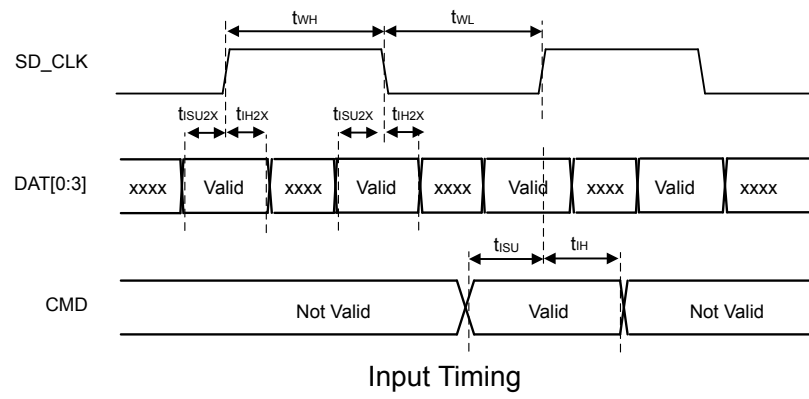


Figure 4.16. SDIO DDR Mode Timing

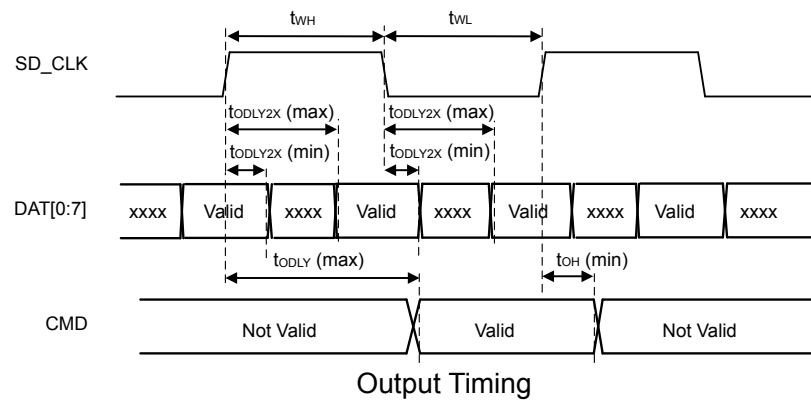
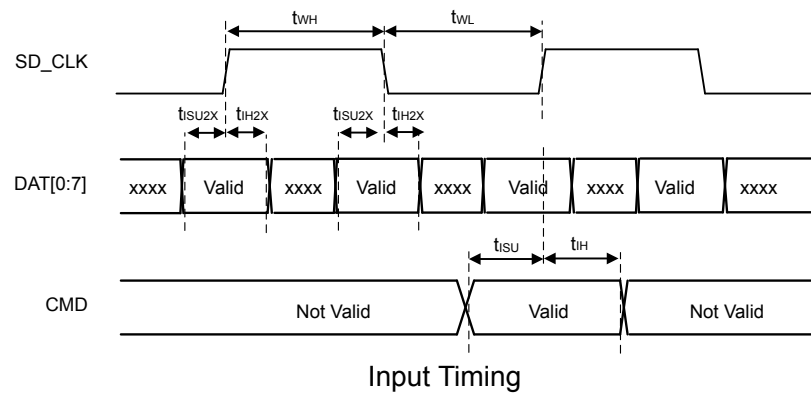


Figure 4.19. SDIO MMC DDR Mode Timing

QSPI DDR Mode Timing (Locations 1, 2)

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 53, RX DLL = 88, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.57. QSPI DDR Mode Timing (Locations 1, 2)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Half SCLK period	T/2	HFXO	$(1/F_{SCLK}) * 0.4 - 0.4$	—	—	ns
		HFRCO, AUXHFRCO, USHFRCO	$(1/F_{SCLK}) * 0.44$	—	—	ns
Output valid	t_{OV}		—	—	T/2 - 6.6	ns
Output hold	t_{OH}		T/2 - 52.2	—	—	ns
Input setup	t_{SU}		44.8	—	—	ns
Input hold	t_H		-2.4	—	—	ns

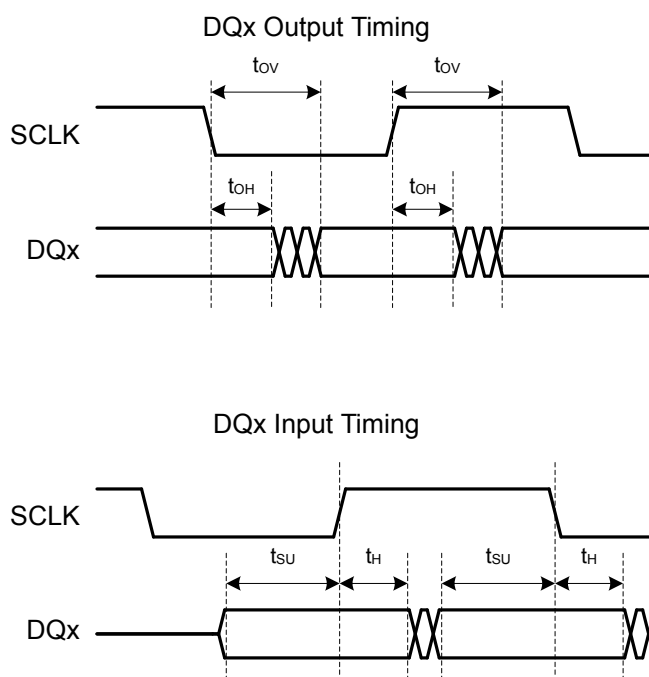


Figure 4.22. QSPI DDR Timing Diagrams

QSPI DDR Flash Timing Example

This example uses timing values for location 0 (DDR mode) to demonstrate the calculation of allowable flash timing using the QSPI in DDR mode.

- Using a configured SCLK frequency (F_{SCLK}) of 8 MHz from the HFXO clock source:
- The resulting minimum half-period, $T/2(\min) = (1/F_{SCLK}) * 0.4 - 0.4 = 49.6$ ns.
- Flash will see a minimum setup time of $T/2 - t_{OV} = T/2 - (T/2 - 5.0) = 5.0$ ns.
- Flash will see a minimum hold time of $t_{OH} = T/2 - 39.4 = 49.6 - 39.4 = 10.2$ ns.
- Flash can have a maximum output valid time of $T/2 - t_{SU} = T/2 - 33.1 = 49.6 - 33.1 = 16.5$ ns.
- Flash can have a minimum output hold time of $t_H = -0.9$ ns.

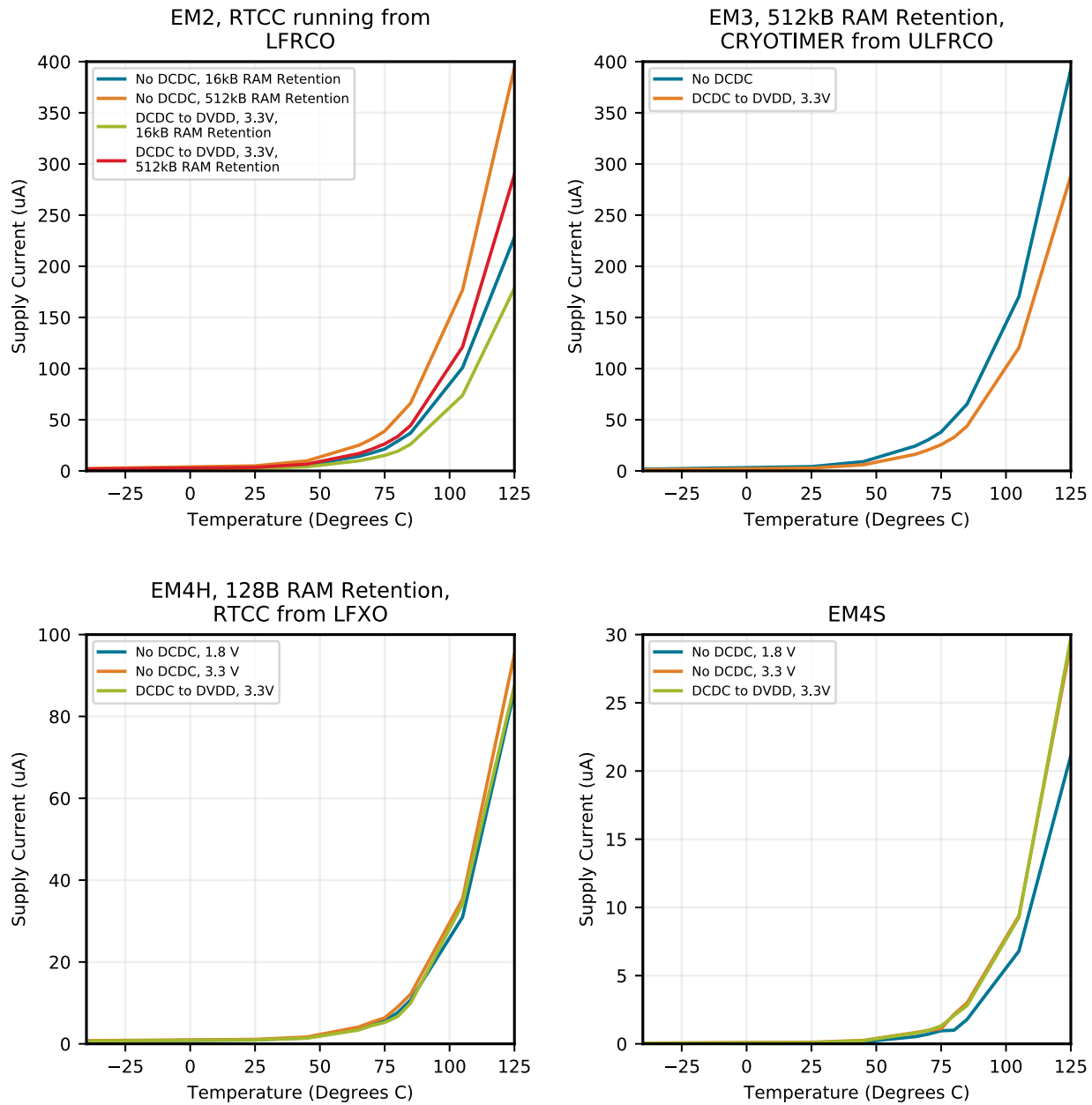


Figure 4.26. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature

5.7 EFM32GG11B3xx in BGA112 Device Pinout

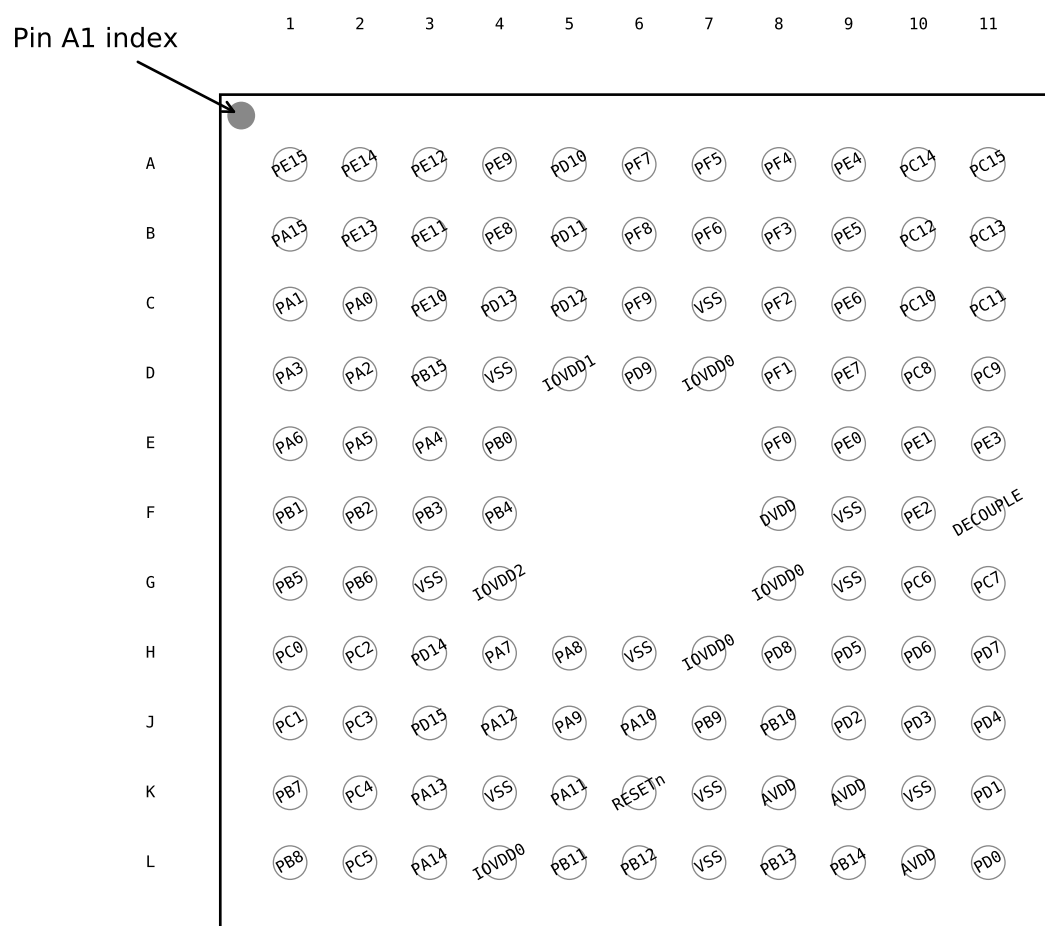


Figure 5.7. EFM32GG11B3xx in BGA112 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.7. EFM32GG11B3xx in BGA112 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD10	A5	GPIO	PF7	A6	GPIO
PF5	A7	GPIO	PF4	A8	GPIO
PE4	A9	GPIO	PC14	A10	GPIO (5V)
PC15	A11	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO (5V)
PC9	42	GPIO (5V)	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PF14	BUSDY BUSCX		TIM1_CC1 #6 TIM4_CC1 #1 TIM5_CC2 #7 WTIM3_CC1 #7	I2C2_SCL #4	
PF11	BUSCY BUSDX	EBI_NANDWEn #5	TIM5_CC2 #6 WTIM3_CC2 #3 PCNT2_S1IN #3	US5_CTS #2 U1_RX #1 I2C2_SCL #2 USB_DP	
PF10	BUSDY BUSCX	EBI_ARDY #5	TIM5_CC1 #6 WTIM3_CC1 #3 PCNT2_S0IN #3	US5_RTS #2 U1_TX #1 I2C2_SDA #2 USB_DM	
PF0	BUSDY BUSCX	EBI_A24 #1	TIM0_CC0 #4 WTIM0_CC1 #4 LE- TIM0_OUT0 #2	US2_TX #5 CAN0_RX #1 US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	PRS_CH15 #2 ACMP3_O #0 DBG_SWCLKTCK BOOT_TX
PA0	BUSBY BUSAX LCD_SEG13	EBI_AD09 #0 EBI_CSTFT #3	TIM0_CC0 #0 TIM0_CC1 #7 TIM3_CC0 #4 PCNT0_S0IN #4	ETH_RMIITXEN #0 ETH_MII_TXCLK #0 SDIO_DAT0 #1 US1_RX #5 US3_TX #0 QSPI0_CS0 #1 LEU0_RX #4 I2C0_SDA #0	CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
PD11	LCD_SEG30	EBI_CS2 #0 EBI_HSNC #1	TIM4_CC0 #6 WTIM3_CC2 #0	ETH_RMIICRS0V #1 SDIO_DAT5 #0 QSPI0_DQ2 #0 ETH_MII_RXD3 #2 US4_CLK #1	
PD10	LCD_SEG29	EBI_CS1 #0 EBI_VSNC #1	TIM4_CC2 #5 WTIM3_CC1 #0	ETH_RMIREFCLK #1 SDIO_DAT6 #0 QSPI0_DQ1 #0 ETH_MII_RXD2 #2 US4_RX #1	CMU_CLK2 #5 CMU_CLKI0 #5
PD9	LCD_SEG28	EBI_CS0 #0 EBI_DTEN #1	TIM4_CC1 #5 WTIM3_CC0 #0	ETH_RMIIRXD0 #1 SDIO_DAT7 #0 QSPI0_DQ0 #0 ETH_MII_RXD1 #2 US4_TX #1	
PF9	BUSCY BUSDX LCD_SEG27	EBI_REn #4 EBI_BL1 #1	TIM4_CC0 #5	ETH_RMIIRXD1 #1 US2_CS #4 QSPI0_DQS #0 ETH_MII_RXD0 #2 ETH_TSUTMRTOG #3 SDIO_WP #0 U0_RTS #0 U1_CTS #1	ETM_TD0 #1
PF8	BUSDY BUSCX LCD_SEG26	EBI_WEn #4 EBI_BL0 #1	TIM0_CC2 #1 TIM4_CC2 #4	ETH_RMIITXEN #1 US2_CLK #4 QSPI0_CS1 #0 ETH_MII_RXDV #2 ETH_TSUEXTCLK #3 SDIO_CD #0 U0_CTS #0 U1_RTS #1	ETM_TCLK #1 GPIO_EM4WU8

Table 5.23. ACMP0 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP0Y	BUSACMP0X	Bus
PF14	PF15	PF15	PF14	PB14	PB15	PB15	PB14			CH31
	PF13	PF13			PB13	PB13				CH30
PF12			PF12	PB12			PB12			CH29
	PF11	PF11			PB11	PB11				CH28
PF10			PF10	PB10			PB10			CH27
	PF9	PF9			PB9	PB9				CH26
PF8			PF8							CH25
	PF7	PF7								CH24
PF6			PF6	PB6			PB6			CH23
	PF5	PF5			PB5	PB5				CH22
PF4			PF4	PB4			PB4			CH21
	PF3	PF3			PB3	PB3				CH20
PF2			PF2	PB2			PB2			CH19
	PF1	PF1			PB1	PB1				CH18
PF0			PF0	PB0			PB0			CH17
	PE15	PE15			PA15	PA15				CH16
PE14			PE14	PA14			PA14			CH15
	PE13	PE13			PA13	PA13				CH14
PE12			PE12	PA12			PA12			CH13
	PE11	PE11			PA11	PA11				CH12
PE10			PE10	PA10			PA10			CH11
	PE9	PE9			PA9	PA9				CH10
PE8			PE8	PA8			PA8			CH9
	PE7	PE7			PA7	PA7		PC7	PC7	CH8
PE6			PE6	PA6			PA6	PC6	PC6	CH7
	PE5	PE5			PA5	PA5		PC5	PC5	CH6
PE4			PE4	PA4			PA4	PC4	PC4	CH5
					PA3	PA3		PC3	PC3	CH4
				PA2			PA2	PC2	PC2	CH3
	PE1	PE1			PA1	PA1		PC1	PC1	CH2
PE0			PE0	PA0			PA0	PC0	PC0	CH1
										CH0

Table 5.27. ADC0 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSADC0Y	BUSADC0X	Bus
	PF15	PF15			PB15	PB15				CH31
PF14			PF14	PB14			PB14			CH30
	PF13	PF13			PB13	PB13				CH29
PF12			PF12	PB12			PB12			CH28
	PF11	PF11			PB11	PB11				CH27
PF10			PF10	PB10			PB10			CH26
	PF9	PF9			PB9	PB9				CH25
PF8			PF8							CH24
	PF7	PF7								CH23
PF6			PF6	PB6			PB6			CH22
	PF5	PF5			PB5	PB5				CH21
PF4			PF4	PB4			PB4			CH20
	PF3	PF3			PB3	PB3				CH19
PF2			PF2	PB2			PB2			CH18
	PF1	PF1			PB1	PB1				CH17
PF0			PF0	PB0			PB0			CH16
	PE15	PE15			PA15	PA15				CH15
PE14			PE14	PA14			PA14			CH14
	PE13	PE13			PA13	PA13				CH13
PE12			PE12	PA12			PA12			CH12
	PE11	PE11			PA11	PA11				CH11
PE10			PE10	PA10			PA10			CH10
	PE9	PE9			PA9	PA9				CH9
PE8			PE8	PA8			PA8			CH8
	PE7	PE7			PA7	PA7		PD7	PD7	CH7
PE6			PE6	PA6			PA6	PD6	PD6	CH6
	PE5	PE5			PA5	PA5		PD5	PD5	CH5
PE4			PE4	PA4			PA4	PD4	PD4	CH4
					PA3	PA3		PD3	PD3	CH3
				PA2			PA2	PD2	PD2	CH2
	PE1	PE1			PA1	PA1		PD1	PD1	CH1
PE0			PE0	PA0			PA0	PD0	PD0	CH0

Table 5.29. CSEN Bus and Pin Mapping

[illegible]

Table 5.30. IDAC0 Bus and Pin Mapping

APORT1Y	APORT1X	Port
BUSCY	BUSCX	Bus
PF15		CH31
	PF14	CH30
PF13		CH29
	PF12	CH28
PF11		CH27
	PF10	CH26
PF9		CH25
	PF8	CH24
PF7		CH23
	PF6	CH22
PF5		CH21
	PF4	CH20
PF3		CH19
	PF2	CH18
PF1		CH17
	PF0	CH16
PE15		CH15
	PE14	CH14
PE13		CH13
	PE12	CH12
PE11		CH11
	PE10	CH10
PE9		CH9
	PE8	CH8
PE7		CH7
	PE6	CH6
PE5		CH5
	PE4	CH4
		CH3
		CH2
PE1		CH1
	PE0	CH0

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA1_N																																	
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY	PF14	PF15	PF13	PF11	PF9	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4		PE1	PE0	
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY				PF12																												
APORT1Y	BUSAY	BUSBY	BUSCY	BUSDY																													
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	PB14						PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2	PA0	
APORT3Y	BUSCY	BUSBY	BUSCY	BUSCY		PF15	PF13	PF11	PF9			PF5		PF3		PF1		PE15		PE13		PE11		PE10		PE8		PE6		PE4		PE1	
APORT4Y	BUSDY																																

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	
OPA2_OUT																																		
APORT1Y	BUSAY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	
APORT3Y	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	
APORT4Y	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	
APORT1X	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	
APORT2X	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	
APORT3X	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	
APORT4X	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	
APORT1N	BUSAN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	
APORT2N	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	
APORT3N	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	
APORT4N	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	
APORT1Y	BUSAY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	
APORT3Y	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY
APORT4Y	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY
APORT1X	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX
APORT2X	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX
APORT3X	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX
APORT4X	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX	BUSDX
APORT1N	BUSAN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN
APORT2N	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN
APORT3N	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN
APORT4N	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSDN	BUSD

9. BGA112 Package Specifications

9.1 BGA112 Package Dimensions

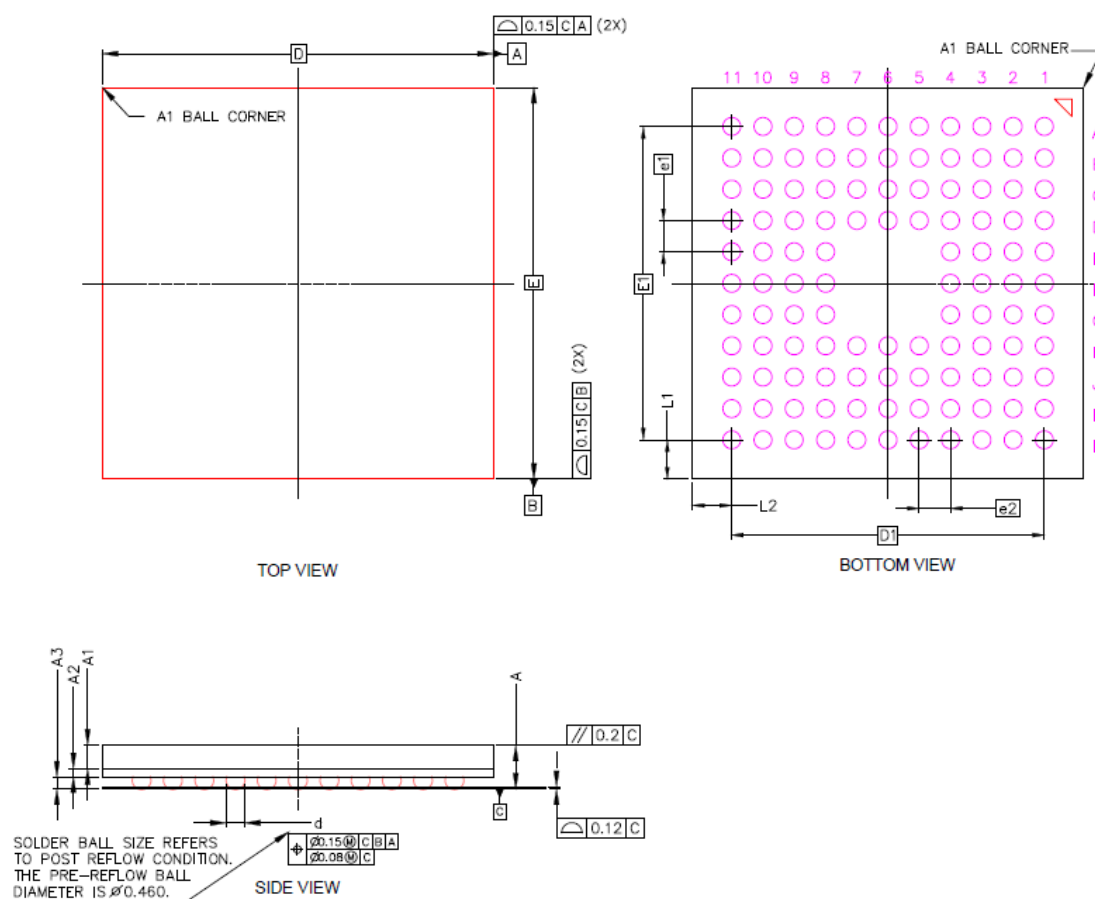


Figure 9.1. BGA112 Package Drawing

9.3 BGA112 Package Marking



Figure 9.3. BGA112 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.

12.2 QFN64 PCB Land Pattern

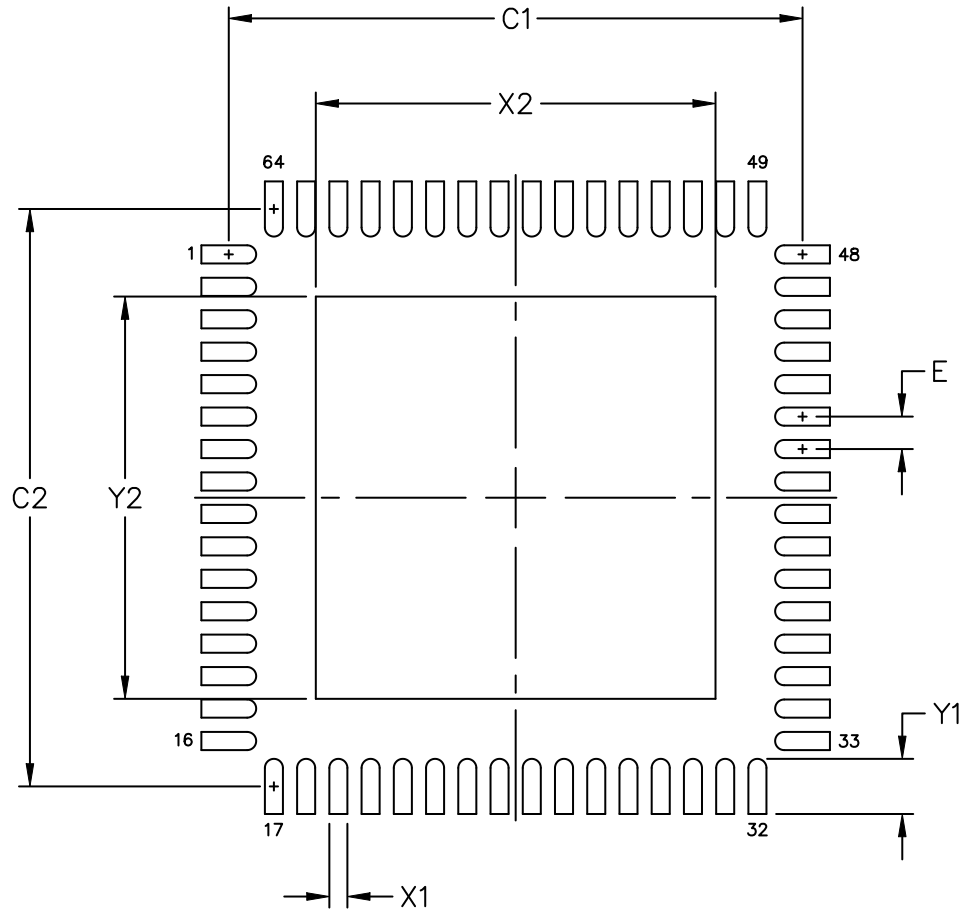


Figure 12.2. QFN64 PCB Land Pattern Drawing