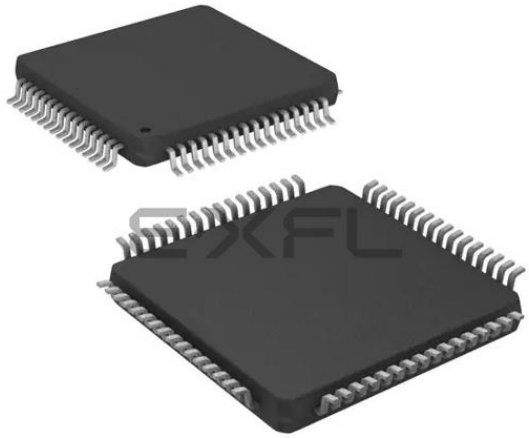
Silicon Labs - EFM32GG11B120F2048GQ64-B Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b120f2048gq64-b

3.2 Power

The EFM32GG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

3.4.2 Internal and External Oscillators

The EFM32GG11 supports two crystal oscillators and fully integrates five RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 50 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (USHFRCO) is available for timing the USB, SDIO and QSPI peripherals. The USHFRCO can be syncronized to the host's USB clock to allow the USB to operate in device mode without the additional cost of an external crystal.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode[3]	I_{ACTIVE_LPM}	32 MHz HFRCO, CPU running while loop from flash	—	82	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	83	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	88	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	257	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1]	$I_{ACTIVE\_CCM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	117	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1231	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode[3]	$I_{ACTIVE\_LPM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	72	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	219	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{EM1_DCM}	72 MHz HFRCO	—	42	—	µA/MHz
		50 MHz crystal	—	46	—	µA/MHz
		48 MHz HFRCO	—	46	—	µA/MHz
		32 MHz HFRCO	—	53	—	µA/MHz
		26 MHz HFRCO	—	57	—	µA/MHz
		16 MHz HFRCO	—	72	—	µA/MHz
		1 MHz HFRCO	—	663	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode[3]	I_{EM1_LPM}	32 MHz HFRCO	—	42	—	µA/MHz
		26 MHz HFRCO	—	43	—	µA/MHz
		16 MHz HFRCO	—	48	—	µA/MHz
		1 MHz HFRCO	—	219	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[2]	$I_{EM1\_DCM\_VS}$	19 MHz HFRCO	—	60	—	µA/MHz
		1 MHz HFRCO	—	637	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode[3]	$I_{EM1\_LPM\_VS}$	19 MHz HFRCO	—	39	—	µA/MHz
		1 MHz HFRCO	—	190	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode[3]	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	2.8	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	3.1	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[5]	—	2.1	—	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.4	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis (V_{CM} = 1.25 V, BIASPROG[4] = 0x10, FULLBIAS[4] = 1)	$V_{ACMPHYST}$	HYSTSEL[5] = HYST0	TBD	0	TBD	mV
		HYSTSEL[5] = HYST1	TBD	18	TBD	mV
		HYSTSEL[5] = HYST2	TBD	33	TBD	mV
		HYSTSEL[5] = HYST3	TBD	46	TBD	mV
		HYSTSEL[5] = HYST4	TBD	57	TBD	mV
		HYSTSEL[5] = HYST5	TBD	68	TBD	mV
		HYSTSEL[5] = HYST6	TBD	79	TBD	mV
		HYSTSEL[5] = HYST7	TBD	90	TBD	mV
		HYSTSEL[5] = HYST8	TBD	0	TBD	mV
		HYSTSEL[5] = HYST9	TBD	-18	TBD	mV
		HYSTSEL[5] = HYST10	TBD	-33	TBD	mV
		HYSTSEL[5] = HYST11	TBD	-45	TBD	mV
		HYSTSEL[5] = HYST12	TBD	-57	TBD	mV
		HYSTSEL[5] = HYST13	TBD	-67	TBD	mV
		HYSTSEL[5] = HYST14	TBD	-78	TBD	mV
		HYSTSEL[5] = HYST15	TBD	-88	TBD	mV
Comparator delay[3]	$t_{ACMPDELAY}$	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	30	—	µs
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	3.7	—	µs
		BIASPROG[4] = 0x02, FULLBIAS[4] = 1	—	360	—	ns
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[4] =0x10, FULLBIAS[4] = 1	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	CSRESSEL[6] = 0	—	infinite	—	kΩ
		CSRESSEL[6] = 1	—	15	—	kΩ
		CSRESSEL[6] = 2	—	27	—	kΩ
		CSRESSEL[6] = 3	—	39	—	kΩ
		CSRESSEL[6] = 4	—	51	—	kΩ
		CSRESSEL[6] = 5	—	100	—	kΩ
		CSRESSEL[6] = 6	—	162	—	kΩ
		CSRESSEL[6] = 7	—	235	—	kΩ

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.
2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.
3. ± 100 mV differential drive.
4. In ACMPn_CTRL register.
5. In ACMPn_HYSTERESIS registers.
6. In ACMPn_INPUTSEL register.

4.1.18 Capacitive Sense (CSEN)

Table 4.26. Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single conversion time (1x accumulation)	t_{CNV}	12-bit SAR Conversions	—	20.2	—	µs
		16-bit SAR Conversions	—	26.4	—	µs
		Delta Modulation Conversion (single comparison)	—	1.55	—	µs
Maximum external capacitive load	C_{EXTMAX}	CS0CG=7 (Gain = 1x), including routing parasitics	—	68	—	pF
		CS0CG=0 (Gain = 10x), including routing parasitics	—	680	—	pF
Maximum external series impedance	R_{EXTMAX}		—	1	—	kΩ
Supply current, EM2 bonded conversions, WARMUPMODE=NORMAL, WARMUPCNT=0	I_{CSEN_BOND}	12-bit SAR conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	326	—	nA
		Delta Modulation conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	226	—	nA
		12-bit SAR conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	33	—	nA
		Delta Modulation conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	25	—	nA
Supply current, EM2 scan conversions, WARMUPMODE=NORMAL, WARMUPCNT=0	I_{CSEN_EM2}	12-bit SAR conversions, 20 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	690	—	nA
		Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	515	—	nA
		12-bit SAR conversions, 200 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	79	—	nA
		Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	57	—	nA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
MISO hold time [1] [3]	t_{H_MI}	USART2, location 4, IOVDD = 1.8 V	-11.6	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	-11.6	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	-9.1	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	-9.1	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	-8	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	-8	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

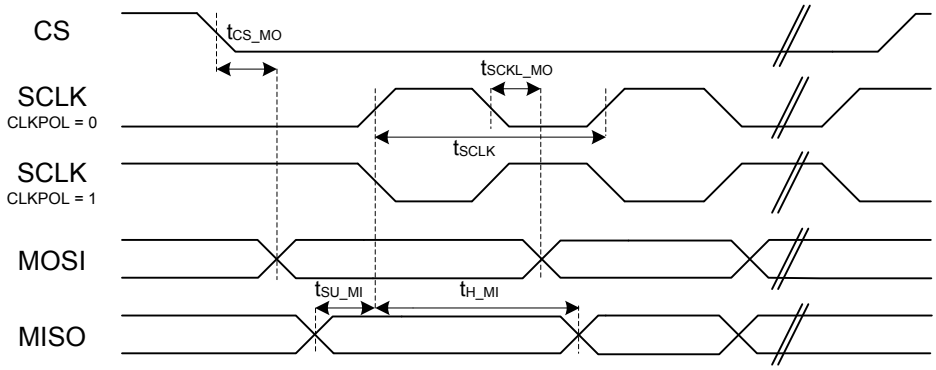


Figure 4.1. SPI Master Timing Diagram

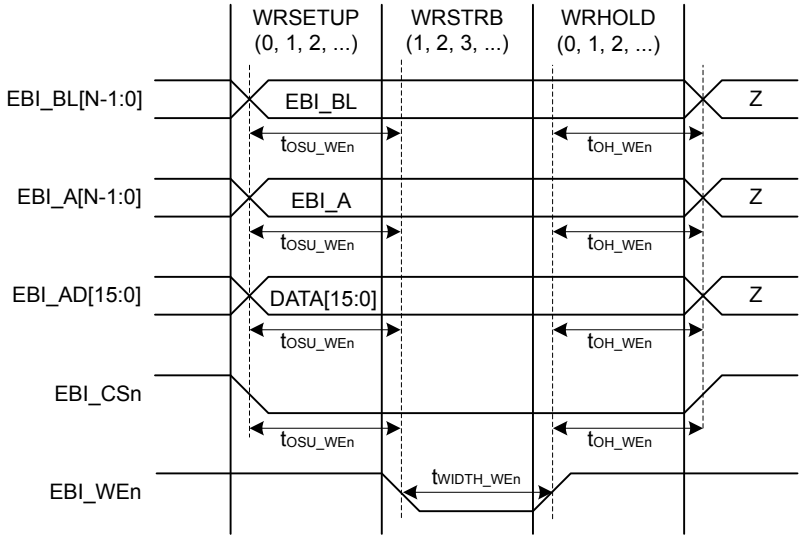


Figure 4.3. EBI Write Enable Output Timing Diagram

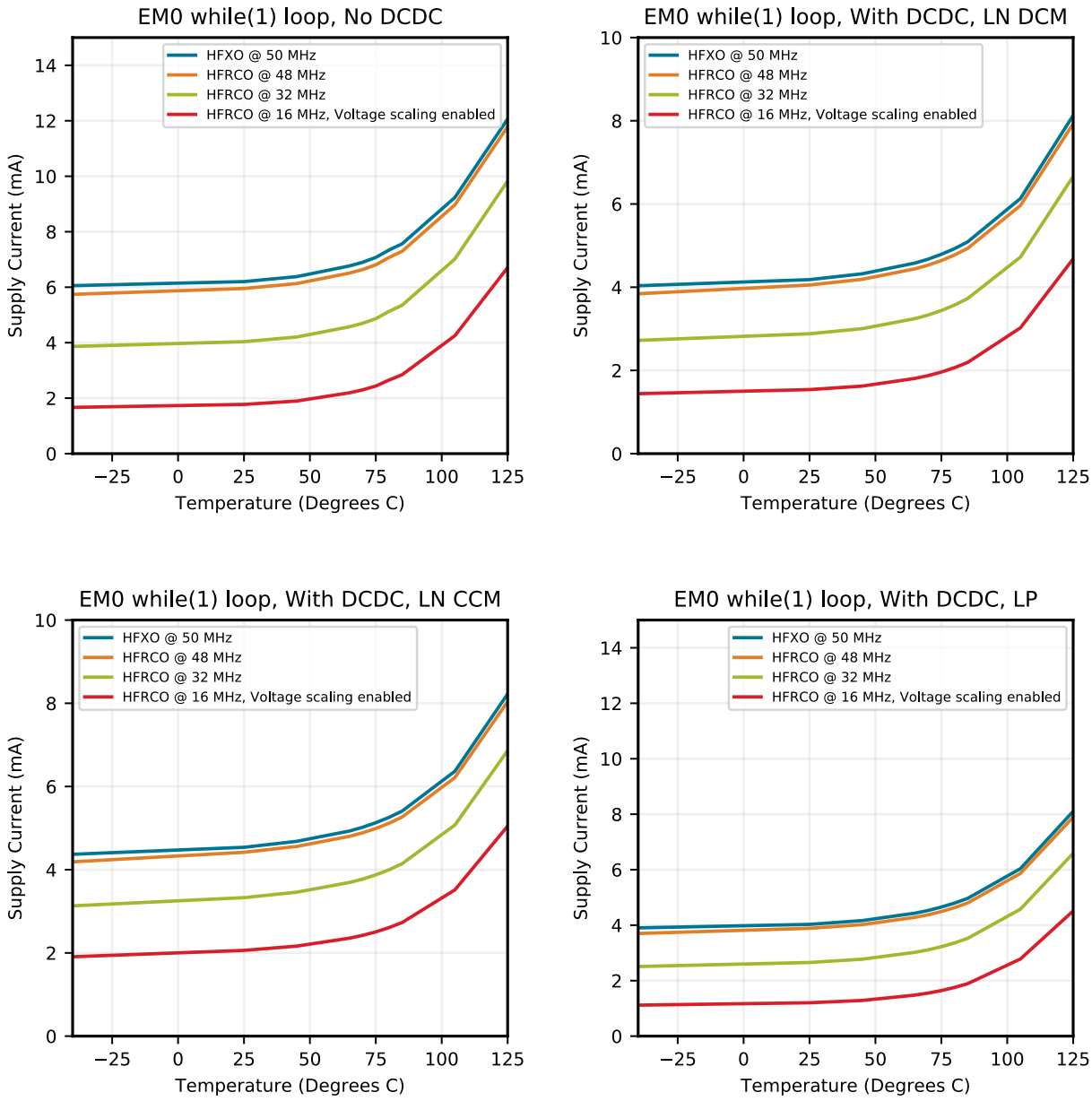


Figure 4.24. EM0 Active Mode Typical Supply Current vs. Temperature

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
IOVDD1	F7 G7	Digital IO power supply 1.	VSS	F8 G8 G9 H6 H7 H8 H9 H10 H11 J6 J7 J8 J9 J10 J11 K8 K9 L8 L9	Ground
NC	F9	No Connect.	IOVDD0	F10 F11 G10 G11 K6 K7 K10 K11 L6 L7 L10 L11	Digital IO power supply 0.
PI5	F14	GPIO (5V)	PI4	F15	GPIO (5V)
PI3	F16	GPIO (5V)	PA5	G1	GPIO
PG6	G2	GPIO (5V)	PG5	G3	GPIO (5V)
PI2	G14	GPIO (5V)	PI1	G15	GPIO (5V)
PI0	G16	GPIO (5V)	PA6	H1	GPIO
PG8	H2	GPIO (5V)	PG7	H3	GPIO (5V)
PE5	H14	GPIO	PE6	H15	GPIO
PE7	H16	GPIO	PG11	J1	GPIO (5V)
PG10	J2	GPIO (5V)	PG9	J3	GPIO (5V)
PE3	J14	GPIO	PE4	J15	GPIO
DECOUPLE	J16	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PG14	K1	GPIO
PG13	K2	GPIO	PG12	K3	GPIO
PE1	K14	GPIO (5V)	PE2	K15	GPIO
DVDD	K16	Digital power supply.	PG15	L1	GPIO (5V)
PB15	L2	GPIO (5V)	PB0	L3	GPIO
PE0	L14	GPIO (5V)	PC7	L15	GPIO
VREGVDD	L16	Voltage regulator VDD input	PB1	M1	GPIO

5.10 EFM32GG11B4xx in QFP100 Device Pinout

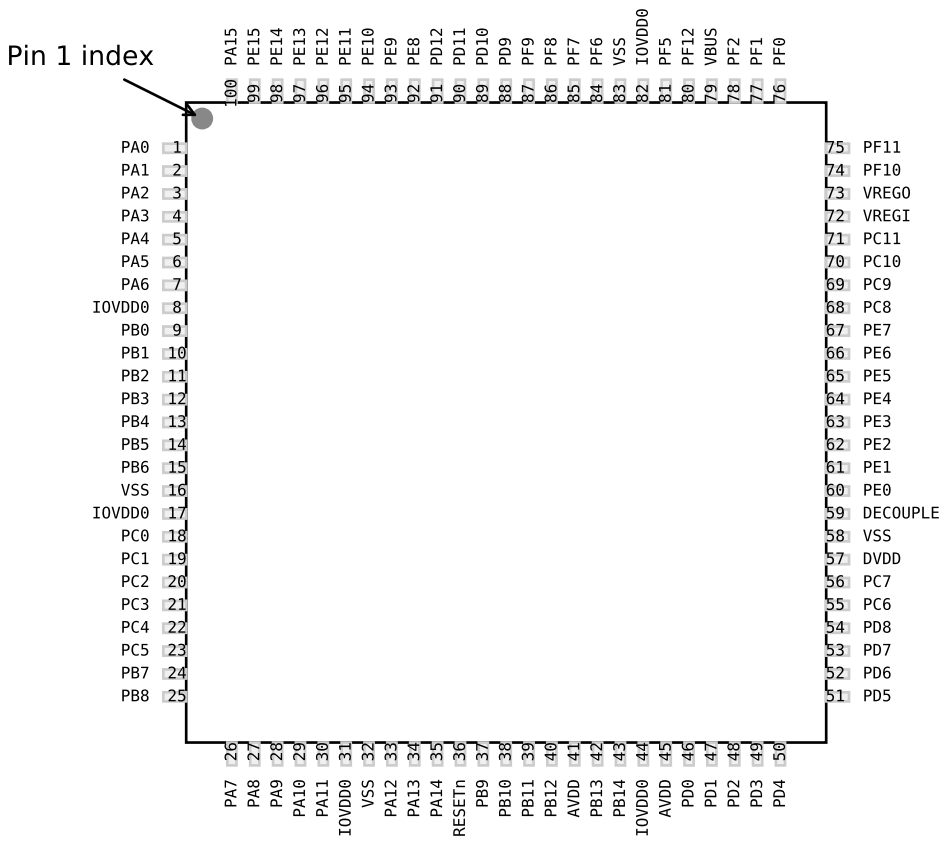


Figure 5.10. EFM32GG11B4xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.10. EFM32GG11B4xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA12	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	PB12	22	GPIO
AVDD	24	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	28	GPIO (5V)
PD1	29	GPIO	PD2	30	GPIO (5V)
PD3	31	GPIO	PD4	32	GPIO
PD5	33	GPIO	PD6	34	GPIO
PD8	35	GPIO	VREGVSS	36	Voltage regulator VSS
VREGSW	37	DCDC regulator switching node	VREGVDD	38	Voltage regulator VDD input
DVDD	39	Digital power supply.	DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	41	GPIO	PE5	42	GPIO
PE6	43	GPIO	PE7	44	GPIO
VREGI	45	Input to 5 V regulator.	VREGO	46	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PF10	47	GPIO (5V)	PF11	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.
PF12	53	GPIO	PF5	54	GPIO
PE8	57	GPIO	PE9	58	GPIO
PE10	59	GPIO	PE11	60	GPIO
PE12	61	GPIO	PE13	62	GPIO
PE14	63	GPIO	PE15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PRS_CH7	0: PB13 1: PA7 2: PE7		Peripheral Reflex System PRS, channel 7.
PRS_CH8	0: PA8 1: PA2 2: PE9		Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA9 1: PA3 2: PB10		Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PA10 1: PC2 2: PD4		Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PA11 1: PC3 2: PD5		Peripheral Reflex System PRS, channel 11.
PRS_CH12	0: PA12 1: PB6 2: PD8		Peripheral Reflex System PRS, channel 12.
PRS_CH13	0: PA13 1: PB9 2: PE14		Peripheral Reflex System PRS, channel 13.
PRS_CH14	0: PA14 1: PC6 2: PE15		Peripheral Reflex System PRS, channel 14.
PRS_CH15	0: PA15 1: PC7 2: PF0		Peripheral Reflex System PRS, channel 15.
PRS_CH16	0: PA4 1: PB12 2: PE4		Peripheral Reflex System PRS, channel 16.
PRS_CH17	0: PA5 1: PB15 2: PE5		Peripheral Reflex System PRS, channel 17.
PRS_CH18	0: PB2 1: PC10 2: PC4		Peripheral Reflex System PRS, channel 18.
PRS_CH19	0: PB3 1: PC11 2: PC5		Peripheral Reflex System PRS, channel 19.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
SDIO_DAT7	0: PD9 1: PB4		SDIO Data 7.
SDIO_WP	0: PF9 1: PC5 2: PB15 3: PB9		SDIO Write Protect.
TIM0_CC0	0: PA0 1: PF6 2: PD1 3: PB6	4: PF0 5: PC4 6: PA8 7: PA1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PF7 2: PD2 3: PC0	4: PF1 5: PC5 6: PA9 7: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PF8 2: PD3 3: PC1	4: PF2 5: PA7 6: PA10 7: PA13	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PC13 2: PF3 3: PC2	4: PB7	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PC14 2: PF4 3: PC3	4: PB8	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PC15 2: PF5 3: PC4	4: PB11	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PC13 1: PE10 2: PB0 3: PB7	4: PD6 5: PF2 6: PF13 7: PI6	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PC14 1: PE11 2: PB1 3: PB8	4: PD7 5: PF3 6: PF14 7: PI7	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PC15 1: PE12 2: PB2 3: PB11	4: PC13 5: PF4 6: PF15 7: PI8	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PC12 1: PE13 2: PB3 3: PB12	4: PC14 5: PF12 6: PF5 7: PI9	Timer 1 Capture Compare input / output channel 3.
TIM2_CC0	0: PA8 1: PA12 2: PC8 3: PF2	4: PB6 5: PC2 6: PG8 7: PG5	Timer 2 Capture Compare input / output channel 0.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
U0_TX	0: PF6 1: PE0 2: PA3 3: PC14	4: PC4 5: PF1 6: PD7	UART0 Transmit output. Also used as receive input in half duplex communication.
U1_CTS	0: PC14 1: PF9 2: PB11 3: PE4	4: PC4 5: PH13	UART1 Clear To Send hardware flow control input.
U1_RTS	0: PC15 1: PF8 2: PB12 3: PE5	4: PC5 5: PH14	UART1 Request To Send hardware flow control output.
U1_RX	0: PC13 1: PF11 2: PB10 3: PE3	4: PE13 5: PH12	UART1 Receive input.
U1_TX	0: PC12 1: PF10 2: PB9 3: PE2	4: PE12 5: PH11	UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	0: PE12 1: PE5 2: PC9 3: PC15	4: PB13 5: PA12 6: PG14	USART0 clock input / output.
US0_CS	0: PE13 1: PE4 2: PC8 3: PC14	4: PB14 5: PA13 6: PG15	USART0 chip select input / output.
US0_CTS	0: PE14 1: PE3 2: PC7 3: PC13	4: PB6 5: PB11 6: PH0	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PE15 1: PE2 2: PC6 3: PC12	4: PB5 5: PD6 6: PH1	USART0 Request To Send hardware flow control output.
US0_RX	0: PE11 1: PE6 2: PC10 3: PE12	4: PB8 5: PC1 6: PG13	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PE10 1: PE7 2: PC11 3: PE13	4: PB7 5: PC0 6: PG12	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PB7 1: PD2 2: PF0 3: PC15	4: PC3 5: PB11 6: PE5	USART1 clock input / output.
US1_CS	0: PB8 1: PD3 2: PF1 3: PC14	4: PC0 5: PE4 6: PB2	USART1 chip select input / output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US3_RTS	0: PA5 1: PC1 2: PA14 3: PC15	4: PG5 5: PG11	USART3 Request To Send hardware flow control output.
US3_RX	0: PA1 1: PE7 2: PB7 3: PG7	4: PG1 5: PI13	USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).
US3_TX	0: PA0 1: PE6 2: PB3 3: PG6	4: PG0 5: PI12	USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI).
US4_CLK	0: PC4 1: PD11 2: PI2 3: PI8	4: PH6	USART4 clock input / output.
US4_CS	0: PC5 1: PD12 2: PI3 3: PI9	4: PH7	USART4 chip select input / output.
US4_CTS	0: PA7 1: PD13 2: PI4 3: PI10	4: PH8	USART4 Clear To Send hardware flow control input.
US4_RTS	0: PA8 1: PD14 2: PI5 3: PI11	4: PH9	USART4 Request To Send hardware flow control output.
US4_RX	0: PB8 1: PD10 2: PI1 3: PI7	4: PH5	USART4 Asynchronous Receive. USART4 Synchronous mode Master Input / Slave Output (MISO).
US4_TX	0: PB7 1: PD9 2: PI0 3: PI6	4: PH4	USART4 Asynchronous Transmit. Also used as receive input in half duplex communication. USART4 Synchronous mode Master Output / Slave Input (MOSI).
US5_CLK	0: PB11 1: PD13 2: PF13 3: PH12		USART5 clock input / output.
US5_CS	0: PB13 1: PD14 2: PF12 3: PH13		USART5 chip select input / output.
US5_CTS	0: PB14 1: PD15 2: PF11 3: PH14		USART5 Clear To Send hardware flow control input.
US5_RTS	0: PB12 1: PB15 2: PF10 3: PH15		USART5 Request To Send hardware flow control output.

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA3_OUT																																	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
OPA3_P																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
VDAC0_OUT0 / OPA0_OUT																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

9.2 BGA112 PCB Land Pattern

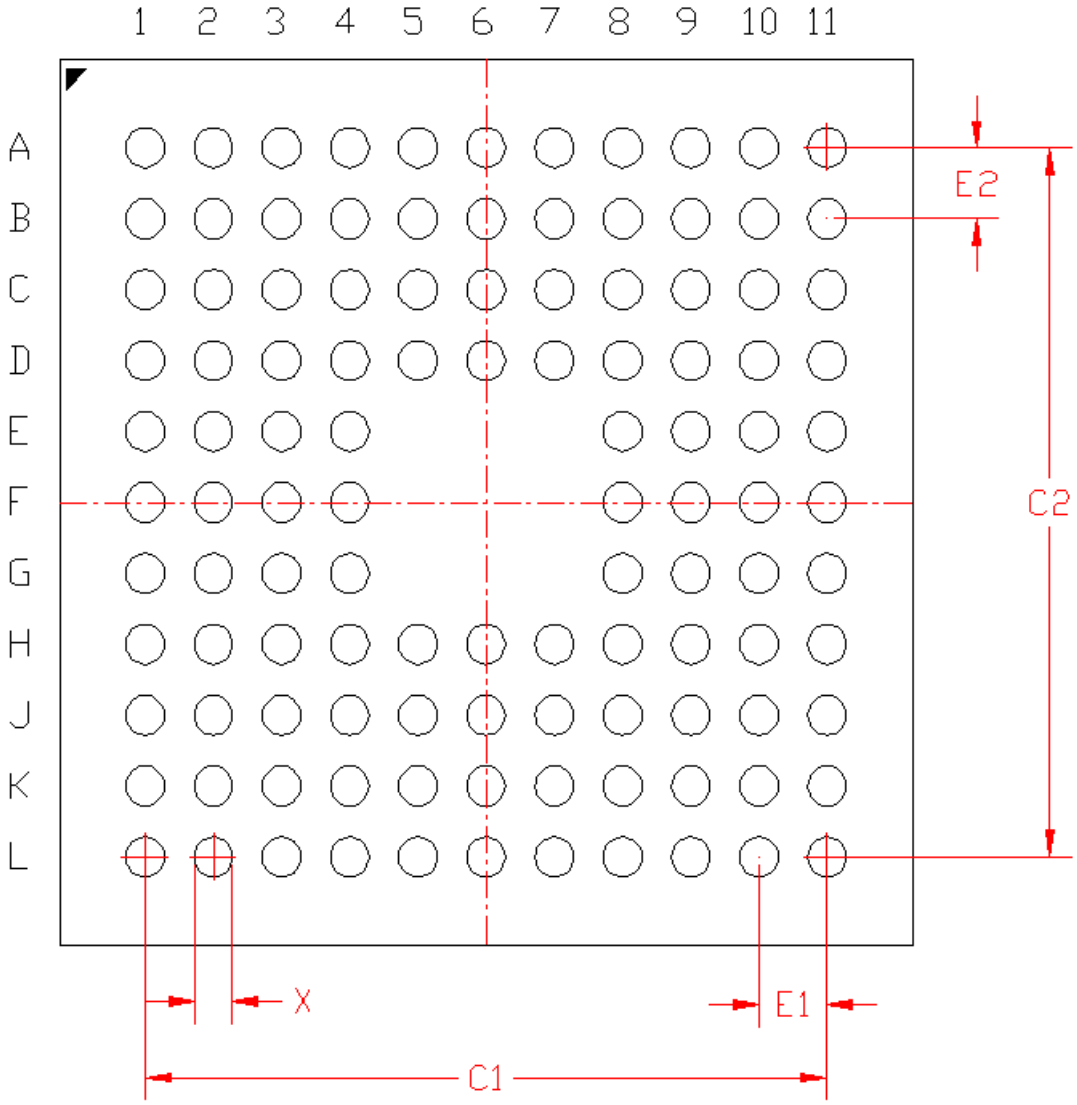


Figure 9.2. BGA112 PCB Land Pattern Drawing

Table 9.2. BGA112 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.45	
C1		8.00	
C2		8.00	
E1		0.8	
E2		0.8	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.3 BGA112 Package Marking

Figure 9.3. BGA112 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.