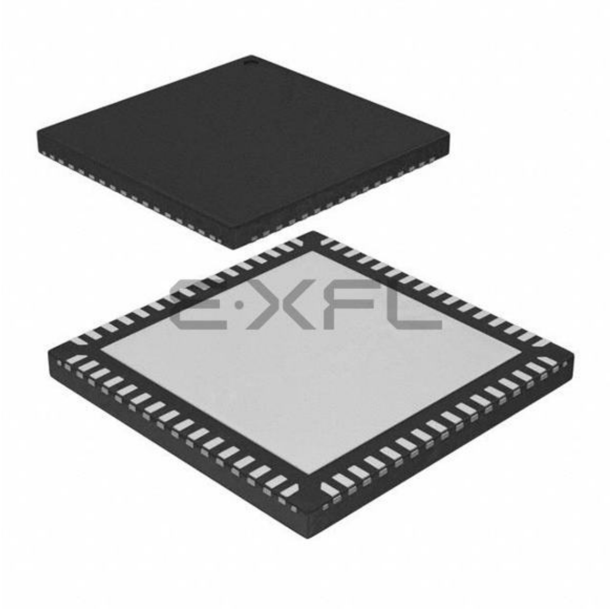
Silicon Labs - EFM32GG11B120F2048IM64-B Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	56
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b120f2048im64-b

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Converter	USB	Ethernet	QSPI	SDIO	LCD	GPIO	Package	Temp Range
EFM32GG11B520F2048GQ64-A	2048	512	Yes	No	No	No	No	Yes	50	QFP64	-40 to +85°C
EFM32GG11B510F2048GQ64-A	2048	384	Yes	No	No	No	No	Yes	50	QFP64	-40 to +85°C
EFM32GG11B520F2048GM64-A	2048	512	Yes	No	No	No	No	Yes	53	QFN64	-40 to +85°C
EFM32GG11B510F2048GM64-A	2048	384	Yes	No	No	No	No	Yes	53	QFN64	-40 to +85°C
EFM32GG11B520F2048IQ64-A	2048	512	Yes	No	No	No	No	Yes	50	QFP64	-40 to +125°C
EFM32GG11B510F2048IQ64-A	2048	384	Yes	No	No	No	No	Yes	50	QFP64	-40 to +125°C
EFM32GG11B520F2048IM64-A	2048	512	Yes	No	No	No	No	Yes	53	QFN64	-40 to +125°C
EFM32GG11B510F2048IM64-A	2048	384	Yes	No	No	No	No	Yes	53	QFN64	-40 to +125°C
EFM32GG11B420F2048GL120-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	93	BGA120	-40 to +85°C
EFM32GG11B420F2048IL120-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	93	BGA120	-40 to +125°C
EFM32GG11B420F2048GL112-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	87	BGA112	-40 to +85°C
EFM32GG11B420F2048IL112-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	87	BGA112	-40 to +125°C
EFM32GG11B420F2048GQ100-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	83	QFP100	-40 to +85°C
EFM32GG11B420F2048IQ100-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	83	QFP100	-40 to +125°C
EFM32GG11B420F2048GQ64-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	50	QFP64	-40 to +85°C
EFM32GG11B420F2048GM64-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	53	QFN64	-40 to +85°C
EFM32GG11B420F2048IQ64-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	50	QFP64	-40 to +125°C
EFM32GG11B420F2048IM64-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	53	QFN64	-40 to +125°C
EFM32GG11B320F2048GL112-A	2048	512	No	No	No	No	No	Yes	90	BGA112	-40 to +85°C
EFM32GG11B310F2048GL112-A	2048	384	No	No	No	No	No	Yes	90	BGA112	-40 to +85°C
EFM32GG11B320F2048GQ100-A	2048	512	No	No	No	No	No	Yes	86	QFP100	-40 to +85°C
EFM32GG11B310F2048GQ100-A	2048	384	No	No	No	No	No	Yes	86	QFP100	-40 to +85°C
EFM32GG11B120F2048GQ64-A	2048	512	No	No	No	No	No	No	53	QFP64	-40 to +85°C
EFM32GG11B110F2048GQ64-A	2048	384	No	No	No	No	No	No	53	QFP64	-40 to +85°C
EFM32GG11B120F2048GM64-A	2048	512	No	No	No	No	No	No	56	QFN64	-40 to +85°C
EFM32GG11B110F2048GM64-A	2048	384	No	No	No	No	No	No	56	QFN64	-40 to +85°C
EFM32GG11B120F2048IQ64-A	2048	512	No	No	No	No	No	No	53	QFP64	-40 to +125°C
EFM32GG11B110F2048IQ64-A	2048	384	No	No	No	No	No	No	53	QFP64	-40 to +125°C
EFM32GG11B120F2048IM64-A	2048	512	No	No	No	No	No	No	56	QFN64	-40 to +125°C
EFM32GG11B110F2048IM64-A	2048	384	No	No	No	No	No	No	56	QFN64	-40 to +125°C

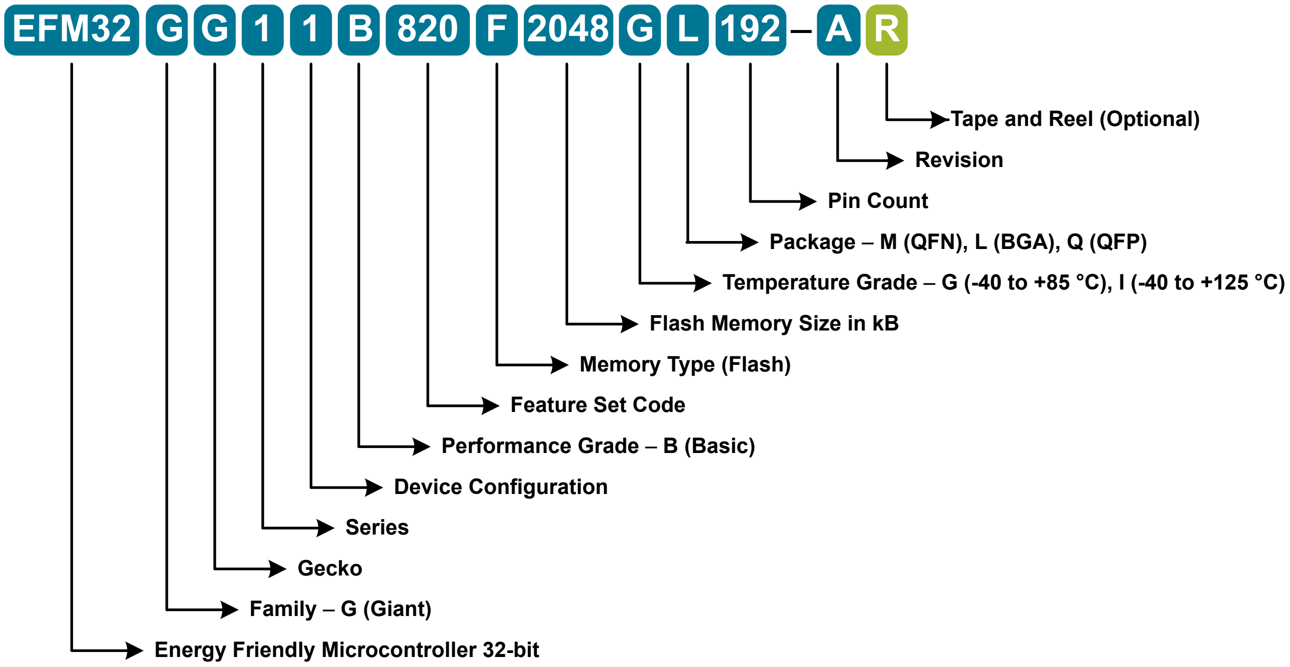


Figure 2.1. Ordering Code Key

3.11 Memory Map

The EFM32GG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

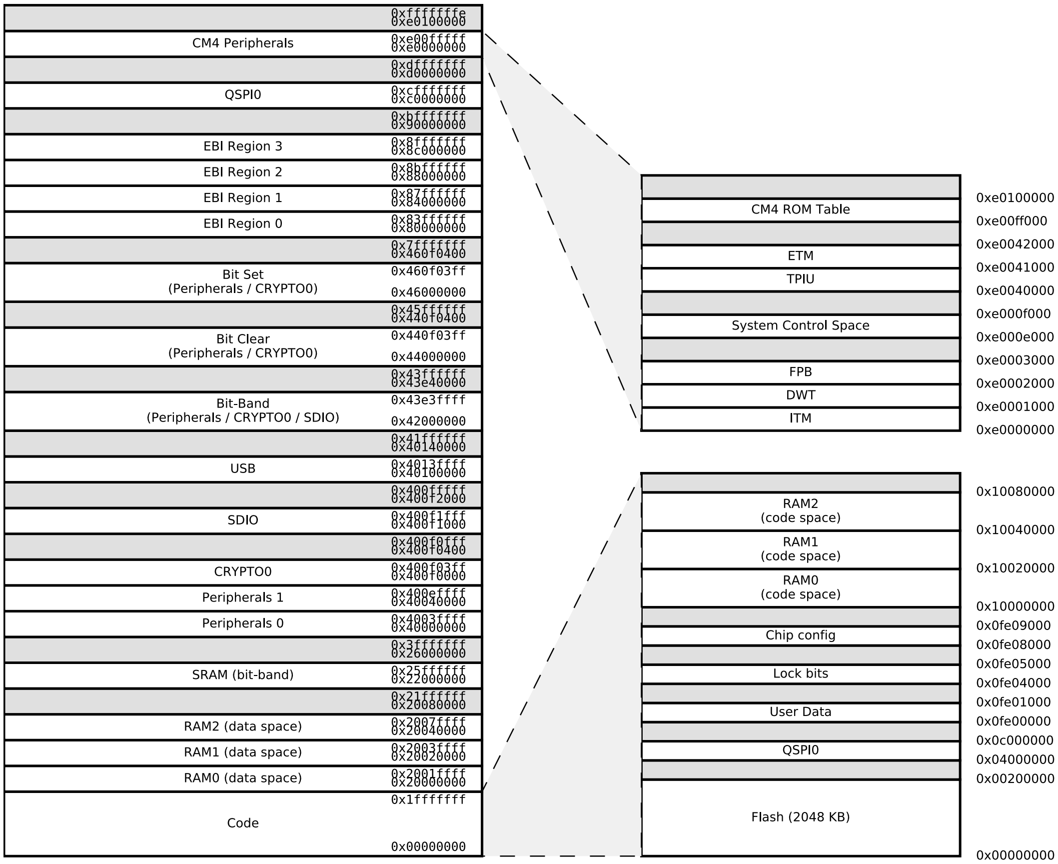


Figure 3.2. EFM32GG11 Memory Map — Core Peripherals and Code Space

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.
6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and $THETA_{JA}$.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN64 Package	$THETA_{JA\_QFN64}$	4-Layer PCB, Air velocity = 0 m/s	—	17.8	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	15.4	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	13.8	—	°C/W
Thermal resistance, TQFP64 Package	$THETA_{JA\_TQFP64}$	4-Layer PCB, Air velocity = 0 m/s	—	33.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	32.1	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	30.1	—	°C/W
Thermal resistance, TQFP100 Package	$THETA_{JA\_TQFP100}$	4-Layer PCB, Air velocity = 0 m/s	—	44.1	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	37.7	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	35.5	—	°C/W
Thermal resistance, BGA112 Package	$THETA_{JA\_BGA112}$	4-Layer PCB, Air velocity = 0 m/s	—	42.0	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	37.0	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	35.3	—	°C/W
Thermal resistance, BGA120 Package	$THETA_{JA\_BGA120}$	4-Layer PCB, Air velocity = 0 m/s	—	47.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	41.8	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	39.6	—	°C/W
Thermal resistance, BGA152 Package	$THETA_{JA\_BGA152}$	4-Layer PCB, Air velocity = 0 m/s	—	35.7	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	31.0	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	29.5	—	°C/W
Thermal resistance, BGA192 Package	$THETA_{JA\_BGA192}$	4-Layer PCB, Air velocity = 0 m/s	—	47.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	41.8	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	39.6	—	°C/W

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	3.9	—	μA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	4.3	—	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.8	TBD	μA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFRCO	—	3.6	TBD	μA
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	1.08	—	μA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.69	—	μA
		128 byte RAM retention, no RTCC	—	0.69	TBD	μA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.16	TBD	μA
Current consumption of peripheral power domain 1, with voltage scaling enabled	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[1]	—	0.68	—	μA
Current consumption of peripheral power domain 2, with voltage scaling enabled	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[1]	—	0.28	—	μA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.4 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.7.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.9. Current Consumption 1.8 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	72 MHz HFRCO, CPU running Prime from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	140	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	122	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	122	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	126	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	131	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	315	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	107	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	259	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	72 MHz HFRCO	—	57	—	µA/MHz
		50 MHz crystal	—	59	—	µA/MHz
		48 MHz HFRCO	—	59	—	µA/MHz
		32 MHz HFRCO	—	61	—	µA/MHz
		26 MHz HFRCO	—	63	—	µA/MHz
		16 MHz HFRCO	—	68	—	µA/MHz
		1 MHz HFRCO	—	252	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	55	—	µA/MHz
		1 MHz HFRCO	—	207	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	3.7	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	4.0	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.5	—	µA

4.1.8 Wake Up Times

Table 4.10. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	11.8	—	μs
		Code execution from RAM	—	4.1	—	μs
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	11.8	—	μs
		Code execution from RAM	—	4.1	—	μs
Wake up from EM4H[1]	t_{EM4H_WU}	Executing from flash	—	94	—	μs
Wake up from EM4S[1]	t_{EM4S_WU}	Executing from flash	—	294	—	μs
Time from release of reset source to first instruction execution	t_{RESET}	Soft Pin Reset released	—	55	—	μs
		Any other reset released	—	359	—	μs
Power mode scaling time	t_{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz[4] [2]	—	31.8	—	μs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz[3]	—	4.3	—	μs

Note:

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/μs for approximately 20 μs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).
3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 μs + 29 HFCLKs.
4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 μs + 28 HFCLKs.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
MISO hold time [1] [3]	t_{H_MI}	USART2, location 4, IOVDD = 1.8 V	-11.6	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	-11.6	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	-9.1	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	-9.1	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	-8	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	-8	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

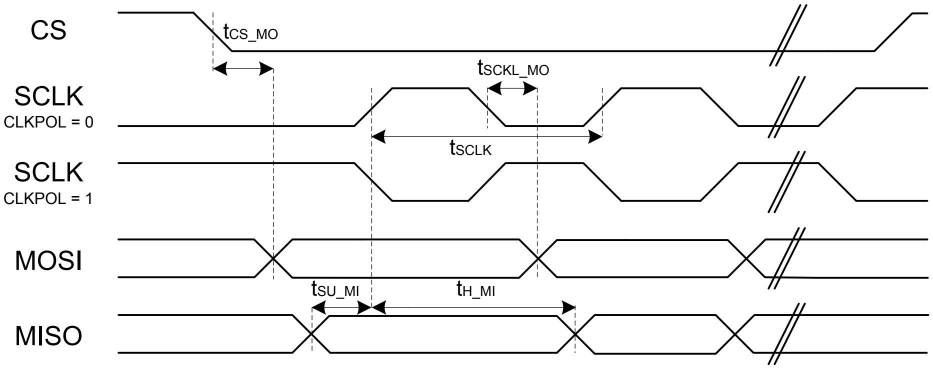


Figure 4.1. SPI Master Timing Diagram

4.1.25 External Bus Interface (EBI)

EBI Write Enable Output Timing

Timing applies to both EBI_WEn and EBI_NANDWEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.36. EBI Write Enable Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_WEn / EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid	t_{OH_WEn}	IOVDD ≥ 1.62 V	-22 + (WRHOLD * $t\{_{\}HFCORECLK\{}\}$)	—	—	ns
		IOVDD ≥ 3.0 V	-13 + (WRHOLD * $t_{HFCORECLK}$)	—	—	ns
Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_WEn / EBI_NANDWEn edge[1]	t_{OSU_WEn}	IOVDD ≥ 1.62 V	-12 + (WRSETUP * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-10 + (WRSETUP * $t_{HFCORECLK}$)	—	—	ns
EBI_WEn / EBI_NANDWEn pulse width[1]	t_{WIDTH_WEn}	IOVDD ≥ 1.62 V	-6 + (MAX(1, WRSTRB) * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-5 + (MAX(1, WRSTRB) * $t_{HFCORECLK}$)	—	—	ns

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of t_{WIDTH_WEn} and increases the length of t_{OSU_WEn} by 1/2 * $t_{HFCLKNODIV}$.

SDIO HS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.47. SDIO HS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	45	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	10.0	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	10.0	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.69	3.23	—	ns
Clock fall time	t_F		1.42	2.79	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}		0	—	13	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}		2	—	—	ns

SDIO DDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 30 pF on all pins.

Table 4.49. SDIO DS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.69	6.52	—	ns
Clock fall time	t_F		1.42	4.96	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		1.8	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		0.8	—	—	ns
Input setup time, DAT[0:3] valid to SD_CLK	t_{ISU2X}		6	—	—	ns
Input hold time, SD_CLK to DAT[0:3] change	t_{IH2X}		1.5	—	—	ns
Output delay time, SD_CLK to DAT[0:3] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:3] change	t_{OH2X}		0.8	—	—	ns

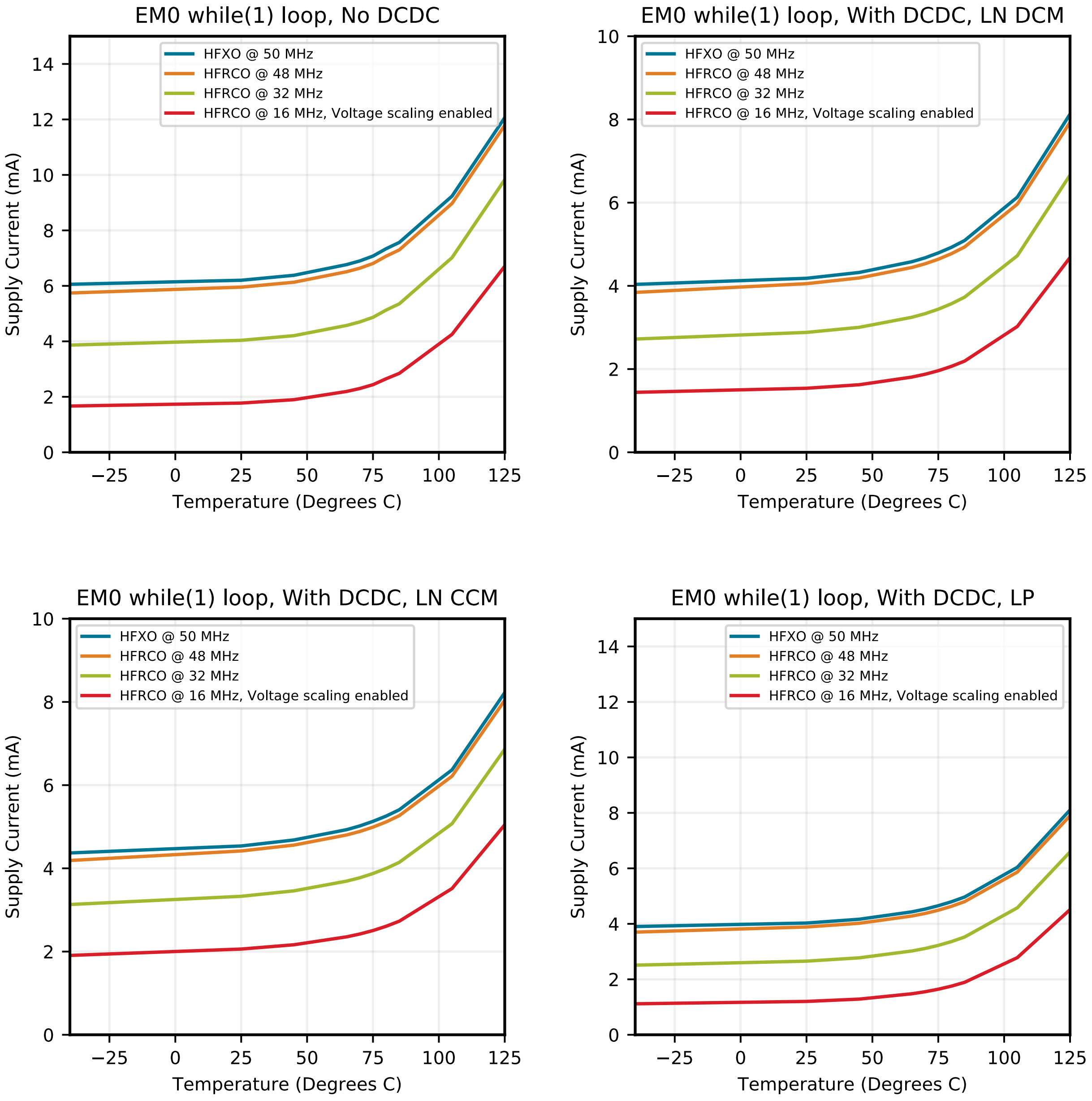


Figure 4.24. EM0 Active Mode Typical Supply Current vs. Temperature

5.5 EFM32GG11B4xx in BGA120 Device Pinout

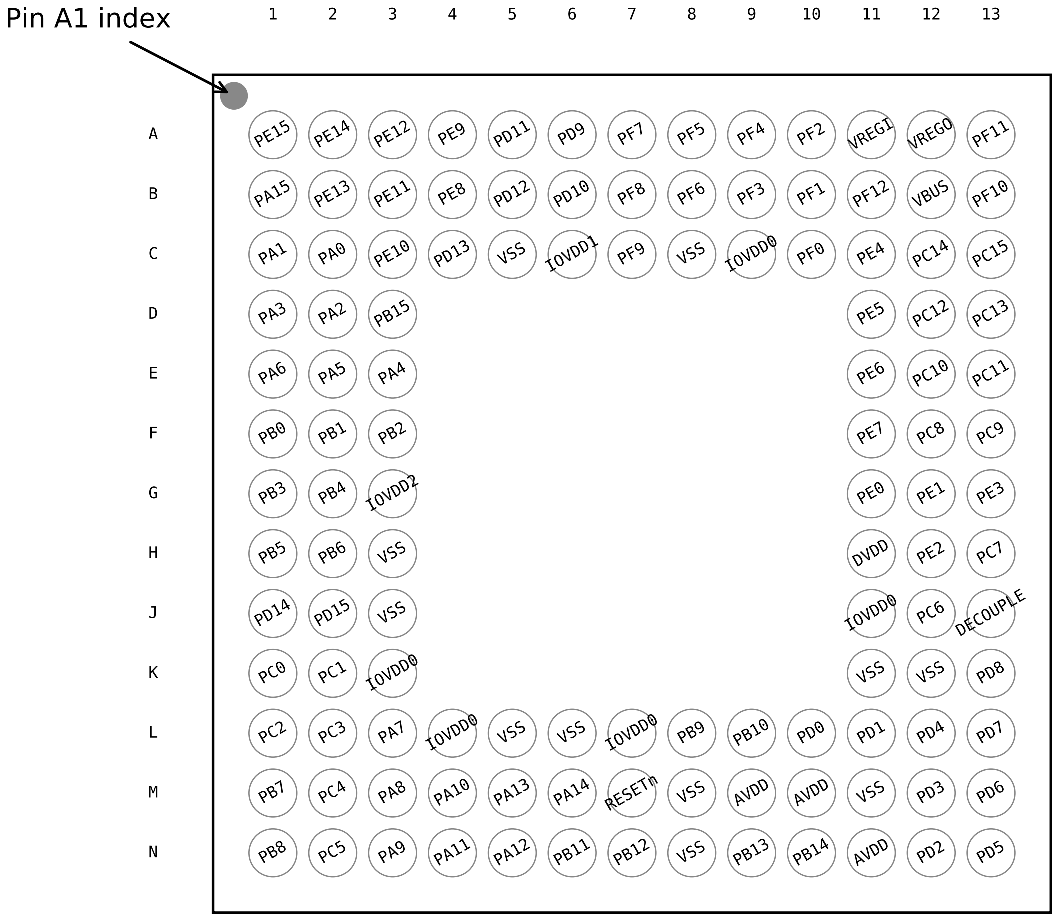


Figure 5.5. EFM32GG11B4xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.5. EFM32GG11B4xx in BGA120 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF4	A9	GPIO	PF2	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PD8	H8	GPIO	PD5	H9	GPIO
PD6	H10	GPIO	PD7	H11	GPIO
PC1	J1	GPIO (5V)	PC3	J2	GPIO (5V)
PD15	J3	GPIO (5V)	PA12	J4	GPIO (5V)
PA9	J5	GPIO	PA10	J6	GPIO
PB9	J7	GPIO (5V)	PB10	J8	GPIO (5V)
PD2	J9	GPIO (5V)	PD3	J10	GPIO
PD4	J11	GPIO	PB7	K1	GPIO
PC4	K2	GPIO	PA13	K3	GPIO (5V)
PA11	K5	GPIO	RESETn	K6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	K8 K9 L10	Analog power supply.	PD1	K11	GPIO
PB8	L1	GPIO	PC5	L2	GPIO
PA14	L3	GPIO	PB11	L5	GPIO
PB12	L6	GPIO	PB13	L8	GPIO
PB14	L9	GPIO	PD0	L11	GPIO (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF3	79	GPIO	PF4	80	GPIO
PF5	81	GPIO	PF6	84	GPIO
PF7	85	GPIO	PF8	86	GPIO
PF9	87	GPIO	PD9	88	GPIO
PD10	89	GPIO	PD11	90	GPIO
PD12	91	GPIO	PE8	92	GPIO
PE9	93	GPIO	PE10	94	GPIO
PE11	95	GPIO	PE12	96	GPIO
PE13	97	GPIO	PE14	98	GPIO
PE15	99	GPIO	PA15	100	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.18 EFM32GG11B4xx in QFN64 Device Pinout

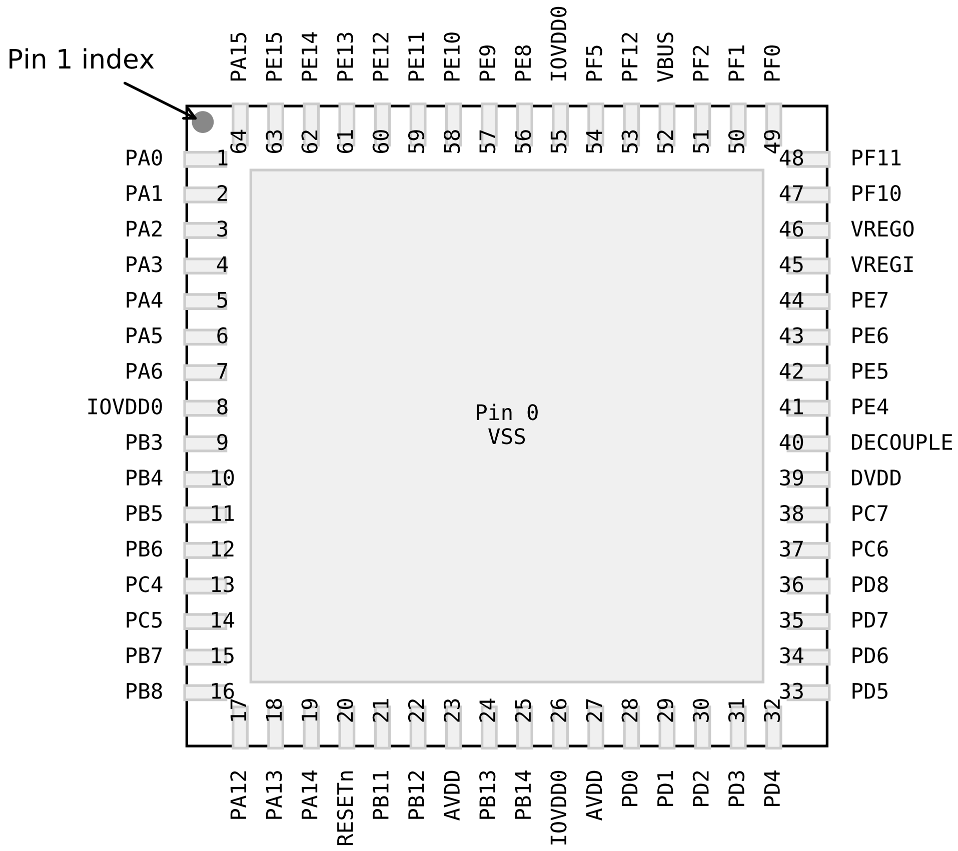


Figure 5.18. EFM32GG11B4xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.18. EFM32GG11B4xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

Table 5.31. VDAC0 / OPA Bus and Pin Mapping

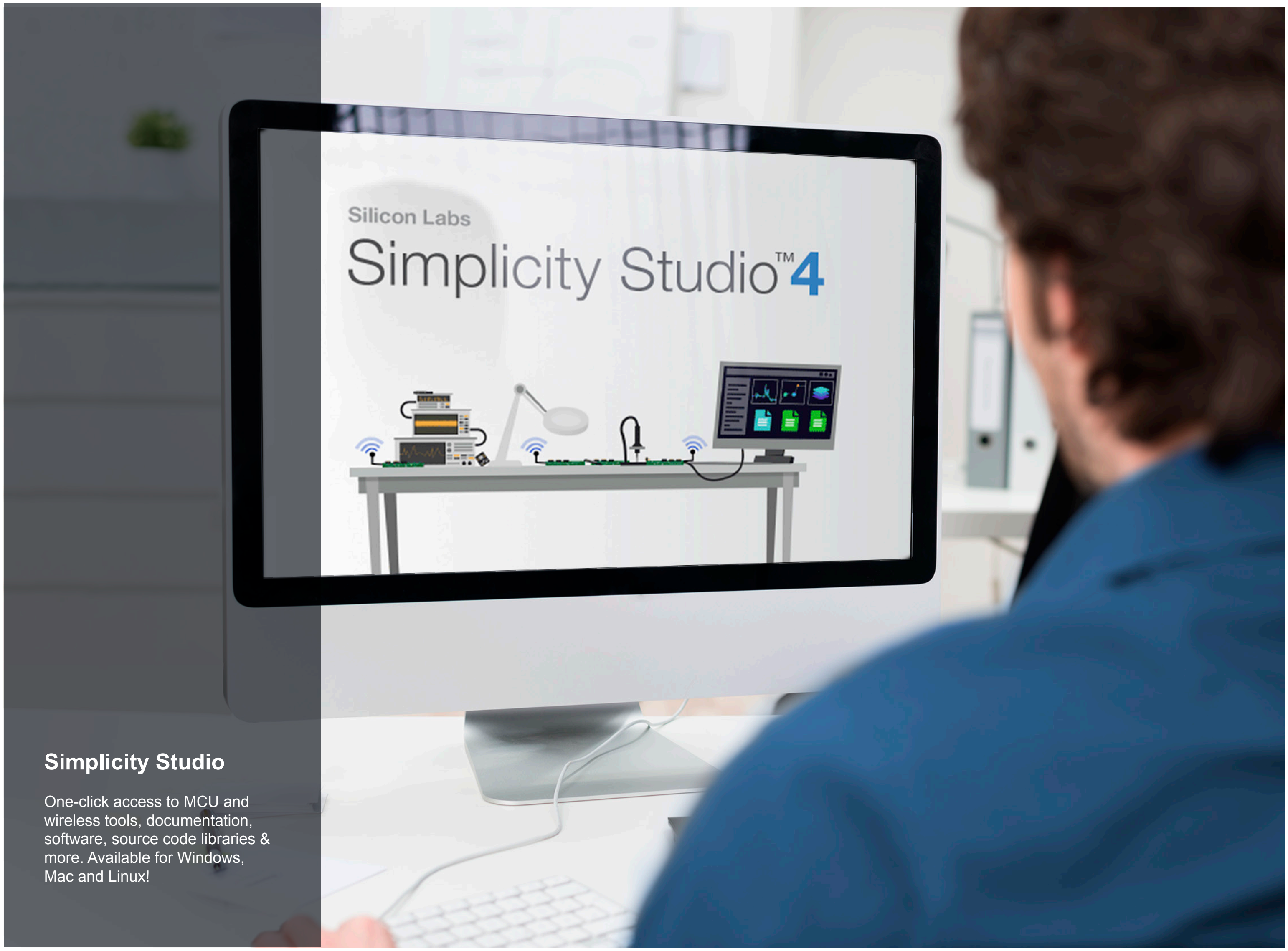
Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA0_N																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
OPA0_P																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	

Table 7.2. BGA152 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.20	
C1		6.50	
C2		6.50	
E1		0.5	
E2		0.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.



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