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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b120f2048iq64-b

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3. System Overview

3.1 Introduction

The Giant Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Giant Gecko Series 1 Reference Manual.

A block diagram of the Giant Gecko Series 1 family is shown in Figure 3.1 Detailed EFM32GG11 Block Diagram on page 11. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.



Figure 3.1. Detailed EFM32GG11 Block Diagram

3.2 Power

The EFM32GG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

4.1.16 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.24.	Digital to	Analog Converter	(VDAC)
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Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Output voltage	V _{DACOUT}	Single-Ended	0	_	V _{VREF}	V
		Differential ²	-V _{VREF}	_	V _{VREF}	V
Current consumption includ- ing references (2 channels) ¹	I _{DAC}	500 ksps, 12-bit, DRIVES- TRENGTH = 2, REFSEL = 4	_	402	_	μΑ
		44.1 ksps, 12-bit, DRIVES- TRENGTH = 1, REFSEL = 4	_	88	_	μΑ
		200 Hz refresh rate, 12-bit Sam- ple-Off mode in EM2, DRIVES- TRENGTH = 2, BGRREQTIME = 1, EM2REFENTIME = 9, REFSEL = 4, SETTLETIME = 0x0A, WAR- MUPTIME = 0x02		2		μA
Current from HFPERCLK ⁴	IDAC_CLK		_	5.25		µA/MHz
Sample rate	SR _{DAC}		_	_	500	ksps
DAC clock frequency	f _{DAC}		_	_	1	MHz
Conversion time	t _{DACCONV}	f _{DAC} = 1MHz	2	_	_	μs
Settling time	t _{DACSETTLE}	50% fs step settling to 5 LSB	_	2.5		μs
Startup time	t _{DACSTARTUP}	Enable to 90% fs output, settling to 10 LSB	_		12	μs
Output impedance	R _{OUT}	DRIVESTRENGTH = 2, 0.4 V \leq V _{OUT} \leq V _{OPA} - 0.4 V, -8 mA $<$ I _{OUT} $<$ 8 mA, Full supply range	_	2	_	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V $\leq V_{OUT} \leq V_{OPA}$ - 0.4 V, -400 μ A < I _{OUT} < 400 μ A, Full supply range	—	2	_	Ω
		$ \begin{array}{l} DRIVESTRENGTH = 2,\ 0.1\ V \leq \\ V_{OUT} \leq V_{OPA} - 0.1\ V,\ -2\ mA < \\ I_{OUT} < 2\ mA,\ Full \ supply \ range \end{array} $		2	_	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V $\leq V_{OUT} \leq V_{OPA} - 0.1 V$, -100 µA < I _{OUT} < 100 µA, Full supply range		2	_	Ω
Power supply rejection ratio ⁶	PSRR	Vout = 50% fs. DC	_	65.5	_	dB

4.1.19 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAIN-OUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes^{8 1}.

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Supply voltage (from AVDD)	V _{OPA}	HCMDIS = 0, Rail-to-rail input range	2	—	3.8	V
		HCMDIS = 1	1.62	_	3.8	V
Input voltage	V _{IN}	HCMDIS = 0, Rail-to-rail input range	V _{VSS}	_	V _{OPA}	V
		HCMDIS = 1	V _{VSS}	_	V _{OPA} -1.2	V
Input impedance	R _{IN}		100	_	—	MΩ
Output voltage	V _{OUT}		V _{VSS}	_	V _{OPA}	V
Load capacitance ²	C _{LOAD}	OUTSCALE = 0	_	—	75	pF
		OUTSCALE = 1	_	_	37.5	pF
Output impedance	R _{OUT}	$\label{eq:VOUT} \begin{array}{l} DRIVESTRENGTH = 2 \text{ or } 3, 0.4 \text{ V} \\ \leq V_{OUT} \leq V_{OPA} \text{ - } 0.4 \text{ V}, \text{ -8 mA } < \\ I_{OUT} < 8 \text{ mA}, \text{ Buffer connection}, \\ \text{Full supply range} \end{array}$	_	0.25		Ω
		$ DRIVESTRENGTH = 0 \text{ or } 1, 0.4 \text{ V} \\ \leq \text{V}_{\text{OUT}} \leq \text{V}_{\text{OPA}} - 0.4 \text{ V}, -400 \mu\text{A} < \\ \text{I}_{\text{OUT}} < 400 \mu\text{A}, \text{Buffer connection,} \\ \text{Full supply range} $	_	0.6	_	Ω
		$\label{eq:DRIVESTRENGTH} \begin{array}{l} DRIVESTRENGTH = 2 \mbox{ or } 3, \mbox{ 0.1 V} \\ \leq V_{OUT} \leq V_{OPA} - 0.1 \mbox{ V}, \mbox{ -2 mA} < \\ I_{OUT} < 2 \mbox{ mA}, \mbox{ Buffer connection}, \\ \mbox{ Full supply range} \end{array}$		0.4	_	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V $\leq V_{OUT} \leq V_{OPA} - 0.1 V$, -100 µA < $I_{OUT} < 100 µA$, Buffer connection, Full supply range	_	1	_	Ω
Internal closed-loop gain	G _{CL}	Buffer connection	TBD	1	TBD	-
		3x Gain connection	TBD	2.99	TBD	-
		16x Gain connection	TBD	15.7	TBD	-
Active current ⁴	I _{OPA}	DRIVESTRENGTH = 3, OUT- SCALE = 0	—	580	_	μA
		DRIVESTRENGTH = 2, OUT- SCALE = 0	_	176	_	μA
		DRIVESTRENGTH = 1, OUT- SCALE = 0	—	13	_	μA
		DRIVESTRENGTH = 0, OUT- SCALE = 0	_	4.7	_	μA

Table 4.27. Operational Amplifier (OPAMP)

4.1.24 USART SPI

SPI Master Timing

Table 4.34. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
SCLK period ^{1 3 2}	t _{SCLK}	All USARTs except USART2	2 * ^t HFPERCLK	—	_	ns
		USART2	2 * t _{HFPERBCLK}	_	_	ns
CS to MOSI ^{1 3}	t _{CS_MO}	USART2, location 4, IOVDD = 1.8 V	-3.2	—	6.8	ns
		USART2, location 4, IOVDD = 3.0 V	-2.3		6.0	ns
		USART2, location 5, IOVDD = 1.8 V	-8.1	_	6.3	ns
		USART2, location 5, IOVDD = 3.0 V	-7.3	_	4.4	ns
		All other USARTs and locations, IOVDD = 1.8 V	-15	_	13	ns
		All other USARTs and locations, IOVDD = 3.0 V	-13	_	11	ns
SCLK to MOSI ^{1 3}	t _{SCLK_MO}	USART2, location 4, IOVDD = 1.8 V	-0.3	—	9.2	ns
		USART2, location 4, IOVDD = 3.0 V	-0.3	—	8.6	ns
		USART2, location 5, IOVDD = 1.8 V	-3.6	_	5.0	ns
		USART2, location 5, IOVDD = 3.0 V	-3.4	—	3.2	ns
		All other USARTs and locations, IOVDD = 1.8 V	-10	—	11	ns
		All other USARTs and locations, IOVDD = 3.0 V	-9	_	11	ns
MISO setup time ^{1 3}	t _{SU_MI}	USART2, location 4, IOVDD = 1.8 V	39.7	_	_	ns
		USART2, location 4, IOVDD = 3.0 V	22.4	_	_	ns
		USART2, location 5, IOVDD = 1.8 V	49.2	_	_	ns
		USART2, location 5, IOVDD = 3.0 V	30.0	—	_	ns
		All other USARTs and locations, IOVDD = 1.8 V	55		_	ns
		All other USARTs and locations, IOVDD = 3.0 V	36	_	_	ns

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
SCLK period ^{1 3 2}	t _{SCLK}		6 * t _{HFPERCLK}	—	—	ns
SCLK high time ^{1 3 2}	t _{SCLK_HI}		2.5 * t _{HFPERCLK}	—	—	ns
SCLK low time ^{1 3 2}	t _{SCLK_LO}		2.5 * t _{HFPERCLK}	—	—	ns
CS active to MISO ^{1 3}	t _{CS_ACT_MI}		24	_	69	ns
CS disable to MISO ^{1 3}	t _{CS_DIS_MI}		19	_	175	ns
MOSI setup time ^{1 3}	t _{SU_MO}		7	_	—	ns
MOSI hold time ^{1 3 2}	t _{H_MO}		6	_	—	ns
SCLK to MISO ^{1 3 2}	t _{SCLK_MI}		16 + 1.5 * t _{HFPERCLK}	—	43 + 2.5 * ^t HFPERCLK	ns

Table 4.35. SPI Slave Timing

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).

2. t_{HFPERCLK} is one period of the selected HFPERCLK.

3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).



Figure 4.2. SPI Slave Timing Diagram

SDIO MMC DDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Clock frequency during data transfer	F _{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	_	20	MHz
		Using HFXO	_	_	TBD	MHz
Clock low time	t _{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6		_	ns
		Using HFXO	TBD	_	—	ns
Clock high time	t _{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6		_	ns
		Using HFXO	TBD		_	ns
Clock rise time	t _R		1.13	2.37	—	ns
Clock fall time	t _F		1.01	2.02	_	ns
Input setup time, CMD valid to SD_CLK	t _{ISU}		5.3			ns
Input hold time, SD_CLK to CMD change	t _{IH}		2.5	_	_	ns
Output delay time, SD_CLK to CMD valid	t _{ODLY}		0	_	16	ns
Output hold time, SD_CLK to CMD change	t _{OH}		3		_	ns
Input setup time, DAT[0:7] valid to SD_CLK	t _{ISU2X}		5.3		_	ns
Input hold time, SD_CLK to DAT[0:7] change	t _{IH2X}		2.5		_	ns
Output delay time, SD_CLK to DAT[0:7] valid	t _{ODLY2X}		0		16	ns
Output hold time, SD_CLK to DAT[0:7] change	t _{OH2X}		3			ns

Table 4.53. SDIO MMC DDR Mode Timing (Location 0, 3V I/O)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA15	B1	GPIO	PE14	B2	GPIO
PE12	B3	GPIO	PE8	B4	GPIO
PD11	B5	GPIO	PD9	B6	GPIO
PF8	B7	GPIO	PF6	B8	GPIO
PF14	B9	GPIO (5V)	PF12	B10	GPIO
PF2	B11	GPIO	PF0	B12	GPIO (5V)
PC14	B13	GPIO (5V)	VREGO	B14	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs
PA1	C1	GPIO	PA0	C2	GPIO
PD13	C3	GPIO (5V)	PE10	C4	GPIO
PI8	C5	GPIO (5V)	PI7	C6	GPIO (5V)
Pl6	C7	GPIO (5V)	PF5	C8	GPIO
PF15	C9	GPIO (5V)	PF4	C10	GPIO
PF3	C11	GPIO	PC13	C12	GPIO (5V)
PC12	C13	GPIO (5V)	VREGI	C14	Input to 5 V regulator.
PA3	D1	GPIO	PA2	D2	GPIO
PD14	D3	GPIO (5V)	PC11	D12	GPIO (5V)
PC10	D13	GPIO (5V)	PC9	D14	GPIO (5V)
PA5	E1	GPIO	PA4	E2	GPIO
PD15	E3	GPIO (5V)	IOVDD1	E6	Digital IO power supply 1.
VSS	E7 E8 G5 G7 G8 G10 H5 H7 H8 H10 K7 K8	Ground	IOVDD0	E9 F10 J5 J10 K6 K9	Digital IO power supply 0.
PC8	E12	GPIO (5V)	PI5	E13	GPIO (5V)
Pl4	E14	GPIO (5V)	PG0	F1	GPIO (5V)
PA6	F2	GPIO	PG1	F3	GPIO (5V)
IOVDD2	F5	Digital IO power supply 2.	PI3	F12	GPIO (5V)
PI2	F13	GPIO (5V)	PI1	F14	GPIO (5V)
PG3	G1	GPIO (5V)	PG4	G2	GPIO (5V)
PG2	G3	GPIO (5V)	PE7	G12	GPIO
P10	G13	GPIO (5V)	DECOUPLE	G14	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC1	J1	GPIO (5V)	PC3	J2	GPIO (5V)
PD15	J3	GPIO (5V)	PA12	J4	GPIO (5V)
PA9	J5	GPIO	PA10	J6	GPIO
PB9	J7	GPIO (5V)	PB10	J8	GPIO (5V)
PD2	J9	GPIO (5V)	PD3	J10	GPIO
PD4	J11	GPIO	PB7	K1	GPIO
PC4	K2	GPIO	PA13	K3	GPIO (5V)
PA11	K5	GPIO	RESETn	K6	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	K8 K9 L10	Analog power supply.	PD1	K11	GPIO
PB8	L1	GPIO	PC5	L2	GPIO
PA14	L3	GPIO	PB11	L5	GPIO
PB12	L6	GPIO	PB13	L8	GPIO
PB14	L9	GPIO	PD0	L11	GPIO (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.



Figure 5.15. EFM32GG11B1xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.15. EFN	132GG11B1xx in	QFP64 Device	Pinout
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 26 55	Digital IO power supply 0.	VSS	8 22 56	Ground
PC0	9	GPIO (5V)	PC1	10	GPIO (5V)
PC2	11	GPIO (5V)	PC3	12	GPIO (5V)



Figure 5.17. EFM32GG11B5xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.17. EFM32GG11B5xx in QFN64 Device Pino	ut
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 27 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

5.21 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 5.20 GPIO Functionality Table for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ACMP0_O	0: PE13 1: PE2 2: PD6 3: PB11	4: PA6 5: PB0 6: PB2 7: PB3	Analog comparator ACMP0, digital output.
ACMP1_O	0: PF2 1: PE3 2: PD7 3: PA12	4: PA14 5: PB9 6: PB10 7: PA5	Analog comparator ACMP1, digital output.
ACMP2_O	0: PD8 1: PE0 2: PE1 3: PI0	4: Pl1 5: Pl2	Analog comparator ACMP2, digital output.
ACMP3_O	0: PF0 1: PC15 2: PC14 3: PC13	4: Pl4 5: Pl5	Analog comparator ACMP3, digital output.
ADC0_EXTN	0: PD7		Analog to digital converter ADC0 external reference input negative pin.
ADC0_EXTP	0: PD6		Analog to digital converter ADC0 external reference input positive pin.
ADC1_EXTN	0: PD7		Analog to digital converter ADC1 external reference input negative pin.
ADC1_EXTP	0: PD6		Analog to digital converter ADC1 external reference input positive pin.
BOOT_RX	0: PF1		Bootloader RX.
BOOT_TX	0: PF0		Bootloader TX.

Table 5.21. Alternate Functionality Overview

Alternate	LOCA		
Functionality	0 - 3	4 - 7	Description
ETH_MIITXD2	0: PA2 1: PG2		Ethernet MII Transmit Data Bit 2.
ETH_MIITXD3	0: PA1 1: PG1		Ethernet MII Transmit Data Bit 3.
ETH_MIITXEN	0: PA5 1: PG5		Ethernet MII Transmit Enable.
ETH_MIITXER	0: PA6 1: PG6		Ethernet MII Transmit Error.
ETH_RMIICRSDV	0: PA4 1: PD11		Ethernet RMII Carrier Sense / Data Valid.
ETH_RMIIREFCLK	0: PA3 1: PD10		Ethernet RMII Reference Clock.
ETH_RMIIRXD0	0: PA2 1: PD9		Ethernet RMII Receive Data Bit 0.
ETH_RMIIRXD1	0: PA1 1: PF9		Ethernet RMII Receive Data Bit 1.
ETH_RMIIRXER	0: PA5 1: PD12		Ethernet RMII Receive Error.
ETH_RMIITXD0	0: PE15 1: PF7		Ethernet RMII Transmit Data Bit 0.
ETH_RMIITXD1	0: PE14 1: PF6		Ethernet RMII Transmit Data Bit 1.
ETH_RMIITXEN	0: PA0 1: PF8		Ethernet RMII Transmit Enable.
ETH_TSUEXTCLK	0: PB5 1: PD15 2: PC2 3: PF8		Ethernet IEEE1588 External Reference Clock.

Alternate	LOCA		
Functionality	0 - 3	4 - 7	Description
LES_ALTEX6	0: PE12		LESENSE alternate excite output 6.
LES_ALTEX7	0: PE13		LESENSE alternate excite output 7.
LES_CH0	0: PC0		LESENSE channel 0.
LES_CH1	0: PC1		LESENSE channel 1.
LES_CH2	0: PC2		LESENSE channel 2.
LES_CH3	0: PC3		LESENSE channel 3.
LES_CH4	0: PC4		LESENSE channel 4.
LES_CH5	0: PC5		LESENSE channel 5.
LES_CH6	0: PC6		LESENSE channel 6.
LES_CH7	0: PC7		LESENSE channel 7.
LES_CH8	0: PC8		LESENSE channel 8.
LES_CH9	0: PC9		LESENSE channel 9.
LES_CH10	0: PC10		LESENSE channel 10.

Alternate	LOCA		
Functionality	0 - 3	4 - 7	Description
PCNT0_S0IN	0: PC13 1: PE0 2: PC0 3: PD6	4: PA0 5: PB0 6: PB5 7: PB12	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PC14 1: PE1 2: PC1 3: PD7	4: PA1 5: PB1 6: PB6 7: PB11	Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	0: PA5 1: PB3 2: PD15 3: PC4	4: PA7 5: PA12 6: PB11 7: PG14	Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	0: PA6 1: PB4 2: PB0 3: PC5	4: PA8 5: PA13 6: PB12 7: PG15	Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	0: PD0 1: PE8 2: PB13 3: PF10	4: PC12 5: PI2 6: PI0 7: PH14	Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	0: PD1 1: PE9 2: PB14 3: PF11	4: PC13 5: PI1 6: PH15 7: PH13	Pulse Counter PCNT2 input number 1.
PRS_CH0	0: PA0 1: PF3 2: PC14 3: PF2		Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PA1 1: PF4 2: PC15 3: PE12		Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PC0 1: PF5 2: PE10 3: PE13		Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PC1 1: PE8 2: PE11 3: PA0		Peripheral Reflex System PRS, channel 3.
PRS_CH4	0: PC8 1: PB0 2: PF1		Peripheral Reflex System PRS, channel 4.
PRS_CH5	0: PC9 1: PB1 2: PD6		Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA6 1: PB14 2: PE6		Peripheral Reflex System PRS, channel 6.

Alternate LOCATION		ATION	
Functionality	0 - 3	4 - 7	Description
US3_RTS	0: PA5 1: PC1 2: PA14 3: PC15	4: PG5 5: PG11	USART3 Request To Send hardware flow control output.
US3_RX	0: PA1 1: PE7 2: PB7 3: PG7	4: PG1 5: PI13	USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).
US3_TX	0: PA0 1: PE6 2: PB3 3: PG6	4: PG0 5: PI12	USART3 Asynchronous Transmit. Also used as receive input in half duplex communica- tion. USART3 Synchronous mode Master Output / Slave Input (MOSI).
US4_CLK	0: PC4 1: PD11 2: PI2 3: PI8	4: PH6	USART4 clock input / output.
US4_CS	0: PC5 1: PD12 2: PI3 3: PI9	4: PH7	USART4 chip select input / output.
US4_CTS	0: PA7 1: PD13 2: PI4 3: PI10	4: PH8	USART4 Clear To Send hardware flow control input.
US4_RTS	0: PA8 1: PD14 2: PI5 3: PI11	4: PH9	USART4 Request To Send hardware flow control output.
US4_RX	0: PB8 1: PD10 2: PI1 3: PI7	4: PH5	USART4 Asynchronous Receive. USART4 Synchronous mode Master Input / Slave Output (MISO).
US4_TX	0: PB7 1: PD9 2: PI0 3: PI6	4: PH4	USART4 Asynchronous Transmit. Also used as receive input in half duplex communica- tion. USART4 Synchronous mode Master Output / Slave Input (MOSI).
US5_CLK	0: PB11 1: PD13 2: PF13 3: PH12		USART5 clock input / output.
US5_CS	0: PB13 1: PD14 2: PF12 3: PH13		USART5 chip select input / output.
US5_CTS	0: PB14 1: PD15 2: PF11 3: PH14		USART5 Clear To Send hardware flow control input.
US5_RTS	0: PB12 1: PB15 2: PF10 3: PH15		USART5 Request To Send hardware flow control output.

7.2 BGA152 PCB Land Pattern



Figure 7.2. BGA152 PCB Land Pattern Drawing



Figure 9.3. BGA112 Package Marking

The package marking consists of:

- PPPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.

Table 12.2. QFN64 PCB Land Pattern Dimensions

Dimension	Тур
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	7.30
Y2	7.30

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This Land Pattern Design is based on the IPC-7351 guidelines.

3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

6. The stencil thickness should be 0.125 mm (5 mils).

7. The ratio of stencil aperture to land pad size can be 1:1 for all pads.

8. A 3x3 array of 1.45 mm square openings on a 2.00 mm pitch can be used for the center ground pad.

9. A No-Clean, Type-3 solder paste is recommended.

10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



Figure 12.3. QFN64 Package Marking

The package marking consists of:

- PPPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.