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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

# Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

## Details

E·XFI

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I <sup>2</sup> C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	90
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b320f2048gl112-a

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### 3.4.2 Internal and External Oscillators

The EFM32GG11 supports two crystal oscillators and fully integrates five RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 50 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (USHFRCO) is available for timing the USB, SDIO and QSPI peripherals. The USHFRCO can be syncronized to the host's USB clock to allow the USB to operate in device mode without the additional cost of an external crystal.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

#### 3.5 Counters/Timers and PWM

#### 3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER\_0 only.

#### 3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER\_0 only.

#### 3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

#### 3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of wave-forms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

#### 3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

# 3.11 Memory Map

The EFM32GG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

	8xfq1qqqe	]		
CM4 Peripherals	8xe88fffff			
	8×85555555			
QSPIO	0xcfffffff			
	8886666666			
EBI Region 3	8×855555555			
EBI Region 2	8×8844444	i \		
EBI Region 1	8×87555555			0xe0100000
EBI Region 0	8×83555555		CM4 ROM Table	0xe00ff000
5	8×7fffffff			0xe0042000
Bit Set	0x460f03ff		EIM	0xe0041000
(Peripherals / CRYPTO0)	0×46000000		TPIO	0xe0040000
	8×455F5455	) `, F	System Control Space	0xe000f000
Bit Clear (Paripherals / CRXPTOD)	0x440f03ff		b)stern control opace	0xe000e000
(Feripherals / CKTF100)	0x44000000 0x43ffffff		FPB	0xe0003000
Pit Pand	0x43e40000 0x43e3ffff		DWT	0xe0002000
(Peripherals / CRYPTO0 / SDIO)	0×42000000		ITM	0xe0001000
	8×41146666	1 -		0xe0000000
USB	8×48136666	1 _		
	8×488‡£555	1 /-	DAMO	0x10080000
SDIO	8×488f1666	1 /	(code space)	0100.40000
	8×488f8455		RAM1	0X10040000
CRYPT00	8×488‡8355	1 / -	(code space)	0x10020000
Peripherals 1	8×48825555		(code space)	0
Peripherals 0	8×48834444			0x10000000 0x0fe09000
	8×36666666	1 / F	Chip config	0x0fe08000
SRAM (bit-band)	8×355555555		Lock bits	0x0fe05000
	8×21ffffff			0x0fe04000
RAM2 (data space)	8×28871111		User Data	0x0fe00000
RAM1 (data space)	8×2883ffff		QSPI0	0x0c000000
BAMO (data space)	0x20020000 0x2001ffff	1/		0x04000000 0x00200000
(data space)	0x1ffffff	f T		0.00200000
Code			F <b>l</b> ash (2048 KB)	
	0×000000000			0×00000000
				- 0.000000000

Figure 3.2. EFM32GG11 Memory Map — Core Peripherals and Code Space

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
ADC clock frequency	f <sub>ADCCLK</sub>		_	_	16	MHz
Throughput rate	fADCRATE		_	—	1	Msps
Conversion time <sup>1</sup>	t <sub>ADCCONV</sub>	6 bit	_	7	_	cycles
		8 bit	_	9	_	cycles
		12 bit		13		cycles
Startup time of reference	t <sub>ADCSTART</sub>	WARMUPMODE <sup>4</sup> = NORMAL	_	_	5	μs
generator and ADC core		WARMUPMODE <sup>4</sup> = KEEPIN- STANDBY			2	μs
		WARMUPMODE <sup>4</sup> = KEEPINSLO- WACC	_		1	μs
SNDR at 1Msps and f <sub>IN</sub> = 10kHz	SNDR <sub>ADC</sub>	Internal reference <sup>7</sup> , differential measurement	TBD	67	_	dB
		External reference <sup>6</sup> , differential measurement	_	68	_	dB
Spurious-free dynamic range (SFDR)	SFDR <sub>ADC</sub>	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL <sub>ADC</sub>	12 bit resolution, No missing co- des	TBD		TBD	LSB
Integral non-linearity (INL), End point method	INL <sub>ADC</sub>	12 bit resolution	TBD		TBD	LSB
Offset error	VADCOFFSETERR		TBD	0	TBD	LSB
Gain error in ADC	VADCGAIN	Using internal reference	_	-0.2	TBD	%
		Using external reference	_	-1	—	%
Temperature sensor slope	V <sub>TS_SLOPE</sub>			-1.84		mV/°C

Note:

1. Derived from ADCCLK.

2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU\_PWRCTRL.

3. In ADCn\_BIASPROG register.

4. In ADCn CNTL register.

5. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU PWRCTRL ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.

6. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL\_REF or SCANCTRL\_REF register field and VREFP in the SINGLECTRLX\_VREFSEL or SCANCTRLX\_VREFSEL field. The differential input range with this configuration is ± 1.25 V.

7. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL\_REF or SCANCTRL\_REF register field. The differential input range with this configuration is ± 1.25 V. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.

# **EBI TFT Output Timing**

All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

# Table 4.39. EBI TFT Output Timing

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Output hold time, EBI_DCLK to EBI_AD invalid	toh_dclk	IOVDD ≥ 1.62 V	-23 + (TFTHOLD <sup>* t</sup> нғсоя- есік)	_	_	ns
		IOVDD ≥ 3.0 V	-12 + (TFTHOLD <sup>* t</sup> нFCOR- ECLK)	_		ns
Output setup time, EBI_AD valid to EBI_DCLK	tosu_dclk	IOVDD ≥ 1.62 V	-11 + (TFTSET- UP * <sup>t</sup> HFCOR- ECLK)	_	_	ns
		IOVDD ≥ 3.0 V	-9 + (TFTSET- UP * t <sub>HFCOR-</sub> ECLK)	_	_	ns



Figure 4.6. EBI TFT Output Timing

#### SDIO SDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD\_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO\_CTRL\_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Clock frequency during data transfer	F <sub>SD_CLK</sub>	Using HFRCO, AUXHFRCO, or USHFRCO	_	_	20	MHz
		Using HFXO	_	_	TBD	MHz
Clock low time	t <sub>WL</sub>	Using HFRCO, AUXHFRCO, or USHFRCO	22.6			ns
		Using HFXO	TBD	—	_	ns
Clock high time	t <sub>WH</sub>	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	_	_	ns
		Using HFXO	TBD	_	_	ns
Clock rise time	t <sub>R</sub>		0.99	4.68	_	ns
Clock fall time	t <sub>F</sub>		0.90	3.64	_	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t <sub>ISU</sub>		8	_		ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t <sub>IH</sub>		1.5	_		ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t <sub>ODLY</sub>		0	—	35	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t <sub>OH</sub>		0.8	_	_	ns

# Table 4.48. SDIO SDR Mode Timing (Location 0)



Figure 4.18. SDIO MMC SDR Mode Timing



Figure 4.19. SDIO MMC DDR Mode Timing

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
IOVDD1	F7 G7	Digital IO power supply 1.	VSS	F8 G9 H6 H7 H8 H9 H10 H11 J6 J7 J8 J9 J10 J11 K8 K9 L8 L9	Ground
NC	F9	No Connect.	IOVDD0	F10 F11 G10 G11 K6 K7 K10 K11 L6 L7 L10 L11	Digital IO power supply 0.
PI5	F14	GPIO (5V)	PI4	F15	GPIO (5V)
PI3	F16	GPIO (5V)	PA5	G1	GPIO
PG6	G2	GPIO (5V)	PG5	G3	GPIO (5V)
PI2	G14	GPIO (5V)	PI1	G15	GPIO (5V)
PI0	G16	GPIO (5V)	PA6	H1	GPIO
PG8	H2	GPIO (5V)	PG7	H3	GPIO (5V)
PE5	H14	GPIO	PE6	H15	GPIO
PE7	H16	GPIO	PG11	J1	GPIO (5V)
PG10	J2	GPIO (5V)	PG9	J3	GPIO (5V)
PE3	J14	GPIO	PE4	J15	GPIO
DECOUPLE	J16	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PG14	K1	GPIO
PG13	K2	GPIO	PG12	K3	GPIO
PE1	K14	GPIO (5V)	PE2	K15	GPIO
DVDD	K16	Digital power supply.	PG15	L1	GPIO (5V)
PB15	L2	GPIO (5V)	PB0	L3	GPIO
PE0	L14	GPIO (5V)	PC7	L15	GPIO
VREGVDD	L16	Voltage regulator VDD input	PB1	M1	GPIO



#### Figure 5.2. EFM32GG11B8xx in BGA152 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.2. EFM32GG11B8xx in BGA152 D	Device Pinout
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE13	A2	GPIO
PE11	A3	GPIO	PE9	A4	GPIO
PD12	A5	GPIO	PD10	A6	GPIO
PF9	A7	GPIO	PF7	A8	GPIO
PF13	A9	GPIO (5V)	VBUS	A10	USB VBUS signal and auxiliary input to 5 V regulator.
PF1	A11	GPIO (5V)	PC15	A12	GPIO (5V)
PF11	A13	GPIO (5V)	PF10	A14	GPIO (5V)



## Figure 5.13. EFM32GG11B5xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.13. EFM32GG11B5xx in QFP64 Device Pinor
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_CH11	0: PC11		LESENSE channel 11.
LES_CH12	0: PC12		LESENSE channel 12.
LES_CH13	0: PC13		LESENSE channel 13.
LES_CH14	0: PC14		LESENSE channel 14.
LES_CH15	0: PC15		LESENSE channel 15.
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4	4: PE12 5: PC14 6: PA8 7: PB9	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9 7: PB10	Low Energy Timer LETIM0, output channel 1.
LETIM1_OUT0	0: PA7 1: PA11 2: PA12 3: PC2	4: PB5 5: PB2 6: PG0 7: PG2	Low Energy Timer LETIM1, output channel 0.
LETIM1_OUT1	0: PA6 1: PA13 2: PA14 3: PC3	4: PB6 5: PB1 6: PG1 7: PG3	Low Energy Timer LETIM1, output channel 1.
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	0: PC7 1: PA6 2: PD3 3: PB1	4: PB5 5: PH1	LEUART1 Receive input.
LEU1_TX	0: PC6 1: PA5 2: PD2 3: PB0	4: PB4 5: PH0	LEUART1 Transmit output. Also used as receive input in half duplex communication.

Alternate	LOCA	TION	
Functionality	0 - 3	4 - 7	Description
LFXTAL_N	0: PB8		Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional ex- ternal clock input pin.
LFXTAL_P	0: PB7		Low Frequency Crystal (typically 32.768 kHz) positive pin.
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.
OPA1_N	0: PD7		Operational Amplifier 1 external negative input.
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.
OPA2_N	0: PD3		Operational Amplifier 2 external negative input.
OPA2_OUT	0: PD5		Operational Amplifier 2 output.
OPA2_OUTALT	0: PD0		Operational Amplifier 2 alternative output.
OPA2_P	0: PD4		Operational Amplifier 2 external positive input.
OPA3_N	0: PC7		Operational Amplifier 3 external negative input.
OPA3_OUT	0: PD1		Operational Amplifier 3 output.
OPA3_P	0: PC6		Operational Amplifier 3 external positive input.

#### 5.22 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 5.20 APORT Connection Diagram on page 211 shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.





Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT\_\_), and the channel identifier (CH\_\_). For example, if pin PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	СНЗ	CH2	CH1	CH0
<b>APORT0X</b>	BUSADC1X																									2Hd	9Hd	PH5	PH4	EH4	PH2	PH1	ЬНО
<b>APORT0Y</b>	<b>BUSADC1Y</b>																									2Hd	9Hd	5HG	PH4	EH4	PH2	PH1	ЬНО
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		6A9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		6Yd		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		63d		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

# Table 5.28. ADC1 Bus and Pin Mapping

#### 6.2 BGA192 PCB Land Pattern



Figure 6.2. BGA192 PCB Land Pattern Drawing



Figure 8.3. BGA120 Package Marking

The package marking consists of:

- PPPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.

## 9.2 BGA112 PCB Land Pattern



Figure 9.2. BGA112 PCB Land Pattern Drawing

# 12. QFN64 Package Specifications

# 12.1 QFN64 Package Dimensions



Figure 12.1. QFN64 Package Drawing

Dimension	Min	Тур	Max								
A	0.70	0.75	0.80								
A1	0.00	_	0.05								
b	0.20	0.25	0.30								
A3	0.203 REF										
D	9.00 BSC										
е	0.50 BSC										
E	9.00 BSC										
D2	7.10	7.20	7.30								
E2	7.10	7.20	7.30								
L	0.40	0.45	0.50								
L1	0.00	_	0.10								
ааа	0.10										
bbb	0.10										
ссс	0.10										
ddd	0.05										
eee	0.08										

## Table 12.1. QFN64 Package Dimensions

# Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 13. Revision History

# **Revision 0.6**

March, 2018

- Removed "Confindential" watermark.
- · Updated 4.1 Electrical Characteristics and 4.2 Typical Performance Curves with latest characterization data.

## Revision 0.2

October, 2017

- · Updated memory maps to latest formatting and to include all peripherals.
- Updated all electrical specifications tables with latest characterization results.
- Absolute Maximum Ratings Table:
  - Removed redundant I<sub>VSSMAX</sub> line.
  - Added footnote to clarify V<sub>DIGPIN</sub> specification for 5V tolerant GPIO.
- General Operating Conditions Table:
  - Removed dV<sub>DD</sub> specification and redundant footnote about shorting VREGVDD and AVDD together.
  - Added footnote about IOVDD voltage restriction when CSEN peripheral is used with chopping enabled.
- Flash Memory Characteristics Table: Added timing measurement clarification for Device Erase and Mass Erase.
- · Analog to Digital Converter (ADC) Table:
  - · Added header text for general specification conditions.
  - Added footnote for clarification of input voltage limits.
- · Minor typographical corrections, including capitalization, mis-spellings and punctuation marks, throughout document.
- Minor formatting and styling updates, including table formats, TOC location, and boilerplate information throughout document.

#### **Revision 0.1**

April 27th, 2017

Initial release.