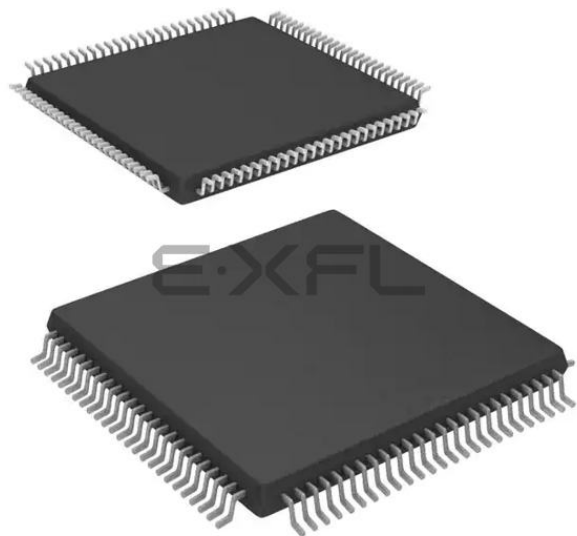




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b320f2048gq100-a

3.8.4	Capacitive Sense (CSEN)	.18
3.8.5	Digital to Analog Current Converter (IDAC)	.18
3.8.6	Digital to Analog Converter (VDAC)	.18
3.8.7	Operational Amplifiers	.18
3.8.8	Liquid Crystal Display Driver (LCD)	.18
3.9	Reset Management Unit (RMU)	.18
3.10	Core and Memory	.18
3.10.1	Processor Core	.18
3.10.2	Memory System Controller (MSC)	.19
3.10.3	Linked Direct Memory Access Controller (LDMA)	.19
3.10.4	Bootloader	.19
3.11	Memory Map	.20
3.12	Configuration Summary	.22
4.	Electrical Specifications	23
4.1	Electrical Characteristics	.23
4.1.1	Absolute Maximum Ratings	.24
4.1.2	Operating Conditions	.25
4.1.3	Thermal Characteristics	.27
4.1.4	DC-DC Converter	.28
4.1.5	5V Regulator	.30
4.1.6	Backup Supply Domain	.31
4.1.7	Current Consumption	.32
4.1.8	Wake Up Times	.39
4.1.9	Brown Out Detector (BOD)	.40
4.1.10	Oscillators	.41
4.1.11	Flash Memory Characteristics	.48
4.1.12	General-Purpose I/O (GPIO)	.49
4.1.13	Voltage Monitor (VMON)	.51
4.1.14	Analog to Digital Converter (ADC)	.52
4.1.15	Analog Comparator (ACMP)	.54
4.1.16	Digital to Analog Converter (VDAC)	.57
4.1.17	Current Digital to Analog Converter (IDAC)	.60
4.1.18	Capacitive Sense (CSEN)	.62
4.1.19	Operational Amplifier (OPAMP)	.64
4.1.20	LCD Driver	.67
4.1.21	Pulse Counter (PCNT)	.68
4.1.22	Analog Port (APORT)	.68
4.1.23	I2C	.69
4.1.24	USART SPI	.72
4.1.25	External Bus Interface (EBI)	.75
4.1.26	Ethernet (ETH)	.84
4.1.27	Serial Data I/O Host Controller (SDIO)	.87
4.1.28	Quad SPI (QSPI)	.102
4.2	Typical Performance Curves	.106
4.2.1	Supply Current	.107
4.2.2	DC-DC Converter	.113

3.6.6 Quad-SPI Flash Controller (QSPI)

The QSPI provides access to a wide range of flash devices with wide I/O busses. The I/O and clocking configuration is flexible and supports many types of devices. Up to 8-bit wide interfaces are supported. The QSPI handles opcodes, status flag polling, and timing configuration automatically.

The external flash memory is mapped directly to internal memory to allow random access to any word in the flash and direct code execution. An integrated instruction cache minimizes latency and allows efficient code execution. Execute in Place (XIP) is supported for devices with this feature.

Large data chunks can be transferred with DMA as efficiently as possible with high throughput and minimal bus load, utilizing an integrated 1 kB SRAM FIFO.

3.6.7 SDIO Host Controller (SDIO)

The SDIO is an SD3.01 / SDIO3.0 / eMMC4.51-compliant Host Controller interface for transferring data to and from SD/MMC/SDIO devices. The module conforms to the SD Host Controller Standard Specification Version 3.00. The Host Controller handles SDIO/SD/MMC Protocol at the transmission level, packing data, adding cyclic redundancy check (CRC), Start/End bits, and checking for transaction format correctness.

3.6.8 Universal Serial Bus (USB)

The USB is a full-speed/low-speed USB 2.0 compliant host/device controller. The USB can be used in device and host-only configurations, while a clock recovery mechanism allows crystal-less operation in device mode. The USB block supports both full speed (12 MBit/s) and low speed (1.5 MBit/s) operation. When operating as a device, a special Low Energy Mode ensures the current consumption is optimized, enabling USB communications on a strict power budget. The USB device includes an internal dedicated Descriptor-Based Scatter/Gather DMA and supports up to 6 OUT endpoints and 6 IN endpoints, in addition to endpoint 0. The on-chip PHY includes internal pull-up and pull-down resistors, as well as voltage comparators for monitoring the VBUS voltage and A/B device identification using the ID line.

3.6.9 Ethernet (ETH)

The Ethernet peripheral is compliant with IEEE 802.3-2002 for Ethernet MAC. It supports 802.1AS and IEEE 1588 precision clock synchronization protocol, as well as 802.3az Energy Efficient Ethernet. The ETH supports a wide variety of frame formats and standard operating modes such as MII/RMII. Direct Memory Access (DMA) support makes it possible to transmit and receive large frames at high data rates with minimal CPU overhead. The Ethernet peripheral supports 10 Mbps and 100 Mbps operation, and includes a total of 8 kB of dedicated dual-port RAM FIFO (4 kB for TX and 4 kB for RX).

3.6.10 Controller Area Network (CAN)

The CAN peripheral provides support for communication at up to 1 Mbps over CAN protocol version 2.0 part A and B. It includes 32 message objects with independent identifier masks and retains message RAM in EM2. Automatic retransmission may be disabled in order to support Time Triggered CAN applications.

3.6.11 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.6.12 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range ⁶	T_A	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage ²	V_{AVDD}		1.8	3.3	3.8	V
VREGVDD operating supply voltage ^{2 1}	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	$I_{VREGVDD}$	DCDC in bypass, $T \leq 85^\circ\text{C}$	—	—	200	mA
		DCDC in bypass, $T > 85^\circ\text{C}$	—	—	100	mA
DVDD operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage	V_{IOVDD}	All IOVDD pins ⁵	1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor ^{3 4}	$C_{DECOUPLE}$		0.75	1.0	2.75	μF
HFCORECLK frequency	f_{CORE}	VSCALE2, MODE = WS3	—	—	72	MHz
		VSCALE2, MODE = WS2	—	—	54	MHz
		VSCALE2, MODE = WS1	—	—	36	MHz
		VSCALE2, MODE = WS0	—	—	18	MHz
		VSCALE0, MODE = WS2	—	—	20	MHz
		VSCALE0, MODE = WS1	—	—	14	MHz
		VSCALE0, MODE = WS0	—	—	7	MHz
HFCLK frequency	f_{HFCLK}	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFSRCCLK frequency	$f_{HFSRCCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFBUSCLK frequency	$f_{HFBUSCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERCLK frequency	$f_{HFPERCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERBCLK frequency	$f_{HFPERBCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFPERCCLK frequency	$f_{HFPERCCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz

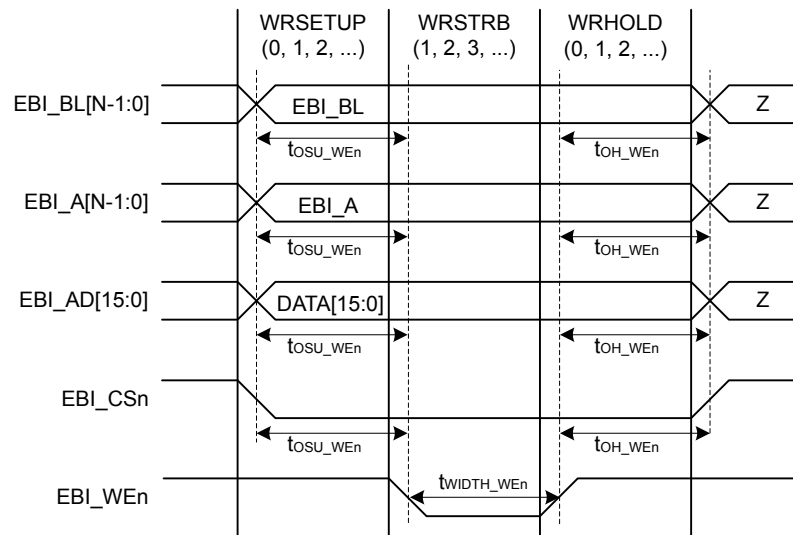


Figure 4.3. EBI Write Enable Output Timing Diagram

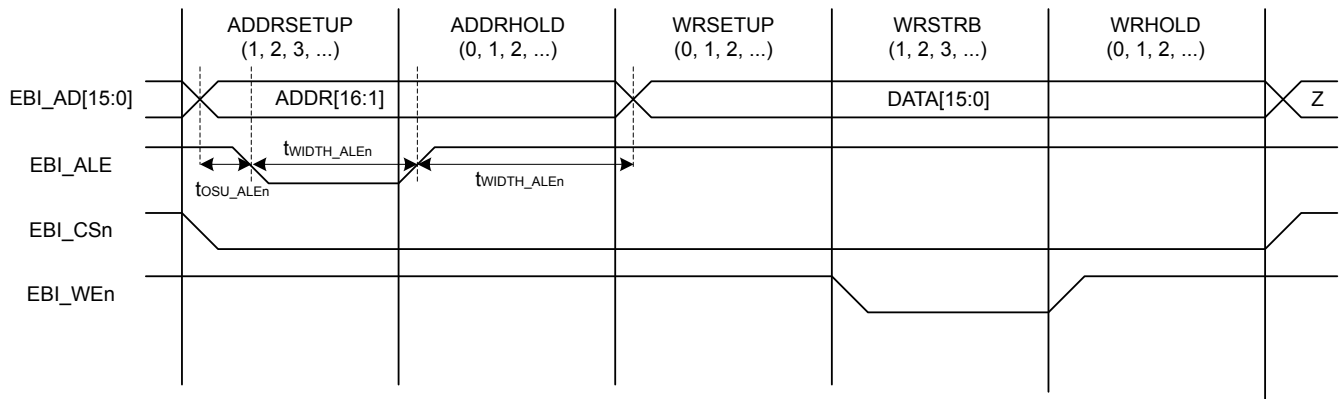


Figure 4.4. EBI Address Latch Enable Output Timing Diagram

EBI TFT Output Timing

All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.39. EBI TFT Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, EBI_DCLK to EBI_AD invalid	t_{OH_DCLK}	IOVDD $\geq$ 1.62 V	-23 + (TFTHOLD * t_{HFCOR-} ECLK)	—	—	ns
		IOVDD $\geq$ 3.0 V	-12 + (TFTHOLD * t_{HFCOR-} ECLK)	—	—	ns
Output setup time, EBI_AD valid to EBI_DCLK	t_{OSU_DCLK}	IOVDD $\geq$ 1.62 V	-11 + (TFTSET- UP * t_{HFCOR-} ECLK)	—	—	ns
		IOVDD $\geq$ 3.0 V	-9 + (TFTSET- UP * t_{HFCOR-} ECLK)	—	—	ns

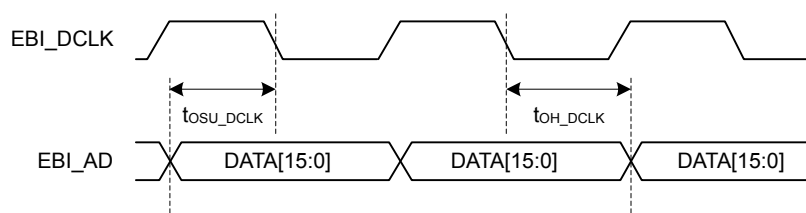


Figure 4.6. EBI TFT Output Timing

SDIO MMC SDR Mode Timing at 1.8 V

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.50. SDIO MMC SDR Mode Timing (Location 0, 1.8V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F _{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	25	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t _{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t _{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t _R		1.96	8.27	—	ns
Clock fall time	t _F		1.67	6.90	—	ns
Input setup time, CMD, DAT[0:7] valid to SD_CLK	t _{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:7] change	t _{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:7] valid	t _{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD, DAT[0:7] change	t _{OH}		3	—	—	ns

QSPI SDR Mode Timing (Locations 1, 2)

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 34, RX DLL = 59, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.55. QSPI SDR Mode Timing (Locations 1, 2)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Full SCLK period	T		$(1/F_{SCLK}) * 0.95$	—	—	ns
Output valid	t_{OV}		—	—	$T/2 - 2.1$	ns
Output hold	t_{OH}		$T/2 - 42.3$	—	—	ns
Input setup	t_{SU}		$48.2 - T/2$	—	—	ns
Input hold	t_H		$T/2 - 5.1$	—	—	ns

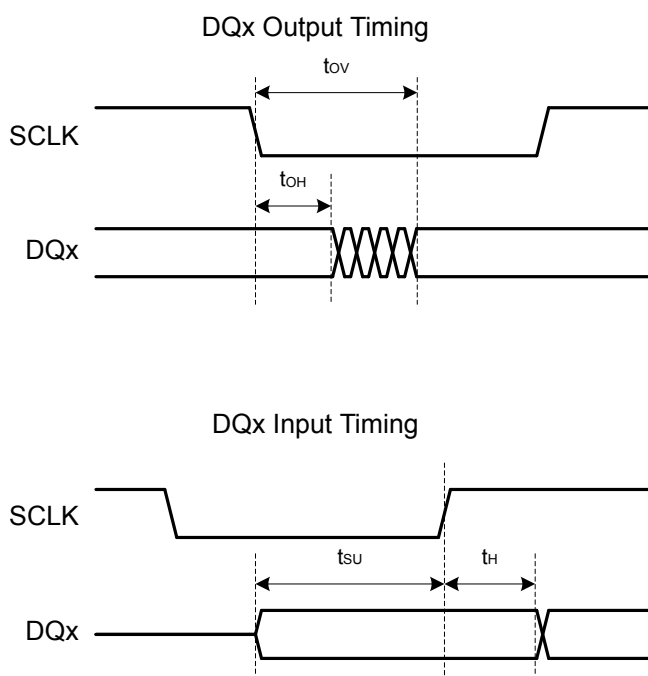


Figure 4.21. QSPI SDR Timing Diagrams

QSPI SDR Flash Timing Example

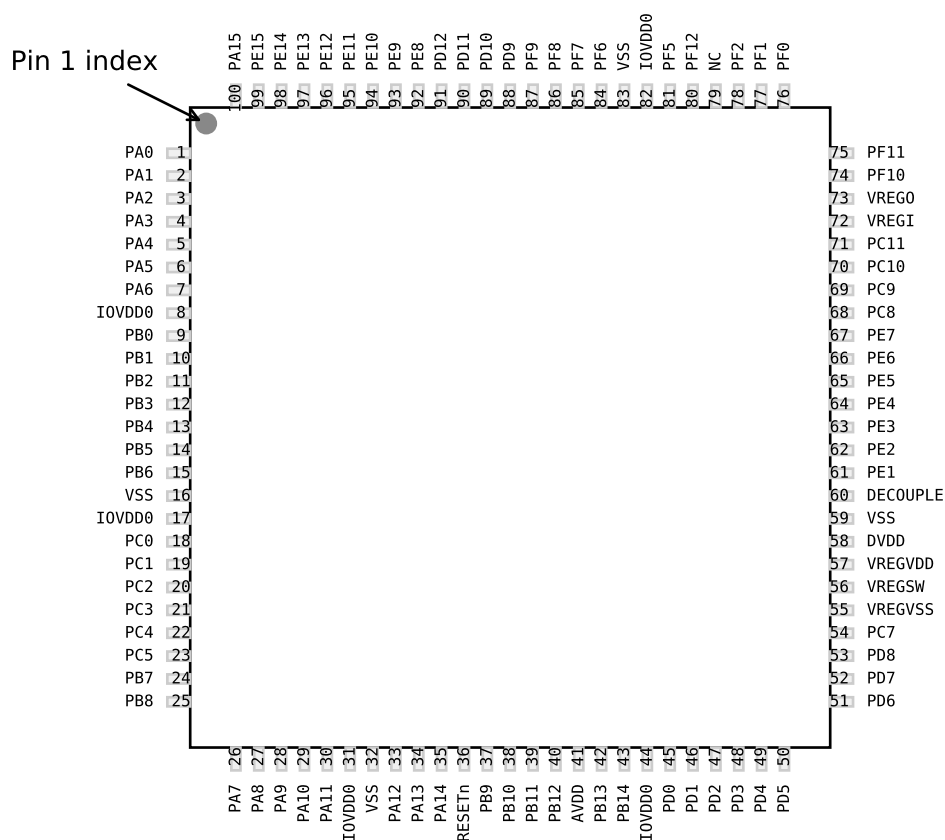
This example uses timing values for location 0 (SDR mode) to demonstrate the calculation of allowable flash timing using the QSPI in SDR mode.

- Using a configured SCLK frequency (F_{SCLK}) of 19 MHz:
- The resulting minimum period, $T(\min) = (1/F_{SCLK}) * 0.95 = 50.0$ ns.
- Flash will see a minimum setup time of $T/2 - t_{OV} = T/2 - (T/2 - 2.4) = 2.4$ ns.
- Flash will see a minimum hold time of $T/2 + t_{OH} = T/2 + (T/2 - 32.9) = T - 32.9 = 50.0 - 32.9 = 17.1$ ns.
- Flash can have a maximum output valid time of $T/2 - t_{SU} = T/2 - (36.2 - T/2) = T - 36.2 = 50.0 - 36.2 = 13.8$ ns.
- Flash can have a minimum output hold time of $t_H - T/2 = (T/2 - 3.3) - T/2 = -3.3$ ns.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PD8	H8	GPIO	PD5	H9	GPIO
PD6	H10	GPIO	PD7	H11	GPIO
PC1	J1	GPIO (5V)	PC3	J2	GPIO (5V)
PD15	J3	GPIO (5V)	PA12	J4	GPIO (5V)
PA9	J5	GPIO	PA10	J6	GPIO
PB9	J7	GPIO (5V)	PB10	J8	GPIO (5V)
PD2	J9	GPIO (5V)	PD3	J10	GPIO
PD4	J11	GPIO	PB7	K1	GPIO
PC4	K2	GPIO	PA13	K3	GPIO (5V)
PA11	K5	GPIO	RESETn	K6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	K8 K9 L10	Analog power supply.	PD1	K11	GPIO
PB8	L1	GPIO	PC5	L2	GPIO
PA14	L3	GPIO	PB11	L5	GPIO
PB12	L6	GPIO	PB13	L8	GPIO
PB14	L9	GPIO	PD0	L11	GPIO (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.



The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.9. EFM32GG11B5xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO (5V)
PC9	42	GPIO (5V)	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.21 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to [5.20 GPIO Functionality Table](#) for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.21. Alternate Functionality Overview

Alternate	LOCATION		Description
Functionality	0 - 3	4 - 7	
ACMP0_O	0: PE13 1: PE2 2: PD6 3: PB11	4: PA6 5: PB0 6: PB2 7: PB3	Analog comparator ACMP0, digital output.
ACMP1_O	0: PF2 1: PE3 2: PD7 3: PA12	4: PA14 5: PB9 6: PB10 7: PA5	Analog comparator ACMP1, digital output.
ACMP2_O	0: PD8 1: PE0 2: PE1 3: PI0	4: PI1 5: PI2	Analog comparator ACMP2, digital output.
ACMP3_O	0: PF0 1: PC15 2: PC14 3: PC13	4: PI4 5: PI5	Analog comparator ACMP3, digital output.
ADC0_EXTN	0: PD7		Analog to digital converter ADC0 external reference input negative pin.
ADC0_EXTP	0: PD6		Analog to digital converter ADC0 external reference input positive pin.
ADC1_EXTN	0: PD7		Analog to digital converter ADC1 external reference input negative pin.
ADC1_EXTP	0: PD6		Analog to digital converter ADC1 external reference input positive pin.
BOOT_RX	0: PF1		Bootloader RX.
BOOT_TX	0: PF0		Bootloader TX.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PF6		LCD segment line 24.
LCD_SEG25	0: PF7		LCD segment line 25.
LCD_SEG26	0: PF8		LCD segment line 26.
LCD_SEG27	0: PF9		LCD segment line 27.
LCD_SEG28	0: PD9		LCD segment line 28.
LCD_SEG29	0: PD10		LCD segment line 29.
LCD_SEG30	0: PD11		LCD segment line 30.
LCD_SEG31	0: PD12		LCD segment line 31.
LCD_SEG32	0: PB0		LCD segment line 32.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
QSPI0_DQ7	0: PE11 1: PB6 2: PG8		Quad SPI 0 Data 7.
QSPI0_DQS	0: PF9 1: PE15 2: PG11		Quad SPI 0 Data S.
QSPI0_SCLK	0: PF6 1: PE14 2: PG0		Quad SPI 0 Serial Clock.
SDIO_CD	0: PF8 1: PC4 2: PA6 3: PB10		SDIO Card Detect.
SDIO_CLK	0: PE13 1: PE14		SDIO Serial Clock.
SDIO_CMD	0: PE12 1: PE15		SDIO Command.
SDIO_DAT0	0: PE11 1: PA0		SDIO Data 0.
SDIO_DAT1	0: PE10 1: PA1		SDIO Data 1.
SDIO_DAT2	0: PE9 1: PA2		SDIO Data 2.
SDIO_DAT3	0: PE8 1: PA3		SDIO Data 3.
SDIO_DAT4	0: PD12 1: PA4		SDIO Data 4.
SDIO_DAT5	0: PD11 1: PA5		SDIO Data 5.
SDIO_DAT6	0: PD10 1: PB3		SDIO Data 6.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM4_CDTI2	0: PD3		Timer 4 Complimentary Dead Time Insertion channel 2.
TIM5_CC0	0: PE4 1: PE7 2: PH13 3: PI0	4: PC8 5: PC11 6: PC14 7: PF12	Timer 5 Capture Compare input / output channel 0.
TIM5_CC1	0: PE5 1: PH11 2: PH14 3: PI1	4: PC9 5: PC12 6: PF10 7: PF13	Timer 5 Capture Compare input / output channel 1.
TIM5_CC2	0: PE6 1: PH12 2: PH15 3: PI2	4: PC10 5: PC13 6: PF11 7: PF14	Timer 5 Capture Compare input / output channel 2.
TIM6_CC0	0: PG0 1: PG6 2: PG12 3: PH2	4: PH8 5: PB13 6: PD1 7: PD4	Timer 6 Capture Compare input / output channel 0.
TIM6_CC1	0: PG1 1: PG7 2: PG13 3: PH3	4: PH9 5: PB14 6: PD2 7: PD5	Timer 6 Capture Compare input / output channel 1.
TIM6_CC2	0: PG2 1: PG8 2: PG14 3: PH4	4: PH10 5: PD0 6: PD3 7: PD6	Timer 6 Capture Compare input / output channel 2.
TIM6_CDTI0	0: PG3 1: PG9 2: PE4 3: PH5		Timer 6 Complimentary Dead Time Insertion channel 0.
TIM6_CDTI1	0: PG4 1: PG10 2: PE5 3: PH6		Timer 6 Complimentary Dead Time Insertion channel 1.
TIM6_CDTI2	0: PG5 1: PG11 2: PE6 3: PH7		Timer 6 Complimentary Dead Time Insertion channel 2.
U0_CTS	0: PF8 1: PE2 2: PA5 3: PC13	4: PB7 5: PD5	UART0 Clear To Send hardware flow control input.
U0_RTS	0: PF9 1: PE3 2: PA6 3: PC12	4: PB8 5: PD6	UART0 Request To Send hardware flow control output.
U0_RX	0: PF7 1: PE1 2: PA4 3: PC15	4: PC5 5: PF2 6: PE4	UART0 Receive input.

Table 5.28. ADC1 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSADC1Y	BUSADC1X	Bus
	PF15	PF15			PB15	PB15				CH31
PF14			PF14	PB14			PB14			CH30
	PF13	PF13			PB13	PB13				CH29
PF12			PF12	PB12			PB12			CH28
	PF11	PF11			PB11	PB11				CH27
PF10			PF10	PB10			PB10			CH26
	PF9	PF9			PB9	PB9				CH25
PF8			PF8							CH24
	PF7	PF7								CH23
PF6			PF6	PB6			PB6			CH22
	PF5	PF5			PB5	PB5				CH21
PF4			PF4	PB4			PB4			CH20
	PF3	PF3			PB3	PB3				CH19
PF2			PF2	PB2			PB2			CH18
	PF1	PF1			PB1	PB1				CH17
PF0			PF0	PB0			PB0			CH16
	PE15	PE15			PA15	PA15				CH15
PE14			PE14	PA14			PA14			CH14
	PE13	PE13			PA13	PA13				CH13
PE12			PE12	PA12			PA12			CH12
	PE11	PE11			PA11	PA11				CH11
PE10			PE10	PA10			PA10			CH10
	PE9	PE9			PA9	PA9				CH9
PE8			PE8	PA8			PA8			CH8
	PE7	PE7			PA7	PA7		PH7	PH7	CH7
PE6			PE6	PA6			PA6	PH6	PH6	CH6
	PE5	PE5			PA5	PA5		PH5	PH5	CH5
PE4			PE4	PA4			PA4	PH4	PH4	CH4
					PA3	PA3		PH3	PH3	CH3
				PA2			PA2	PH2	PH2	CH2
	PE1	PE1			PA1	PA1		PH1	PH1	CH1
PE0			PE0	PA0			PA0	PH0	PH0	CH0

Table 5.29. CSEN Bus and Pin Mapping

APORT4Y		APORT4X	APORT2Y	APORT2X
BUSDY	BUSDX	BUSBY	BUSBX	
	PF15		PB15	
PF14		PB14		
	PF13		PB13	
PF12		PB12		
	PF11		PB11	
PF10		PB10		
	PF9		PB9	
PF8				
	PF7			
PF6		PB6		
	PF5		PB5	
PF4		PB4		
	PF3		PB3	
PF2		PB2		
	PF1		PB1	
PF0		PB0		
	PE15		PA15	
PE14		PA14		
	PE13		PA13	
PE12		PA12		
	PE11		PA11	
PE10		PA10		
	PE9		PA9	
PE8		PA8		
	PE7		PA7	
PE6		PA6		
	PE5		PA5	
PE4		PA4		
			PA3	
		PA2		
	PE1		PA1	
PE0		PA0		

CEXT									
Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24
	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23
CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13
CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3
CH2	CH1	CH0							
CEXT_SENSE									
APORT4Y	APORT4X	APORT2Y	APORT2X						
BUSDY	BUSDX	BUSBY	BUSBX						
	PF15		PB15						
PF14		PB14							
	PF13		PB13						
PF12		PB12							
	PF11		PB11						
PF10		PB10							
	PF9		PB9						
PF8									
	PF7								
PF6		PB6							
	PF5		PB5						
PF4		PB4							
	PF3		PB3						
PF2		PB2							
	PF1		PB1						
PF0		PB0							
	PE15		PA15						
PE14		PA14							
	PE13		PA13						
PE12		PA12							
	PE11		PA11						
PE10		PA10							
	PE9		PA9						
PE8		PA8							
	PE7		PA7						
PE6		PA6							
	PE5		PA5						
PE4		PA4							
			PA3						
		PA2							
	PE1		PA1						
PE0		PA0							

Table 5.30. IDAC0 Bus and Pin Mapping

APORT1Y	APORT1X	Port
BUSCY	BUSCX	Bus
PF15		CH31
	PF14	CH30
PF13		CH29
	PF12	CH28
PF11		CH27
	PF10	CH26
PF9		CH25
	PF8	CH24
PF7		CH23
	PF6	CH22
PF5		CH21
	PF4	CH20
PF3		CH19
	PF2	CH18
PF1		CH17
	PF0	CH16
PE15		CH15
	PE14	CH14
PE13		CH13
	PE12	CH12
PE11		CH11
	PE10	CH10
PE9		CH9
	PE8	CH8
PE7		CH7
	PE6	CH6
PE5		CH5
	PE4	CH4
		CH3
		CH2
PE1		CH1
	PE0	CH0

7. BGA152 Package Specifications

7.1 BGA152 Package Dimensions

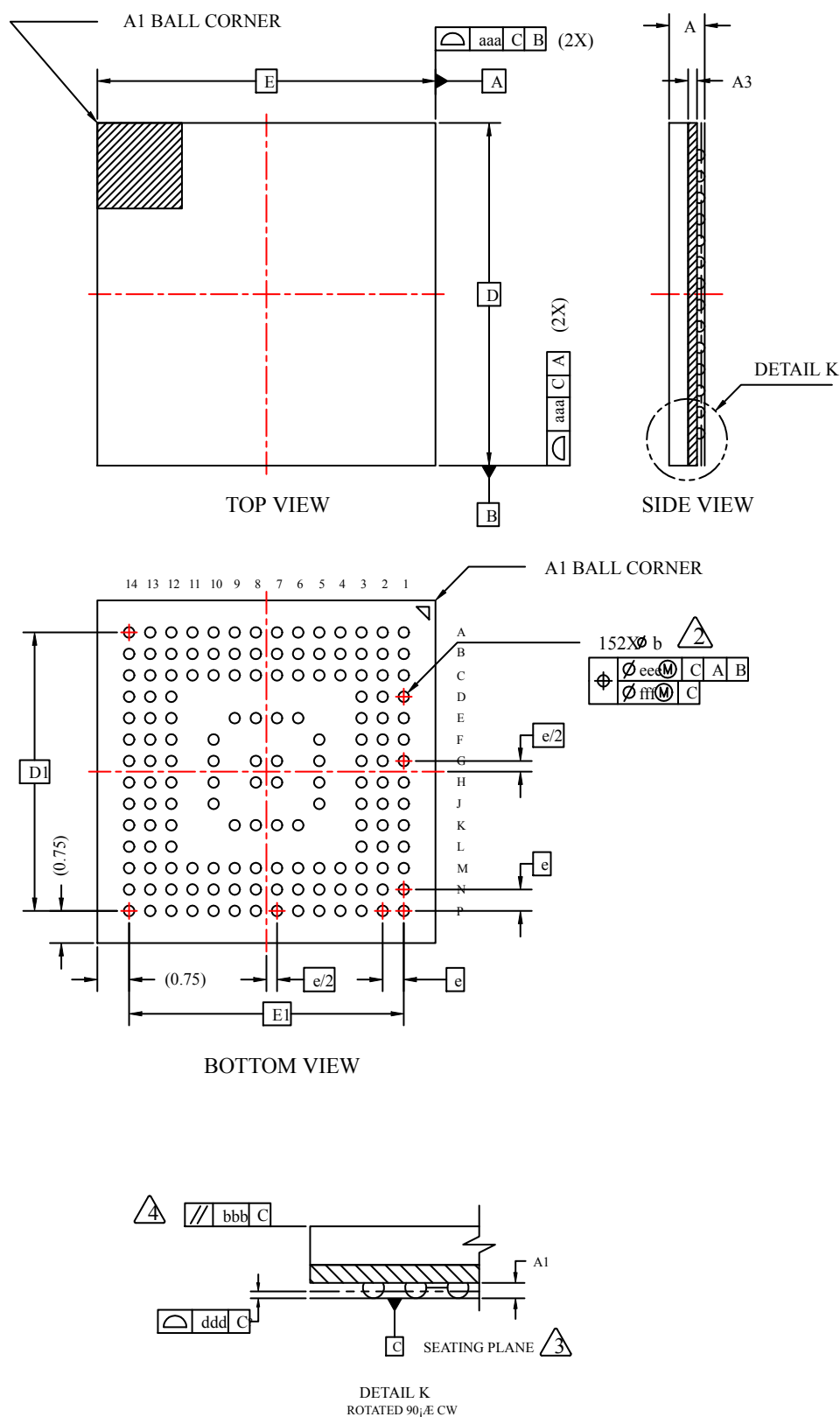


Figure 7.1. BGA152 Package Drawing

8.2 BGA120 PCB Land Pattern

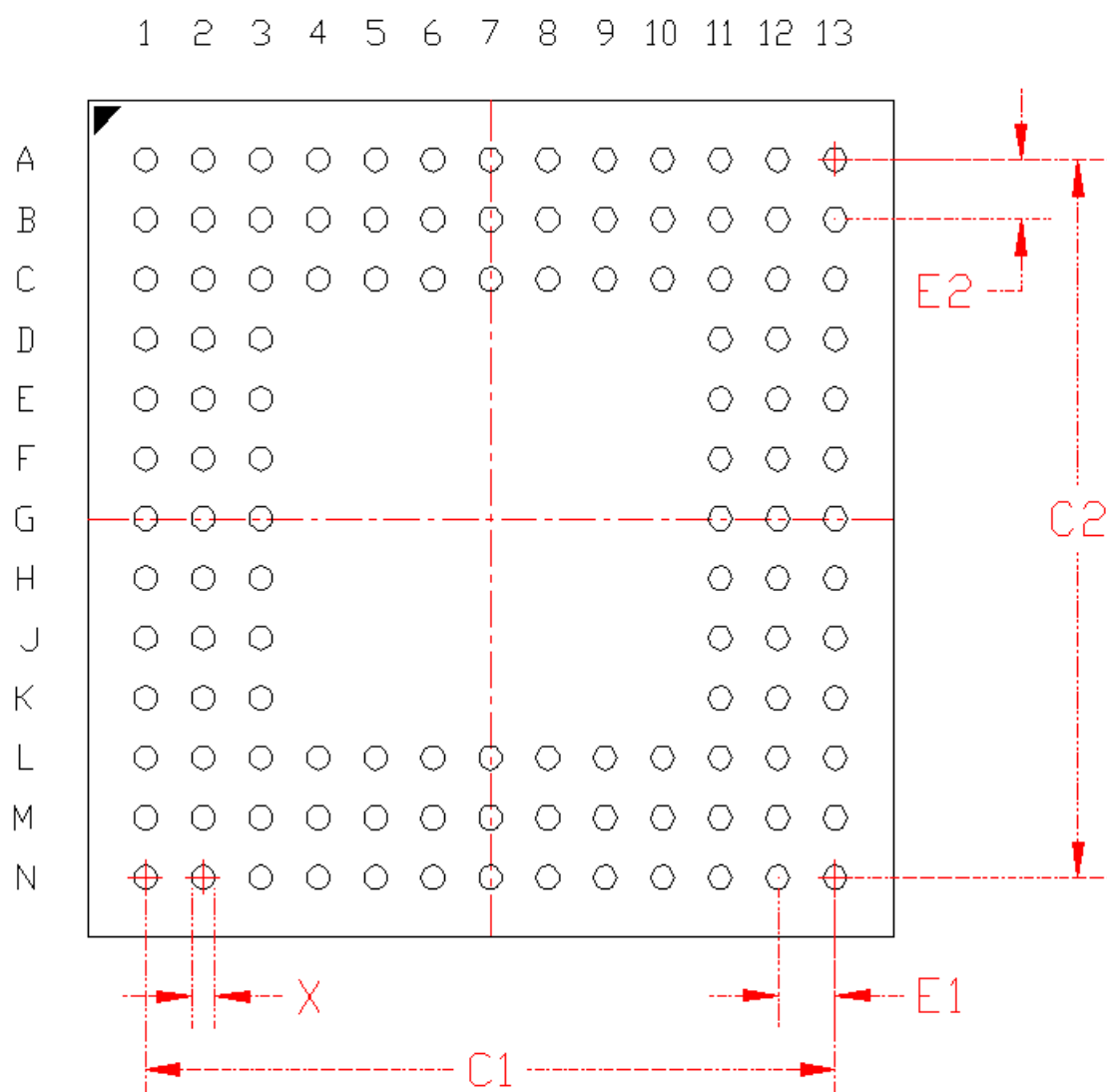


Figure 8.2. BGA120 PCB Land Pattern Drawing

12. QFN64 Package Specifications

12.1 QFN64 Package Dimensions

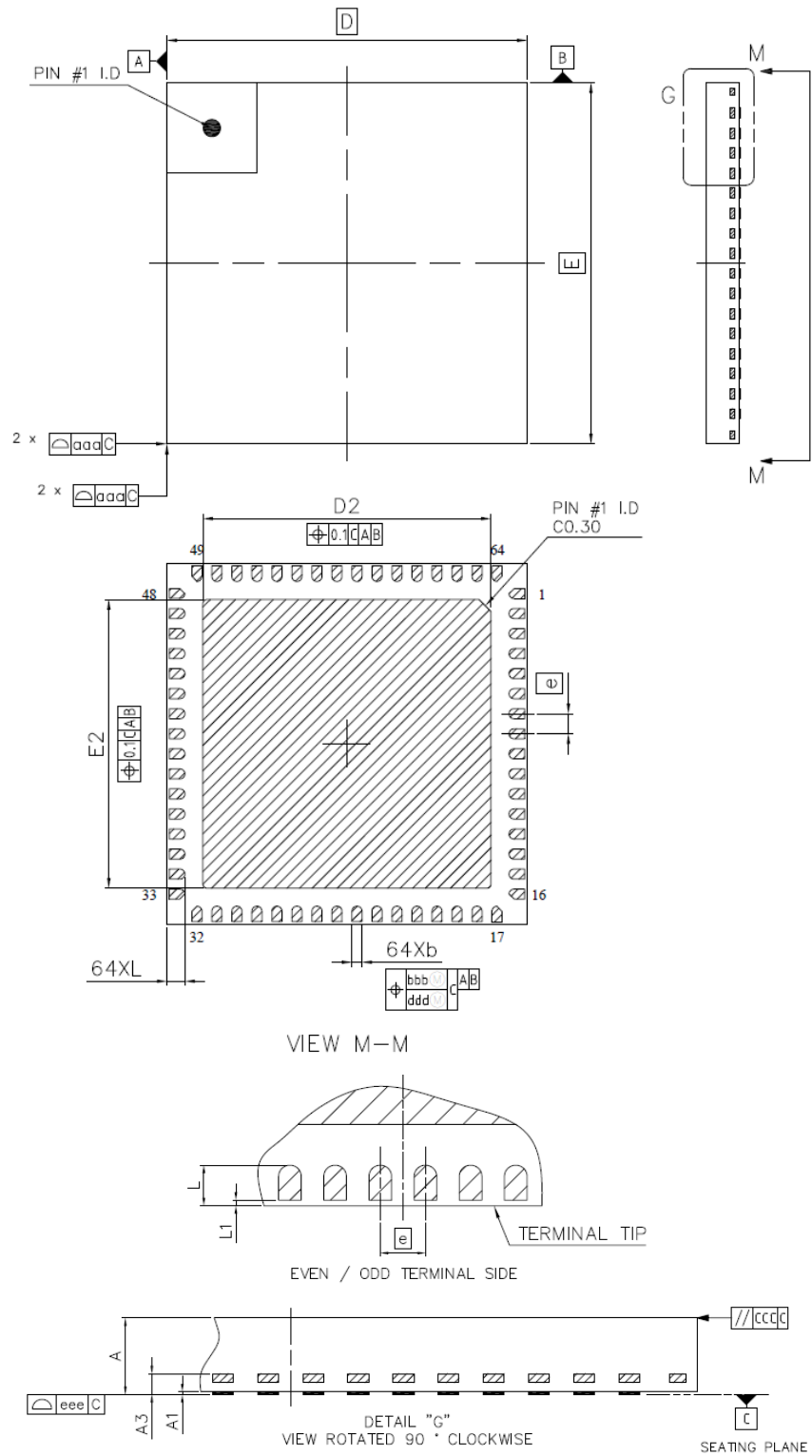


Figure 12.1. QFN64 Package Drawing